How Many Bits are Needed For Memory:

Miller (+Tom's) Useless Piece of Sheet

$2^{\#\text{bits}} - 1 \le \#\text{of bytes}$

Extra Note Space:
"Courage Need Not Be Remembered, For It Is Never Forgotten"

Conversions:

Binary: $\underline{\ \ }_{128}\ \underline{\ \ }_{64}\ \underline{\ \ }_{32}\ \underline{\ \ }_{16}\ \ \underline{\ \ }_{8}\ \underline{\ \ }_{4}\ \underline{\ \ }_{2}\ \underline{\ \ }_{1}$ → i.e. $\underset{7654}{1101}\ \underset{3210}{0101}$

→ Hex: $\underset{3210}{1101}\ \underset{3210}{0101} \to \underbrace{2^3+2^2+2^0}_{13}\ \underbrace{2^2+2^0}_{5} \to \underline{D5}$

→ Dec: $\underset{1}{2^0}+\underset{4}{2^2}+\underset{16}{2^4}+\underset{64}{2^6}+\underset{128}{2^7} \to \underline{213}$

Binary(2) → Decimal(10) → Add up the locations of 1s, sum is decimal

↳ Hex(16) → Add up locations of 1s, split into 2 groups of 4, first group is first letter/number, second is the second

In Hex:
10: A
11: B
12: C
13: D
14: E
15: F

Dec → Bin: 174 → $\underset{2^7}{128}$, 46 → $\underset{2^5}{32}$, 18 → $\underset{2^4}{16}$, $\underset{2^1}{2}$

Binary Result: $\underset{7}{1}\ \underset{6}{0}\ \underset{5}{1}\ \underset{4}{1}\ \underset{3}{0}\ \underset{2}{0}\ \underset{1}{1}\ \underset{0}{0}$

Decimal To Binary: Make a tree, find larges 2^x in it, keep going until 1 or 0 is left, the x in 2^x is the location of 1 in binary

Decimal To Hex: Convert to binary, then to Decimal

How to Convert from 1 Base to Any Base:

I.E 357_{10} to base 4

$4\overline{)357} \to 89\ r\ 1$
$89 \to 22\ r\ 1$
$22 \to 5\ r\ 2$
$5 \to 1\ r\ 1$

$\to 357_{10} = 1121_4$

Extra Notes:
$(5743)_8 \to 10$
$5\times 8+7=47$
↳ $\times 8+4=380 \to \times 8+3=3043$
↳ $(3043)_{10}$

$1+1=2$
↳ $2+2=4$
↳ $4+4=8$

CMOS Power:

$\text{Power} = C \times V_{DD}^2 \times \text{frequency}$

$A+\overline{A}B = A+B$

$\overline{\overline{A}} = A$ ✓

Simplification Methods:

DeMorgan's Law:

$\overline{(X+Y)} = \overline{X}\cdot\overline{Y}$

$+ \longleftrightarrow \cdot$

$x \longleftrightarrow \overline{x}$

Principle of Duality:
- Switch $+ \longleftrightarrow \cdot$
- Switch $0 \longleftrightarrow 1$
- Keep Variables the Same $Y \not\longleftrightarrow \overline{Y}$

Various Rules:

$(x+y) = \overline{\overline{(x+y)}} \to (\overline{\overline{x}\cdot\overline{y}}) \to (x+y)$

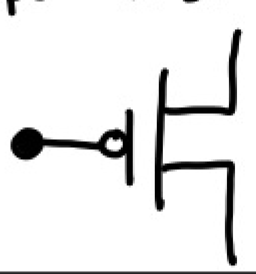
Equivalent

Identities	$X+0=X$	$X\cdot 1 = X$
Null Elements	$X+1=1$	$X\cdot 0=0$
Idempotency	$X+X=X$	$X\cdot X = X$
Involution	$\overline{\overline{(X)}}=X$	
Complements	$X+\overline{X}=1$	$X\cdot\overline{X}=0$

Commutativity	$X+Y=Y+X$	$X\cdot Y = Y\cdot X$
Associativity	$(X+Y)+Z = X+(Y+Z)$	$(X\cdot Y)\cdot Z = X\cdot(Y\cdot Z)$
Distributivity	$X\cdot Y+X\cdot Z = X\cdot(Y+Z)$	$(X+Y)\cdot(X+Z)=X+(Y\cdot Z)$
Covering	$X+X\cdot Y=X$	$X\cdot(X+Y)=X$
Combining	$X\cdot Y+X\cdot\overline{Y}=X$	$(X+Y)\cdot(X+\overline{Y})=X$
Concensus	$X\cdot Y+\overline{X}\cdot Z+Y\cdot Z = X\cdot Y+\overline{X}\cdot Z$	$(X+Y)\cdot(\overline{X}+Z)\cdot(Y+Z) = (X+Y)\cdot(\overline{X}+Z)$

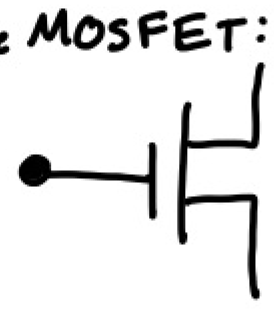
CMOS Gates:

P-Type MOSFET:



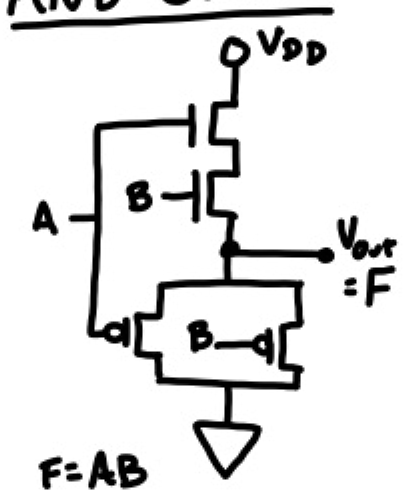
On when low input
Off when high input

N-Type MOSFET:



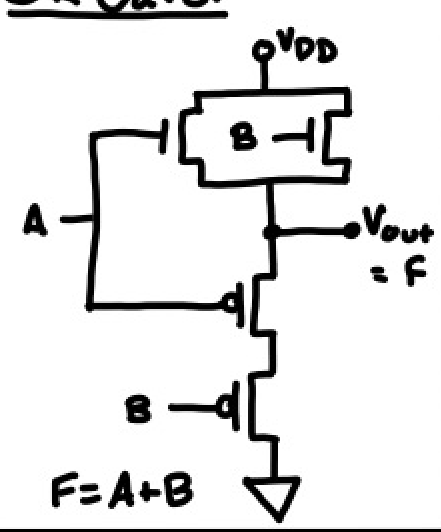
On when high input
Off when low input

AND Gate:



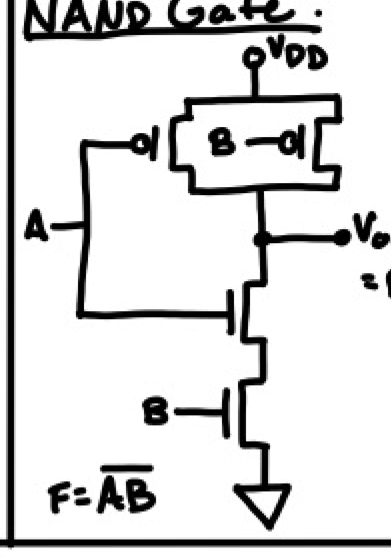
F=AB

OR Gate:



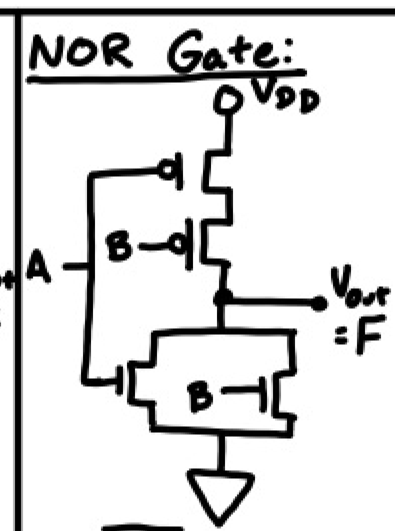
$F=A+B$

NAND Gate:



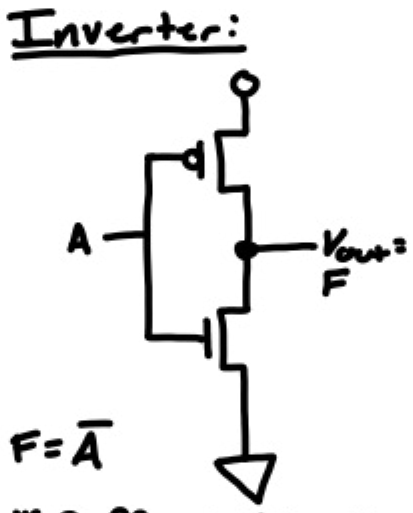
$F=\overline{AB}$

NOR Gate:



$F=\overline{A+B}$

Inverter:



$F=\overline{A}$

* Buffer = 2 inverters

- Fan in: # of inputs
- Can use inverter to invert → NAND ⟷ AND, NOR ⟷ OR

Extra Notes:

$V_{out} = V_{DD}e^{-\frac{t}{RC}} \to H \rightsquigarrow L$ $\quad V_{out} = V_{DD}(1-e^{-\frac{t}{RC}}) \to L \rightsquigarrow H$ $\quad \tau = RC = \frac{1}{2\pi f_c}$

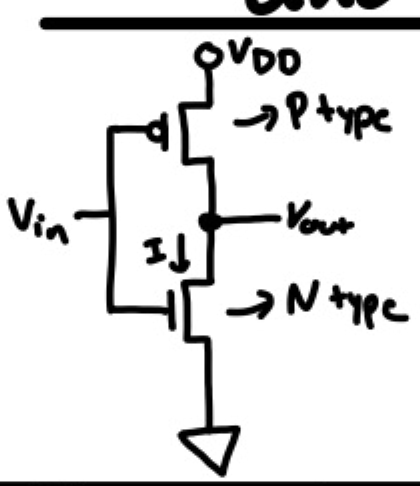
Noise Margins:

$NM_L : V_{IL} - V_{OL}$ → i.e. $NM_L(A\to B): V_{IL,max}(B) - V_{OL,max}(A)$

$NM_H: V_{OH} - V_{IH}$ → i.e. $NM_H(B\to A): V_{OH,min}(B) - V_{IH,min}(A)$

Extra Notes:
"You must believe in your own courage, which has led you to triumph over the many hardships you have faced... and you triumph once again!"

"On" and "Off" Resistance:



i.e.

Channel	On Ω	Off Ω
N	50	0.6 M
P	100	0.6 M

$V_{DD}=5V$

$V_{in}=0 \to$ Low, P on, N off

$V_{out} = V_{DD} \times \left(\frac{0.6M}{50+0.6M}\right)$

$V_{out} \approx 4.99$

$I = V/R$
$4.99/0.6M = \boxed{8.33\mu A}$

$P=IV$ → 4.99
↳ $\boxed{P=41.66\mu W}$

For answers to the exam you are currently taking, scan this QR Code:

Propogation Delay:

- 50% of input to 50% of output
- For NAND Gate: Last to turn to high or first to turn to low
- For NOR Gate: First to turn high or last to turn low
- For AND Gate: Last gate to turn to high or first gate to turn to low
- For OR Gate: First gate to turn to high or last gate to turn to low

Verilog Notes:
- End each statement with a semicolon ;
- Example Verilog Statement:

$\underset{\text{and}}{\underline{\text{gate}}}\ \underset{\text{u0}}{\underline{\text{name}}}\ (\underset{\text{(F}}{\underline{\text{output}}},\ \underset{\text{A,}}{\underline{\text{input 1}}},\ \underset{\text{B)}}{\underline{\text{input 2}}}\ \ldots)$

or

assign $\underline{\text{variable}}$ = $\underline{\text{expression}}$ $\xrightarrow{\text{i.e.}}$ assign F = A&B

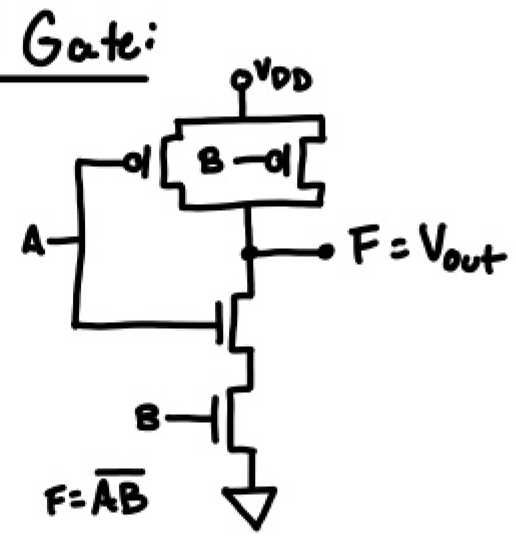
Example Problems:

XNOR of

11010100

1: $1 \oplus 1 = 1$
2: $1 \oplus 0 = 0$
3: $0 \oplus 1 = 0$
4: $0 \oplus 0 = 1$
5: $1 \oplus 1 = 1$
6: $1 \oplus 0 = 0$
7: $0 \oplus 0 = 1$ → Output is 1

NAND Gate:



Convert 143 which is in base 10 into base 2.

143 → 128, 15
128 / 7
15 → 8 / 3, 7
7 → 4 / 2, 3
3 → 2 / 1, 1 / 0

$\frac{1}{7}\ \frac{0}{6}\ \frac{0}{5}\ \frac{0}{4}\ \frac{1}{3}\ \frac{1}{2}\ \frac{1}{1}\ \frac{1}{0}$

A memory chip has a storage capacity of 32KB (kilobytes) (32000). Assuming it is byte addressable, i.e., one byte (8bits) of data are stored at each memory location. How many bits are needed to represent any memory address?

$2^x - 1 \geq 32000 \rightarrow x \geq 15$

Which one of the following truth tables correctly describes the logic function?

$F = \overline{M}\,\overline{N} + MP$

↳ M and N = 0

→ M and P = 1

M	N	P	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Baba Pooooooooooooosh!

Convert the following base 16 (hexadecimal) number to base 2 (binary):

(F6)16 → F = 15

$\frac{1}{8}\ \frac{1}{4}\ \frac{1}{2}\ \frac{1}{1}$ (15) $\quad \frac{0}{8}\ \frac{1}{4}\ \frac{1}{2}\ \frac{0}{1}$ (6)

Convert 10101100 which is base 2 to base 10

$\frac{1}{7}\ \frac{0}{6}\ \frac{1}{5}\ \frac{0}{4}\ \frac{1}{3}\ \frac{1}{2}\ \frac{0}{1}\ \frac{0}{0}$

$2^2 + 2^3 + 2^5 + 2^7 \rightarrow 4 + 8 + 32 + 128 = 172$

Which logic gate passes the input to output?

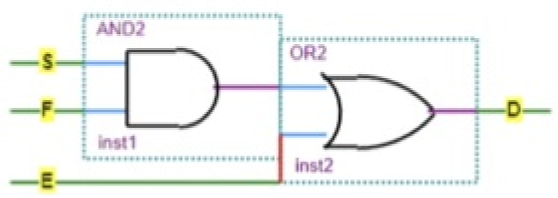
The Buffer Passes input to Output

An emergency exit door system works as follows:

The **door** opens (condition **D**) if:

OR(
1. **Smoke** detector turns on (condition **S**) and (AND) **fire alarm** turns on (condition **F**).
2. A person presses an **emergency button** (condition **E**)

Come up with a logic circuit that best describes the working of the emergency exit door.



Which four-input logic gate does this circuit implement?

$\overline{\left(\overline{\overline{(W+X)} \cdot \overline{(X+Y)}}\right) + \left(\overline{\overline{(Y+Z)} \cdot \overline{(X+Y)}}\right)}$

↓

$\overline{((w+x) + (x+y)) + ((y+z) + (x+y))}$

↓

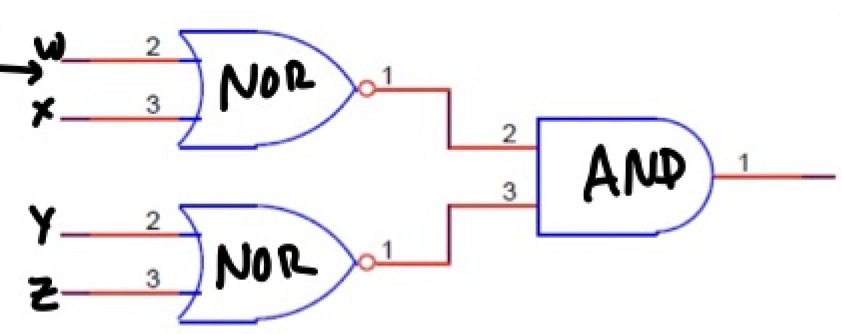
$\overline{(w+x+y) + (y+x+z)}$

↳ $\overline{w+x+y+z}$

What Circuit is This?

$Y = \left((\overline{A+B}) + C\right) \cdot \left(\overline{((\overline{A+B}) + D)}\right) \cdot \left(\overline{((\overline{A+B}) \cdot E)}\right)$

What is this logically equivalent to?



$(\overline{w+x}) \cdot (\overline{y+z})$

$\overline{\overline{w+x} \cdot \overline{y+z}}$

↓

$\overline{w+x+y+z}$

Extra Notes:

$2^0 = 1$ | $2^5 = 32$
$2^1 = 2$ | $2^6 = 64$
$2^2 = 4$ | $2^7 = 128$
$2^3 = 8$ | $2^8 = 256$
$2^4 = 16$ | $2^9 = 512$

A multiple-input XNOR gate (a multiple-input XOR gate followed by a NOT gate detects:

X	y	z	XNOR	
0	0	0	1	0 1s
0	0	1	0	
0	1	0	0	
0	1	1	1	2 1s
1	0	0	0	
1	0	1	1	2 1s
1	1	0	1	2 1s
1	1	1	0	

→ Even # of 1s

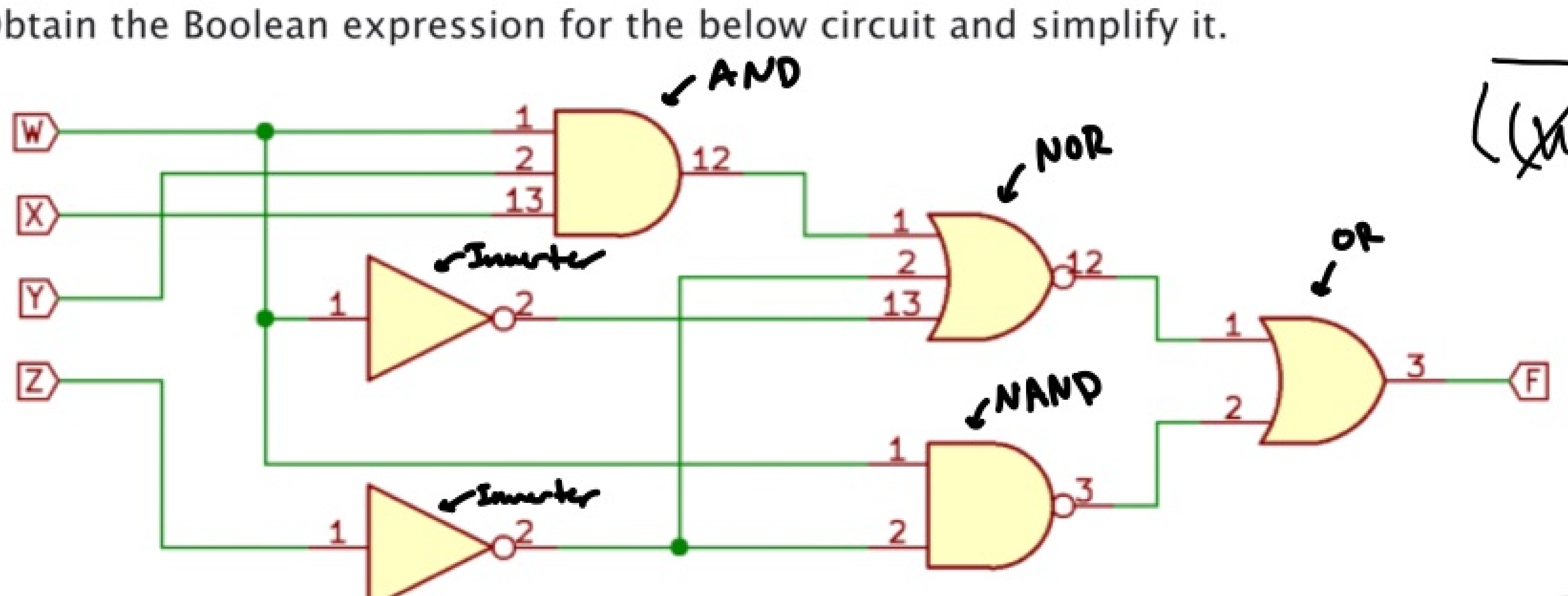
If the Boolean expression (X+Y')' . (X+Z) = X'YZ, then which of the following is true?
Hints: You may use the Principle of Duality.

$(\overline{X \cdot \overline{Y}}) + (X \cdot Z) = \overline{X} + Y + Z$

Did you scan the QR Code?

In Case of emergency

Obtain the Boolean expression for the below circuit and simplify it.



$\overline{((\cancel{W}XY) + \cancel{\overline{Y}} + \overline{Z})} + \overline{(W\,\overline{Z})}$

$\overline{W} + Z$

$(\overline{X+Y}) \cdot \overline{Z} + \overline{W} + Z$

$\overline{Z}X + \overline{Z}Y + \overline{W} + Z \rightarrow Z(1)$

$Z + \overline{W}$

A CMOS circuit dissipates 1200 mW when its Vdd is 4 V and its load capacitance is 5 nF (nanofarads). How much power will the CMOS circuit dissipate if the load capacitance is changed to 6 nF (same Vdd and frequency)?

$P_{new} = \frac{6}{5} P_{old}$ (1200mW)

Simplify the Boolean expression:

W' · (X+Y) · (X'+Y) · W + W · (X+Y+Z) + W' · (X'+Y+Z) + Z'

opposites

$0 \cdot (x+y) \cdot (\overline{x}+y)$ ↳ 0

$wx + wy + wz + \overline{w}\overline{x} + \overline{w}y + \overline{w}z + \overline{z}$

$Y(w+\overline{w}) = Y$

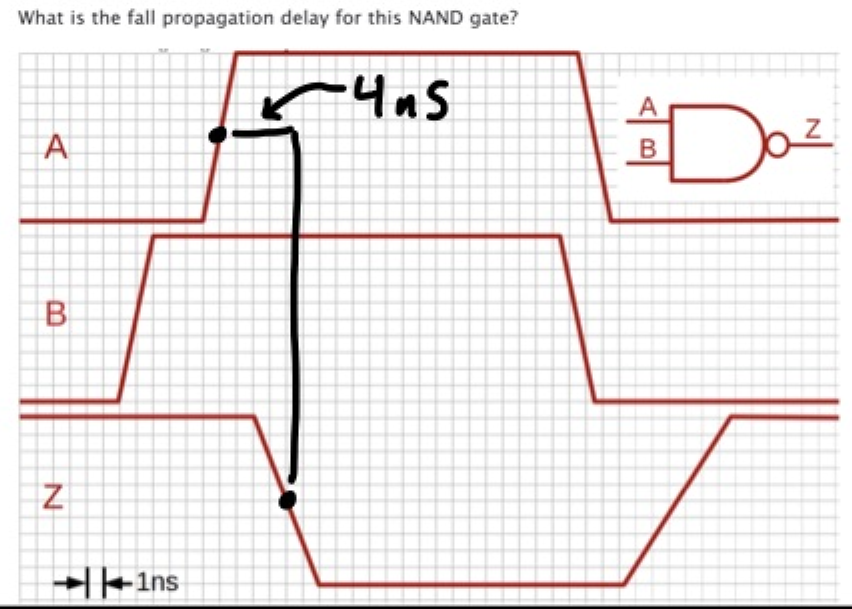
$Z(w+\overline{w}) = Z$

$wx + \overline{w}\overline{x} + y + z + \overline{z}$

$1 + y + wx + \overline{w}\overline{x} \rightarrow 1$

$0 + 1 = 1$

What is the fall propagation delay for this NAND gate?




```
module myCircuit (
    input wire x,
    input wire y,
    input wire z,
    output wire f
);
    wire w;
    assign f = w ^ z;
    assign w = ~(y & x);
endmodule
```

$w = \overline{(y \cdot x)}$

$f = w \oplus z$

$f = (\overline{y \cdot x}) \oplus z$

↳ x=0, y=1, z=0 $\quad f = (\overline{0 \cdot 1}) \oplus 0$

$\overline{0} \oplus 0 \rightarrow f = 1$

Given the DC characteristic tables for devices A and B, what is the high noise margin (NMH) for A->A (output of A connected to input of A)?

Logic Family A DC Characteristics				
V_{CC} = 5.0 V	$V_{OH_{min}}$ = 4.60 V	$V_{OL_{max}}$ = 0.30 V	$V_{IH_{min}}$ = 2.70 V	$V_{IL_{max}}$ = 1.30 V
V_{TH} = (V_{OH} - V_{OL})/2	I_{OH} = -11 mA	I_{OL} = 15 mA	I_{IH} = 2 µA	I_{IL} = -1 µA

Logic Family B DC Characteristics				
V_{CC} = 4.5 V	$V_{OH_{min}}$ = 4.30 V	$V_{OL_{max}}$ = 0.20 V	$V_{IH_{min}}$ = 2.90 V	$V_{IL_{max}}$ = 1.00 V
V_{TH} = (V_{OH} - V_{OL})/2	I_{OH} = -3 mA	I_{OL} = 15 mA	I_{IH} = 8 µA	I_{IL} = -4 µA

$NM_{H(A \rightarrow A)} = \underset{4.6}{V_{OH,min}(A)} - \underset{2.7}{V_{IH,min}(A)} = 1.9$

module func (input wire A, input wire B, output wire Y);
wire K, L, D, E;
not n1(K, A); → $K = \overline{A}$
not n2(L, B); → $L = \overline{B}$
and a1(D, A, B); $D = A \cdot B$
and a2(E, K, L); $E = \overline{A} \cdot \overline{B}$
nor o1(Y, D, E); $Y = \overline{(A \cdot B) + (\overline{A} \cdot \overline{B})}$
end module

↳ $Y = (\overline{A} + \overline{B}) \cdot (A + B)$

→ $A(\cancel{\overline{A}} + \overline{B}) + B(\overline{A} + \cancel{\overline{B}})$

$A\overline{B} + B\overline{A}$