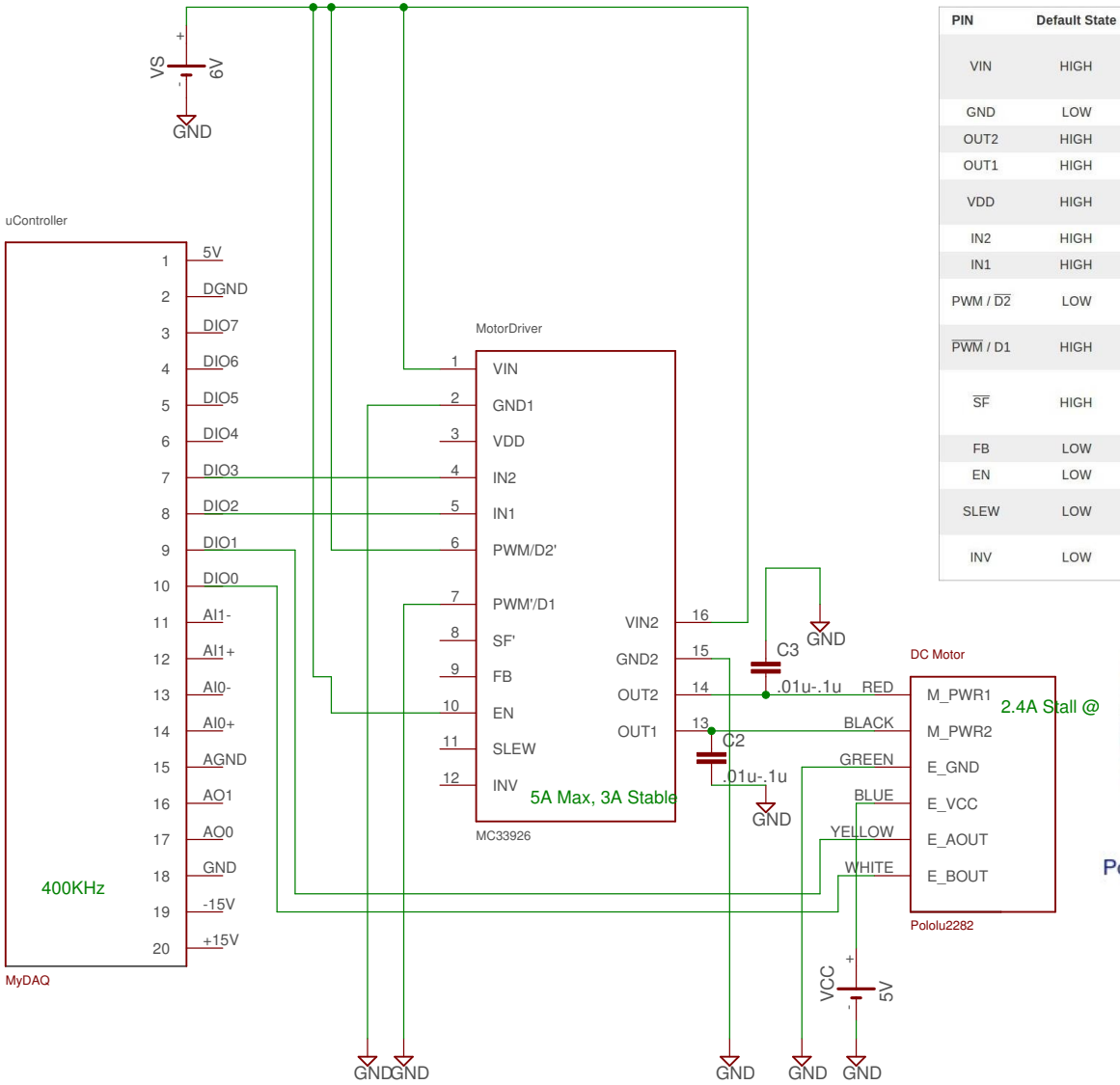
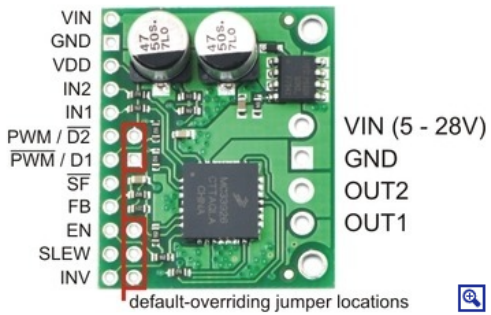


PIN	Default State	Description
VIN	HIGH	This is the main 5 – 28 V motor power supply connection, which should typically be made to the larger VIN pad. Operation from 5 – 8 V reduces maximum current output; the device is also protected for transients up to 40 V. The smaller VIN pad can be used to distribute the VIN node to the rest of the application circuit; for lower-current applications, the pin can also be used to power the motor driver and motor.
GND	LOW	Ground connection for logic and motor power supplies.
OUT2	HIGH	The motor output pin controlled by IN2.
OUT1	HIGH	The motor output pin controlled by IN1.
VDD	HIGH	3-5 V logic supply connection. This pin is used only for the $\overline{SF}$ pull-up and default-overriding jumpers; in the rare case where none of those features is used, VDD can be left disconnected.
IN2	HIGH	The logic input control of OUT2. PWM can be applied to this pin (typically done with both disable lines inactive).
IN1	HIGH	The logic input control of OUT1. PWM can be applied to this pin (typically done with both disable lines inactive).
PWM / $\overline{D2}$	LOW	Inverted disable input: when $\overline{D2}$ is low, OUT1 and OUT2 are set to high impedance. A $\overline{D2}$ PWM duty cycle of 70% gives a motor duty cycle of 70%. Typically, only one of the two disable pins is used, but the default is for both disable pins to be active.
$\overline{PWM}$ / D1	HIGH	Disable input: when D1 is high, OUT1 and OUT2 are set to high impedance. A D1 PWM duty cycle of 70% gives a motor duty cycle of 30%. Typically, only one of the two disable pins is used, but the default is for both disable pins to be active.
$\overline{SF}$	HIGH	Status flag output: an over-current (short circuit) or over-temperature event will cause $\overline{SF}$ to be latched LOW. If either of the disable pins (D1 or $\overline{D2}$) are disabling the outputs, $\overline{SF}$ will also be LOW. Otherwise, this pin is weakly pulled high. This allows the $\overline{SF}$ pins of multiple units to connected to a single input.
FB	LOW	The FB output provides analog current-sense feedback of approximately 525 mV per amp.
EN	LOW	Enable input: when EN is LOW, the chip is in a low-current sleep mode.
SLEW	LOW	Output slew rate selection input. A logical LOW results in a slow output rise time (1.5 µs – 6 µs). A logical HIGH selects a fast output rise time (0.2 µs – 1.45 µs). This pin should be set HIGH for high-frequency (over 10 kHz) PWM.
INV	LOW	A logical high value inverts the meaning of IN1 and IN2. This allows INV to function as a direction line if IN1 and IN2 are set to different values.

Color	Function
Red	motor power (connects to one motor terminal)
Black	motor power (connects to the other motor terminal)
Green	encoder GND
Blue	encoder Vcc (3.5 – 20 V)
Yellow	encoder A output
White	encoder B output

Signal Name	Reference	Direction	Description
AUDIO IN	—	Input	**Audio Input**—Left and right audio inputs on a stereo connector
AUDIO OUT	—	Output	**Audio Output**—Left and right audio outputs on a stereo connector
+15V/–15V	AGND	Output	+15 V/–15 V power supplies
AGND	—	—	**Analog Ground**—Reference terminal for AI, AO, +15 V, and –15 V
AO 0/AO 1	AGND	Output	Analog Output Channels 0 and 1
AI 0+/AI 0–; AI 1+/AI 1–	AGND	Input	Analog Input Channels 0 and 1
DIO <0..7>	DGND	Input or Output	**Digital I/O Signals**—General-purpose digital lines or counter signals
DGND	—	—	**Digital Ground**—Reference for the DIO lines and the +5 V supply
5V	DGND	Output	5 V power supply



Schematic Diagram