

# CS 529 Project 2 Report

## Jou-Chi Huang

### 1. L1 cache

For the first part, I implemented a unified 256 KB L1 cache, while in the second part, I utilized separate L1 instruction cache and L1 data cache. Interestingly, the unified cache displayed higher hit for both instructions and data compared to the separate caches configuration. This could be attributed to the unified cache's ability to optimize allocation more effectively. In my experiments, I observed that overall instruction hits were consistently higher than data hits. This suggests that the unified cache could allocate more space to instructions, if the data cache has additional space. Additionally, a unified cache helps mitigate conflicts, which occur when both caches attempt to store data in the same cache set. Consequently, the unified cache configuration achieved higher hit compared to the separate caches setup.

```
Beginning simulation!
src/sim/simulate.cc:199: info: Entering event queue @ 0. Starting simulation...
src/arch/arm/insts/pseudo.cc:172: warn:           instruction 'bt1' unimplemented
src/sim/mem_state.cc:448: info: Increasing stack size by one page.
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall set_robust_list(...)
src/sim/syscall_emul.cc:85: warn: ignoring syscall rseq(...)
    (further warnings will be suppressed)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)

5 5 5
Matrix #1 rows and columns:
Matrix #2 rows and columns:
84.178589 40.043911 78.526825 80.045563 91.253090
20.557585 34.187054 77.054733 28.499697 55.843029
48.262310 63.258221 37.113663 51.826691 95.270744
91.703316 63.935463 72.012398 15.018654 61.089920
2.613757 25.045790 14.585926 80.613495 16.511230
Enter elements of the second matrix:
40.693493 13.849254 11.772071 99.893524 22.607433
51.780308 84.072113 61.651344 30.307131 64.117676
52.904430 49.864716 97.304726 29.959164 77.364410
53.147751 77.221474 40.622635 89.261414 29.048159
35.893379 80.964729 91.983620 7.905773 94.983376
The product is :
17183.046875 22017.623047 22746.199219 19841.515625 21538.468750
10202.402344 13723.302734 16141.849609 8383.582031 14750.065430
13377.030273 19553.015625 18948.121094 13229.473633 18572.939453
13843.033203 16341.981445 18257.761719 15079.248047 17982.556641
7051.971191 10431.093750 7787.650391 8783.354492 6703.365723
Exiting @ tick 298831645750 because exiting with last active thread context
```

system.cpu.dcache.overallHits::total	112799	# number of overall hits (Count)
system.cpu.dcache.overallMisses::total	1745	# number of overall misses (Count)
system.cpu.icache.overallHits::total	321243	# number of overall hits (Count)
system.cpu.icache.overallMisses::total	1135	# number of overall misses (Count)

## 2. L1 instruction and data caches

For the second part, I implemented separate 256 KB instruction and 256 KB data caches, each with an associativity of 1. Besides observing a significantly lower hit compared to the unified cache configuration, I also obtained lower hits compared to the first test in part three. One possible explanation is that the matrix sizes used in this part were 3x4 and 4x3, whereas in the third experiment, larger matrix sizes of 5x5 and 5x5 were tested. The larger matrix sizes typically result in a higher likelihood of cache hits.

```
Beginning simulation with associativity 1!
src/sim/simulate.cc:199: info: Entering event queue @ 0. Starting simulation...
src/arch/arm/insts/pseudo.cc:172: warn:           instruction 'bt1' unimplemented
src/sim/mem_state.cc:448: info: Increasing stack size by one page.
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall set_robust_list(...)
src/sim/syscall_emul.cc:85: warn: ignoring syscall rseq(...)
    (further warnings will be suppressed)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)

[3 4 4 3
Matrix #1 rows and columns:
Matrix #2 rows and columns:
84.178589 40.043911 78.526825 80.045563
91.253090 20.557585 34.187054 77.054733
28.499697 55.843029 48.262310 63.258221
Enter elements of the second matrix:
37.113663 51.826691 95.270744
91.703316 63.935463 72.012398
15.018654 61.089920 2.613757
25.045790 14.585926 80.613495
The product is :
9980.506836 12887.660156 17561.417969
7715.274902 9256.103516 16475.160156
8487.906250 8918.415039 11962.189453
Exiting @ tick 1726609880000 because exiting with last active thread context
```

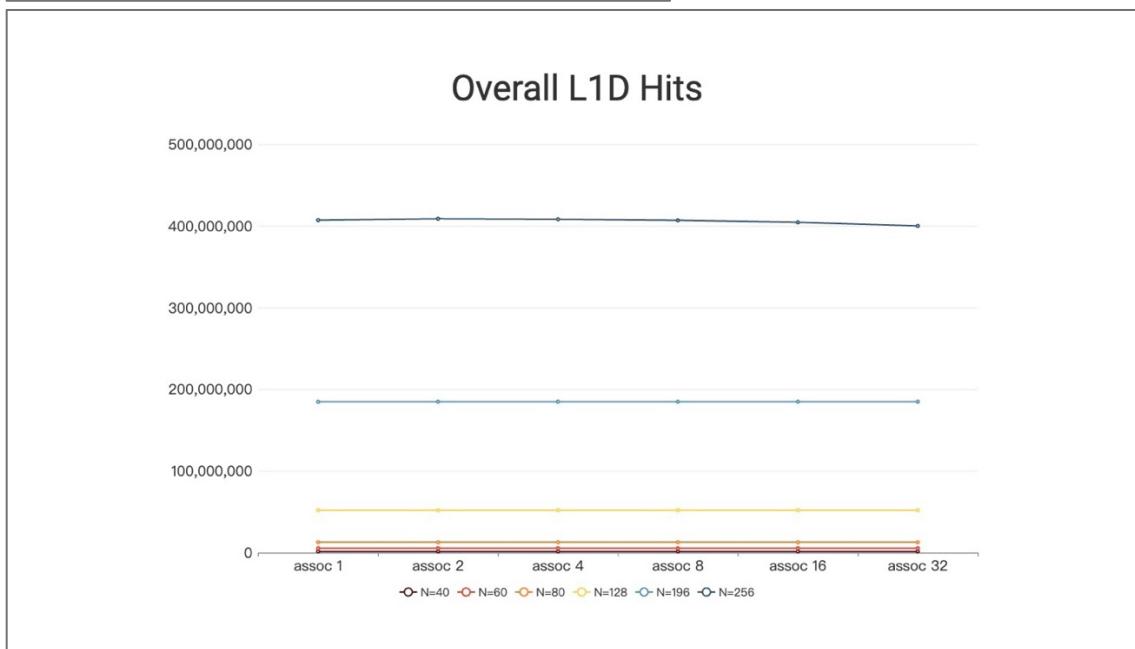
system.cpu.dcache.overallHits::total	66747	# number of overall hits (Count)
system.cpu.dcache.overallMisses::total	1767	# number of overall misses (Count)
system.cpu.icache.overallHits::total	188157	# number of overall hits (Count)
system.cpu.icache.overallMisses::total	1135	# number of overall misses (Count)

### 3. L1 instruction cache, L1 data cache

In this part, I continued to use the same settings as in part two but made changes to the associativity. During this experiment, I observed that regardless of the associativity level, the overall instruction hits remained constant in every case. This consistency can be attributed to the fact that the 256 KB size of the L1 instruction cache is sufficient for our workload, which involves generating random numbers and computing the product of two 5x5 matrices. Consequently, I generated a plot illustrating the data cache hits, which I believe warrants further investigation. Upon analysis, I found that as the matrix size increases, the data cache hits also increase. Additionally, while increasing the associativity led to an increase in data cache hits, the growth rate was slight, and it eventually plateaued at a certain value. This experiment provides valuable insights into determining the optimal associativity level according to the matrix size. Another interesting finding is that when the matrix size is 256x256, the hits start to drop as the associativity increases. This could be attributed to the cache being occupied with evicting old values and replacing them with new ones, leading to increased conflicts between cache lines.

- Plot

	A	B	C	D	E	F	G
1		N=40	N=60	N=80	N=128	N=196	N=256
2	assoc 1	1751238	5627286	13050381	52222713	185022627	407399866
3	assoc 2	1751271	5627318	13050412	52231198	185113130	409116535
4	assoc 4	1751276	5627324	13050419	52231235	185115037	408469976
5	assoc 8	1751276	5627324	13050419	52231239	185115012	407230110
6	assoc 16	1751276	5627324	13050419	52231238	185115012	404803597
7	assoc 32	1751276	5627324	13050419	52231240	185115012	400403636



- Associativity = 1

```

Running simulation with associativity: 1
Global frequency set at 100000000000 ticks per second
src/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (4096 Mbytes)
src/base/statistics.hn:279: warn: One of the stats is a legacy stat. Legacy stat is a stat that does not belong to any statistics::Group
eprecated.
system.remote_gdb: Listening for connections on port 7000
Beginning simulation!
src/sim/simulate.cc:199: info: Entering event queue @ 0. Starting simulation...
src/arch/arm/insts/pseudo.cc:172: warn: instruction 'bt1' unimplemented
src/sim/mem_state.cc:448: info: Increasing stack size by one page.
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall set_robust_list(...)
src/sim/syscall_emul.cc:85: warn: ignoring syscall rseq(...)
(further warnings will be suppressed)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
5 5 5
Matrix #1 rows and columns:
Matrix #2 rows and columns:
84.178589 40.043911 78.526825 80.045563 91.253090
20.557585 34.187054 77.054733 28.499697 55.843029
48.262310 63.258221 37.113663 51.826691 95.270744
91.703316 63.935463 72.012398 15.018654 61.089920
2.613757 25.045790 14.585926 80.613495 16.511230
Enter elements of the second matrix:
40.693493 13.849254 11.772071 99.893524 22.607433
51.780308 84.072113 61.651344 30.307131 64.117676
52.904430 49.864716 97.304726 29.959164 77.364410
53.147751 77.221474 40.622635 89.261414 29.048159
35.893379 80.964729 91.983620 7.905773 94.983376
The product is :
17183.046875 22017.623047 22746.199219 19841.515625 21538.468750
10202.402344 13723.302734 16141.849609 8383.582031 14750.065430
13377.030273 19553.015625 18948.121094 13229.473633 18572.939453
13843.033203 16341.981445 18257.761719 15079.248047 17982.556641
7051.971191 10431.093750 7787.658039 8783.354492 6703.365723
Exiting @ tick 65193127500 because exiting with last active thread context
simSeconds 0.651931 # Number of seconds simulated (Second)
system.cpu.dcache.overallHits::total 112766 # number of overall hits (Count)
system.cpu.dcache.overallMisses::total 1778 # number of overall misses (Count)
system.cpu.icache.overallHits::total 321243 # number of overall hits (Count)
system.cpu.icache.overallMisses::total 1135 # number of overall misses (Count)

```

- Associativity = 2

```

Running simulation with associativity: 2
Global frequency set at 100000000000 ticks per second
src/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (4096 Mbytes)
src/base/statistics.hn:279: warn: One of the stats is a legacy stat. Legacy stat is a stat that does not belong to any statistics::Group
eprecated.
system.remote_gdb: Listening for connections on port 7000
Beginning simulation!
src/sim/simulate.cc:199: info: Entering event queue @ 0. Starting simulation...
src/arch/arm/insts/pseudo.cc:172: warn: instruction 'bt1' unimplemented
src/sim/mem_state.cc:448: info: Increasing stack size by one page.
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall set_robust_list(...)
src/sim/syscall_emul.cc:85: warn: ignoring syscall rseq(...)
(further warnings will be suppressed)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
5 5 5
Matrix #1 rows and columns:
Matrix #2 rows and columns:
84.178589 40.043911 78.526825 80.045563 91.253090
20.557585 34.187054 77.054733 28.499697 55.843029
48.262310 63.258221 37.113663 51.826691 95.270744
91.703316 63.935463 72.012398 15.018654 61.089920
2.613757 25.045790 14.585926 80.613495 16.511230
Enter elements of the second matrix:
40.693493 13.849254 11.772071 99.893524 22.607433
51.780308 84.072113 61.651344 30.307131 64.117676
52.904430 49.864716 97.304726 29.959164 77.364410
53.147751 77.221474 40.622635 89.261414 29.048159
35.893379 80.964729 91.983620 7.905773 94.983376
The product is :
17183.046875 22017.623047 22746.199219 19841.515625 21538.468750
10202.402344 13723.302734 16141.849609 8383.582031 14750.065430
13377.030273 19553.015625 18948.121094 13229.473633 18572.939453
13843.033203 16341.981445 18257.761719 15079.248047 17982.556641
7051.971191 10431.093750 7787.658039 8783.354492 6703.365723
Exiting @ tick 325047627000 because exiting with last active thread context
simSeconds 0.325048 # Number of seconds simulated (Second)
system.cpu.dcache.overallHits::total 112799 # number of overall hits (Count)
system.cpu.dcache.overallMisses::total 1745 # number of overall misses (Count)
system.cpu.icache.overallHits::total 321243 # number of overall hits (Count)
system.cpu.icache.overallMisses::total 1135 # number of overall misses (Count)

```

- Associativity = 4

- Associativity = 8

```

Running simulation with associativity: 8
Global frequency set at 10000000000 ticks per second
src/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (4096 Mbytes)
src/base/statistics.hh:279: warn: One of the stats is a legacy stat. Legacy stat is a stat that does not belong to any statistics::Group
deprecated.
system.remote_gdb: Listening for connections on port 7000
Beginning simulation!
src/sim/simulate.cc:199: info: Entering event queue @ 0. Starting simulation...
src/arch/arm/insts/pseudo.cc:172: warn: instruction 'btii' unimplemented
src/sim/mem_state.cc:448: info: Increasing stack size by one page.
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall set_robust_list(...)
src/sim/syscall_emul.cc:85: warn: ignoring syscall rseq(...)
    (further warnings will be suppressed)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
5 5 5 5
Matrix #1 rows and columns:
Matrix #2 rows and columns:
84.178589 40.043911 78.526285 20.045563 91.253090
20.557585 34.187054 77.054733 28.499697 55.843029
48.262310 63.258221 37.113663 51.826691 95.270744
91.703316 63.935463 72.012398 15.018654 61.089920
2.613757 25.045798 14.585926 80.613495 16.511230
Enter elements of the second matrix:
40.693493 13.849254 11.772071 99.893524 22.607433
51.780308 84.072113 61.651344 30.307131 64.117676
52.904430 49.864716 97.384726 29.959164 77.364410
53.147751 77.221474 40.622635 89.261414 29.048159
35.893379 88.964729 91.983620 7.905773 94.983376
The product is :
17183.044675 22017.623047 22746.199219 19841.515625 21538.468750
10202.402344 13723.302734 16141.849609 8383.582031 14750.065430
13377.030273 19553.015625 18948.121094 13229.473633 18572.939453
13843.033203 16341.981445 18257.761719 15079.248047 17982.556641
7051.971191 10431.893750 7787.658391 8783.354492 6703.365723
Exiting @ tick 225847787500 because exiting with last active thread context
simSeconds                                0.225848          # Number of seconds simulated (Second)
system.cpu.dcache.overallHits::total        112884          # number of overall hits (Count)
system.cpu.dcache.overallMisses::total       1740           # number of overall misses (Count)
system.cpu.icache.overallHits::total         321243          # number of overall hits (Count)
system.cpu.icache.overallMisses::total       1135           # number of overall misses (Count)

```

- Associativity = 16

```

Running simulation with associativity: 16
Global frequency set at 100000000000 ticks per second
src/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (4096 Mbytes)
src/base/statistics.hh:279: warn: One of the stats is a legacy stat. Legacy stat is a stat that does not belong to any statistics::Group.
deprecated.
system.remote_gdb: Listening for connections on port 7000
Beginning simulation!
src/sim/simulate.cc:199: info: Entering event queue @ 0. Starting simulation...
src/arch/arm/insts/pseudo.cc:172: warn: instruction 'bt1' unimplemented
src/sim/mem_state.cc:448: info: Increasing stack size by one page.
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall set_robust_list(...)
src/sim/syscall_emul.cc:85: warn: ignoring syscall rseq(...)
(further warnings will be suppressed)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
5 5 5
Matrix #1 rows and columns:
Matrix #2 rows and columns:
84.178589 40.043911 78.526825 80.045563 91.253090
20.557585 34.187054 77.054733 28.499697 55.843029
48.262310 63.258221 37.113663 51.826691 95.270744
91.703316 63.935463 72.012398 15.018654 61.089920
2.613757 25.045790 14.585926 80.613495 16.511230
Enter elements of the second matrix:
40.693493 13.849254 11.772071 99.893524 22.607433
51.780308 84.072113 61.651344 30.307131 64.117676
52.984430 49.864716 97.304726 29.959164 77.364410
53.147751 77.221474 40.622635 89.261414 29.048159
35.893379 80.964729 91.983620 7.905773 94.983376
The product is :
17183.046875 22017.623047 22746.199219 19841.515625 21538.468750
10202.402344 13723.302734 16141.849689 8383.582031 14750.065430
13377.030273 19553.015625 18948.121094 13229.473633 18572.939453
13843.033203 16341.981445 18257.761719 15079.248047 17982.556641
7051.971191 10431.093750 7787.650391 8783.354492 6703.365723
Exiting @ tick 197773907000 because exiting with last active thread context
simSeconds 0.197774 # Number of seconds simulated (Second)
system.cpu.dcache.overallHits::total 112804 # number of overall hits (Count)
system.cpu.dcache.overallMisses::total 1740 # number of overall misses (Count)
system.cpu.icache.overallHits::total 321243 # number of overall hits (Count)
system.cpu.icache.overallMisses::total 1135 # number of overall misses (Count)

```

- Associativity = 32

```

Running simulation with associativity: 32
Global frequency set at 100000000000 ticks per second
src/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (4096 Mbytes)
src/base/statistics.hh:279: warn: One of the stats is a legacy stat. Legacy stat is a stat that does not belong to any statistics::Group.
deprecated.
system.remote_gdb: Listening for connections on port 7000
Beginning simulation!
src/sim/simulate.cc:199: info: Entering event queue @ 0. Starting simulation...
src/arch/arm/insts/pseudo.cc:172: warn: instruction 'bt1' unimplemented
src/sim/mem_state.cc:448: info: Increasing stack size by one page.
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall set_robust_list(...)
src/sim/syscall_emul.cc:85: warn: ignoring syscall rseq(...)
(further warnings will be suppressed)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
5 5 5
Matrix #1 rows and columns:
Matrix #2 rows and columns:
84.178589 40.043911 78.526825 80.045563 91.253090
20.557585 34.187054 77.054733 28.499697 55.843029
48.262310 63.258221 37.113663 51.826691 95.270744
91.703316 63.935463 72.012398 15.018654 61.089920
2.613757 25.045790 14.585926 80.613495 16.511230
Enter elements of the second matrix:
40.693493 13.849254 11.772071 99.893524 22.607433
51.780308 84.072113 61.651344 30.307131 64.117676
52.984430 49.864716 97.304726 29.959164 77.364410
53.147751 77.221474 40.622635 89.261414 29.048159
35.893379 80.964729 91.983620 7.905773 94.983376
The product is :
17183.046875 22017.623047 22746.199219 19841.515625 21538.468750
10202.402344 13723.302734 16141.849689 8383.582031 14750.065430
13377.030273 19553.015625 18948.121094 13229.473633 18572.939453
13843.033203 16341.981445 18257.761719 15079.248047 17982.556641
7051.971191 10431.093750 7787.650391 8783.354492 6703.365723
Exiting @ tick 430147388250 because exiting with last active thread context
simSeconds 0.438147 # Number of seconds simulated (Second)
system.cpu.dcache.overallHits::total 112804 # number of overall hits (Count)
system.cpu.dcache.overallMisses::total 1740 # number of overall misses (Count)
system.cpu.icache.overallHits::total 321243 # number of overall hits (Count)
system.cpu.icache.overallMisses::total 1135 # number of overall misses (Count)

```

#### 4. $x$ KB L1-I cache, $y$ KB L1-D cache, $z$ MB L2 cache

In this part, I changed the size of the L1 instruction cache, L1 data cache, and L2 cache. All five tests involved generating the product of two 64x64 random numbers matrices. I observed that when setting the L1 instruction cache size from 8 KB to 256 KB, I obtained similar hit numbers. Therefore, I assume that 8 KB or 16 KB may be sufficient for this task. A similar trend was observed with the L1 data cache, where 8 KB or 16 KB may also be sufficient. Regarding L2 cache hits, I found that its size is mostly determined by the size of L1. If L1 is large enough, then L2 hits decrease. Otherwise, L2 hits can experience significant growth.

\*i.e: 64, 128, 2  $\rightarrow$   $x = 64$  KB,  $y = 128$  KB,  $z = 2$  MB

8, 8, 2  $\rightarrow$   $x = 8$  KB,  $y = 8$  KB,  $z = 2$  MB

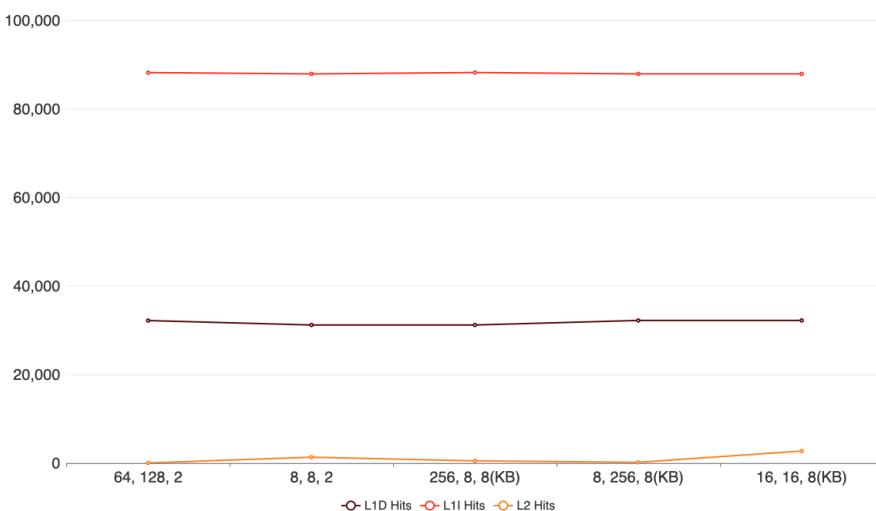
256, 8, 8  $\rightarrow$   $x = 256$  KB,  $y = 8$  KB,  $z = 8$  KB

8, 256, 8  $\rightarrow$   $x = 8$  KB,  $y = 256$  KB,  $z = 8$  KB

16, 16, 8  $\rightarrow$   $x = 16$  KB,  $y = 16$  KB,  $z = 8$  KB

	A	B	C	D
1		L1D Hits	L1I Hits	L2 Hits
2	64, 128, 2	32213	88229	50
3	8, 8, 2	31211	87938	1344
4	256, 8, 8(KB)	31211	88244	516
5	8, 256, 8(KB)	32240	87938	187
6	16, 16, 8(KB)	32240	87938	2741

Overall hits changing  $x, y, z$



- $x = 64, y = 128, z = 2$

```

Running simulation with associativity: 2 4
Global frequency set at 100000000000 ticks per second
src/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range
src/base/statistics.hh:279: warn: One of the stats is a legacy stat. Legacy stat is a stat that does not belong to
Legacy stat is deprecated.
system.remote_gdb: Listening for connections on port 7000
Beginning simulation!
src/sim/simulate.cc:199: info: Entering event queue @ 0. Starting simulation...
src/arch/arm/insts/pseudo.cc:172: warn: instruction 'bt1' unimplemented
src/sim/mem_state.cc:448: info: Increasing stack size by one page.
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall set_robust_list(...)
src/sim/syscall_emul.cc:85: warn: ignoring syscall rseq(...)
(further warnings will be suppressed)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)

[64 64 64 64

Matrix #1 rows and columns:
Matrix #2 rows and columns:
Enter elements of the first matrix:
Enter elements of the second matrix:
The product is :
Exiting @ tick 320206075500 because exiting with last active thread context

```

system.cpu.dcache.overallHits::total	32213	# number of overall hits (Count)
system.cpu.dcache.overallMisses::total	1740	# number of overall misses (Count)
system.cpu.icache.overallHits::total	88229	# number of overall hits (Count)
system.cpu.icache.overallMisses::total	990	# number of overall misses (Count)
system.l2cache.overallHits::total	50	# number of overall hits (Count)
system.l2cache.overallMisses::total	2614	# number of overall misses (Count)

- $x = 8, y = 8, z = 2$

```

Running simulation with associativity: 2 4
Global frequency set at 100000000000 ticks per second
src/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned to
src/base/statistics.hh:279: warn: One of the stats is a legacy stat. Legacy stat is a stat that does not belong to
Legacy stat is deprecated.
system.remote_gdb: Listening for connections on port 7000
Beginning simulation!
src/sim/simulate.cc:199: info: Entering event queue @ 0. Starting simulation...
src/arch/arm/insts/pseudo.cc:172: warn: instruction 'bt1' unimplemented
src/sim/mem_state.cc:448: info: Increasing stack size by one page.
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall set_robust_list(...)
src/sim/syscall_emul.cc:85: warn: ignoring syscall rseq(...)
(further warnings will be suppressed)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)

[64 64 64 64

Matrix #1 rows and columns:
Matrix #2 rows and columns:
Enter elements of the first matrix:
Enter elements of the second matrix:
The product is :
Exiting @ tick 281830407250 because exiting with last active thread context

```

system.cpu.dcache.overallHits::total	31211	# number of overall hits (Count)
system.cpu.dcache.overallMisses::total	2742	# number of overall misses (Count)
system.cpu.icache.overallHits::total	87938	# number of overall hits (Count)
system.cpu.icache.overallMisses::total	1281	# number of overall misses (Count)

system.l2cache.overallHits::total	1344	# number of overall hits (Count)
system.l2cache.overallMisses::total	2614	# number of overall misses (Count)

- $x = 256, y = 8, z = 8(\text{KB})$

```
Running simulation with associativity: 2 4
Global frequency set at 100000000000 ticks per second
src/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range
src/base/statistics.hh:279: warn: One of the stats is a legacy stat. Legacy stat is a stat that does not belong to a core.
Legacy stat is deprecated.
system.remote_gdb: Listening for connections on port 7000
Beginning simulation!
src/sim/simulate.cc:199: info: Entering event queue @ 0. Starting simulation...
src/arch/arm/insts/pseudo.cc:172: warn: instruction 'bt' unimplemented
src/sim/mem_state.cc:448: info: Increasing stack size by one page.
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall set_robust_list(...)
src/sim/syscall_emul.cc:85: warn: ignoring syscall rseq(...)
(further warnings will be suppressed)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
[64 64 64 64
Matrix #1 rows and columns:
Matrix #2 rows and columns:
Enter elements of the first matrix:
Enter elements of the second matrix:
The product is :
Exiting @ tick 694566558000 because exiting with last active thread context
```

system.cpu.dcache.overallHits::total	31211	# number of overall hits (Count)
system.cpu.dcache.overallMisses::total	2742	# number of overall misses (Count)
system.cpu.icache.overallHits::total	88244	# number of overall hits (Count)
system.cpu.icache.overallMisses::total	975	# number of overall misses (Count)
system.l2cache.overallHits::total	516	# number of overall hits (Count)
system.l2cache.overallMisses::total	3136	# number of overall misses (Count)

- $x = 8, y = 256, z = 8(\text{kB})$

```
Running simulation with associativity: 2 4
Global frequency set at 100000000000 ticks per second
src/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range
src/base/statistics.hh:279: warn: One of the stats is a legacy stat. Legacy stat is a stat that does not belong to a core.
Legacy stat is deprecated.
system.remote_gdb: Listening for connections on port 7000
Beginning simulation!
src/sim/simulate.cc:199: info: Entering event queue @ 0. Starting simulation...
src/arch/arm/insts/pseudo.cc:172: warn: instruction 'bt' unimplemented
src/sim/mem_state.cc:448: info: Increasing stack size by one page.
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall set_robust_list(...)
src/sim/syscall_emul.cc:85: warn: ignoring syscall rseq(...)
(further warnings will be suppressed)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
[64 64 64 64
Matrix #1 rows and columns:
Matrix #2 rows and columns:
Enter elements of the first matrix:
Enter elements of the second matrix:
The product is :
Exiting @ tick 271900100750 because exiting with last active thread context
```

system.cpu.dcache.overallHits::total	32240	# number of overall hits (Count)
--------------------------------------	-------	----------------------------------

system.cpu.dcache.overallMisses::total	1713	# number of overall misses (Count)
system.cpu.icache.overallHits::total	87938	# number of overall hits (Count)
system.cpu.icache.overallMisses::total	1281	# number of overall misses (Count)
system.l2cache.overallHits::total	187	# number of overall hits (Count)
system.l2cache.overallMisses::total	2741	# number of overall misses (Count)

- $x = 16, y = 16, z = 8(\text{KB})$

```
Running simulation with associativity: 2 4
Global frequency set at 100000000000 ticks per second
src/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbyte
src/base/statistics.hh:279: warn: One of the stats is a legacy stat. Legacy stat is a stat that does not belong to any stati
Legacy stat is deprecated.
system.remote_gdb: Listening for connections on port 7000
Beginning simulation!
src/sim/simulate.cc:199: info: Entering event queue @ 0. Starting simulation...
src/arch/arm/insts/pseudo.cc:172: warn: instruction 'bt' unimplemented
src/sim/mem_state.cc:448: info: Increasing stack size by one page.
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall set_robust_list(...)
src/sim/syscall_emul.cc:85: warn: ignoring syscall rseq(...)
(further warnings will be suppressed)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
src/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
64 64 64
Matrix #1 rows and columns:
Matrix #2 rows and columns:
Enter elements of the first matrix:
Enter elements of the second matrix:
The product is :
Exiting @ tick 342423293000 because exiting with last active thread context
```

system.cpu.dcache.overallHits::total	32240	# number of overall hits (Count)
system.cpu.dcache.overallMisses::total	1713	# number of overall misses (Count)
system.cpu.icache.overallHits::total	87938	# number of overall hits (Count)
system.cpu.icache.overallMisses::total	1281	# number of overall misses (Count)
system.l2cache.overallHits::total	187	# number of overall hits (Count)
system.l2cache.overallMisses::total	2741	# number of overall misses (Count)