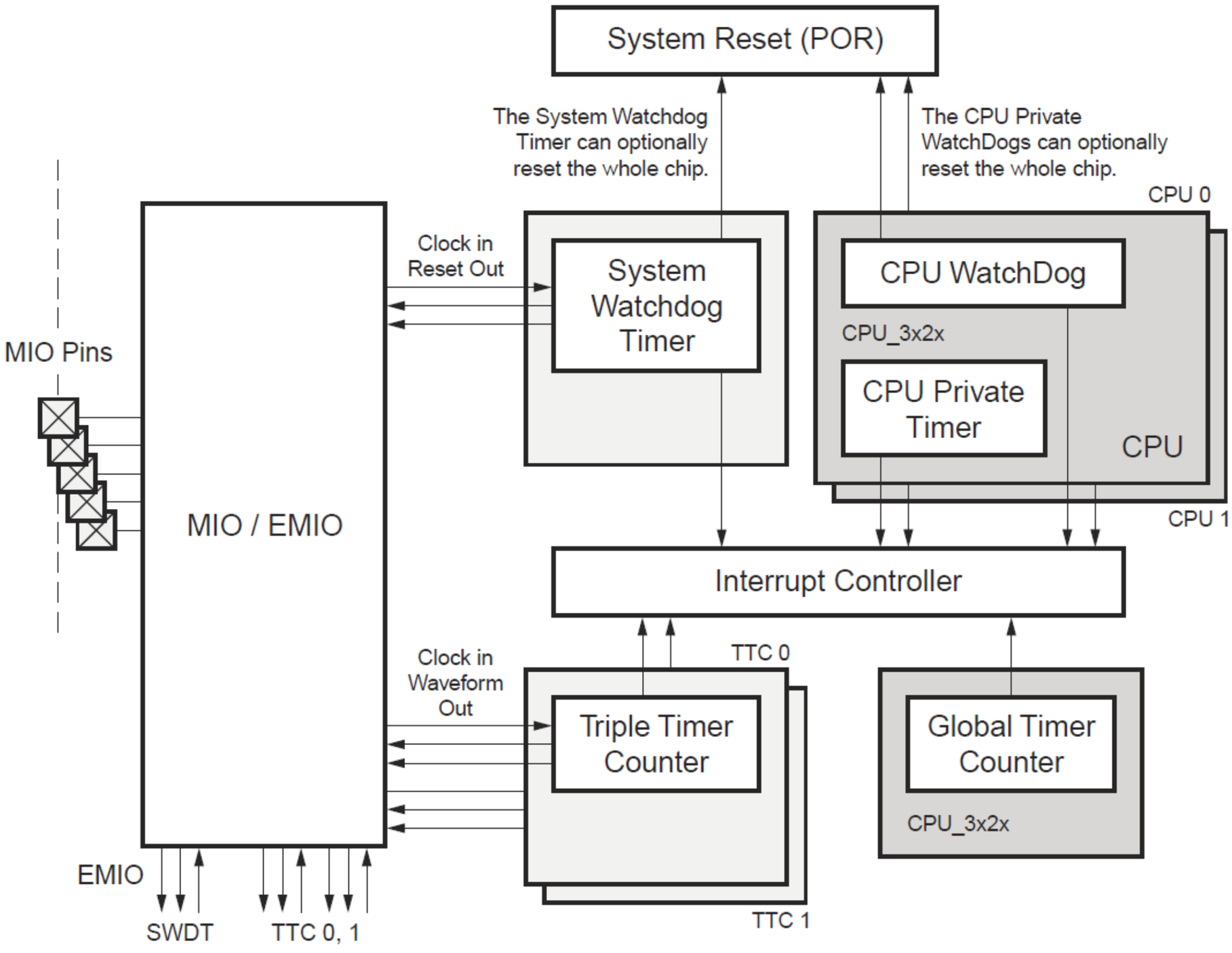
嵌入式体系结构基于ZYNQ
第五讲

Zynq定时器

- Zynq定时器概述
- 定时器硬件
- 定时器编程模式

ZYNQ-SoC 定时器概述



ZYNQ-SoC

定时器概述

- 私有定时器和看门狗频率固定位主频一半
- 系统看门狗和定时器频率可根据需要调整

ZYNQ-SoC 私有定时器

- 32位定时器到零产生中断
- 8位步距寄存器以控制中断间隔
- 可配置单次和自动重装模式
- 可配置计数初值

私有定时器

- 计数频率为CPU时钟的1/2
- 产生PPI中断至GIC
- 复位信号送至PS复位系统

ZYNQ-SoC 私有定时器

Function	Name	Overview
CPU Private Timers		
Reload and current values	Timer Load Timer Counter	Values to be reloaded into the decrementer. Current value of the decrementer.
Control and interrupt	Timer Control Timer Interrupt	Enable, auto reload, IRQ, prescaler, interrupt status.
CPU Private Watchdogs (AWDT 0 and 1)		
Reload and current values	Watchdog Load Watchdog Counter	Values to be reloaded into the decrementer. Current value of the decrementer.
Control and interrupt	Watchdog Control Watchdog Interrupt	Enable, Auto reload, IRQ, prescaler, interrupt status. (this register cannot disable watchdog)
Reset status	Watchdog Reset Status	Reset status as a result of watchdog reaching 0. Cleared with POR only, so SW can tell if the reset was caused by watchdog.
Disable	Watchdog Disable	Disable watchdog through a sequence of writes of two specific words.

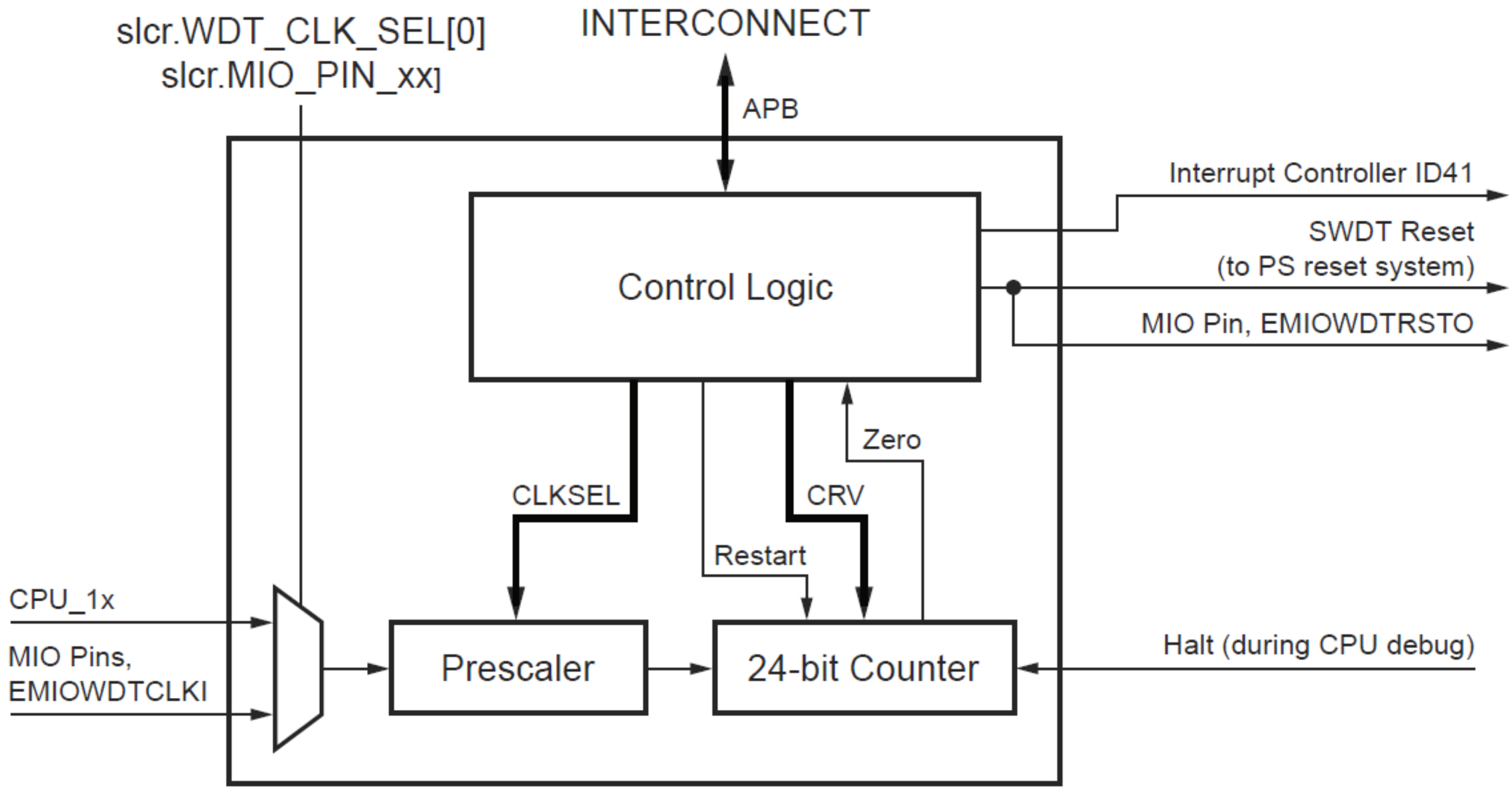
全局定时器

- 64位自增定时器
- 和私有定时器有相同的地址空间
- 复位时只能在安全状态下访问
- 所有CPU均可以访问并通过比较产生中断

全局定时器

Function	Name	Overview
Global Timer (GTC)		
Current values	Global Timer Counter	Current value of the incrementer
Control and interrupt	Global Timer Control Global Interrupt	Enable timer, enable comparator, IRQ, auto-increment, interrupt status
Comparator	Comparator Value Comparator Increment	Current value of the comparator Increment value for the comparator
	Global Timer Disable	Disable watchdog through a sequence of writes of two specific words

ZYNQ-SoC 系统看门狗



系统看门狗

- 24位计数器
- 时钟输入可选
  - PS内部总线时钟
  - PL内部总线时钟
  - MIO外部时钟
- 超时输出方式灵活
  - PS部分系统中断
  - 系统复位
- 超时周期可编程设定
  - 330 μs to 687.2s at 100 MHz
- 输出脉冲宽度可编程设定
  - 4, 8, 16, or 32 clock cycles (CPU_1x clock)

ZYNQ-SoC 系统看门狗

Function	Name	Overview
Clock select	slcr.WDT_CLK_SEL	Selects between the CPU_1x and external clock source (MIO/EMIO).
MIO routing	slcr.MIO_PIN_xx	Routes the SWDT clock input through the MIO multiplexer or EMIO if no MIO routing.
Reset reason	slcr.REBOOT_STATUS	The [SWDT_RST] bit gets set when the SWDT generates a system reset.
Zero mode	swdt.MODE	Enable SWDT, enable interrupt and reset outputs on timeout, set output pulse lengths.
Reload values	swdt.CONTROL	Set the reload values for prescaler and 24-bit counter on timeout.
Restart	swdt.RESTART	Cause the prescaler and the 24-bit counter to reload and restart.
Status	swdt.STATUS	Indicates watchdog reaching zero.

系统看门狗

- 选择输入时钟源
- 设定中断间隔
- 启动看门狗
  - 允许计数器
  - 允许输出脉冲
  - 设定输出脉冲宽度
- 需要重新设定必须停止看门狗并重复前面三步

系统看门狗

- 输入时钟源判定

  if slcr.WDT_CLK_SEL[0] is 0, use CPU_1X
  else if slcr.MIO_PIN_14[7:0] is 01100000, use MIO pin 14
  else if slcr.MIO_PIN_26[7:0] is 01100000, use MIO pin 26
  else if slcr.MIO_PIN_38[7:0] is 01100000, use MIO pin 38
  else if slcr.MIO_PIN_50[7:0] is 01100000, use MIO pin 50
  else if slcr.MIO_PIN_52[7:0] is 01100000, use MIO pin 52
  else use EMIOWDTCLKI

系统看门狗

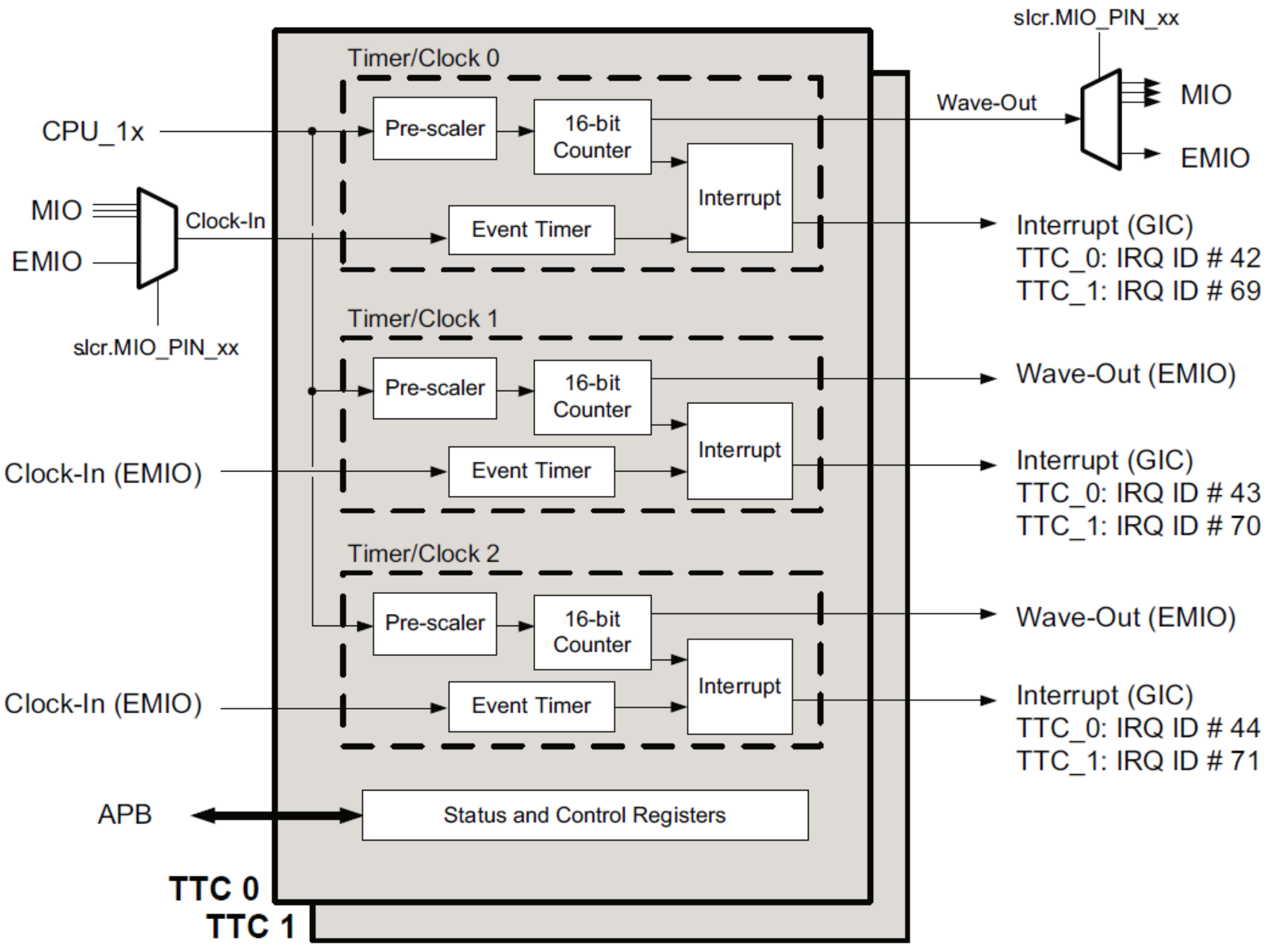
- 复位信号输出

  if slcr.WDT_CLK_sel[0] is 0, no output (to PS reset system only)
  else if slcr.MIO_PIN_15[7:0] is 01100000, use MIO pin 15
  else if slcr.MIO_PIN_27[7:0] is 01100000, use MIO pin 27
  else if slcr.MIO_PIN_39[7:0] is 01100000, use MIO pin 39
  else if slcr.MIO_PIN_51[7:0] is 01100000, use MIO pin 51
  else if slcr.MIO_PIN_53[7:0] is 01100000, use MIO pin 53
  else use EMIOWDTRSTO

系统看门狗

SWDT Signal	I/O	MIO Pins	EMIO Signals	Controller Default Input Value
Clock in	I	14, 26, 38, 50, 52	EMIOWDTCLKI	0
Reset out	O	15, 27, 39, 51, 53	EMIOWDTRSTO	~

ZYNQ-SoC 系统定时器TTC



系统定时器TTC

- 三路独立步距寄存器和计数器
- 可选时钟输入源
  - PS系统时钟
  - PL总线时钟
  - 外部输入时钟
- 每路计数器独立产生中断
- 可中断于溢出、固定间隔和预设数值
- 可在MIO或者PL引脚产生PWM

系统定时器TTC

- 间隔模式
  - 可递增或递减
  - 产生固定间隔
- 溢出模式
  - 可递增或递减
  - 计数器溢出产生中断
- 外部事件计数器模式
  - 复位清零、于计数脉冲时加一
  - **E_En bit**
  - **E_Lo bit**
  - **E_Ov bit**

ZYNQ-SoC 系统定时器TTC

Function	Name	Overview
Clock control	Clock Control register	Controls prescaler, selects clock input, edge
	Counter Control register	Enables counter, sets mode of operation, sets up/down counting, enables matching, enables waveform output
Status	Counter Value register	Returns current counter value
Counter Control	Interval register	Sets interval value
	Match register 1 Match register 2 Match register 3	Sets match values, total 3
Interrupt	Interrupt register	Shows current interrupt status
	Interrupt Enable register	Enable interrupts
Event	Event Control Timer register	Enable event timer, stop timer, sets phrase
	Event register	Shows width of external pulse

系统定时器TTC

- 选择输入时钟源
- 设定时间间隔
- 设定匹配数值
- 允许中断
- 允许/禁止波形输出

系统定时器TTC

- TTC0时钟输入选择
  if slcr.MIO_PIN_19[6:0] is 1100000, use MIO pin 19
  else if slcr.MIO_PIN_31[6:0] is 1100000, use MIO pin 31
  else if slcr.MIO_PIN_43[6:0] is 1100000, use MIO pin 43
  else use EMIOTTC0CLKI0

- TTC1时钟输入选择
  if slcr.MIO_PIN_17[6:0] is 1100000, use MIO pin 17
  else if slcr.MIO_PIN_29[6:0] is 1100000, use MIO pin 29
  else if slcr.MIO_PIN_41[6:0] is 1100000, use MIO pin 41
  else use EMIOTTC1CLKI0

ZYNQ-SoC 系统定时器TTC

TTC	Timer Signal	I/O	MIO Pins	EMIO Signals	Controller Default Input Value
TTC0	Counter/Timer 0 clock in	I	19, 31, 43	EMIOTTC0CLKI0	0
	Counter/Timer 0 wave out	O	18, 30, 42	EMIOTTC0WAVEO0	~
	Counter/Timer 1 clock in	I	N/A	EMIOTTC0CLKI1	0
	Counter/Timer 1 wave out	O	N/A	EMIOTTC0WAVEO1	~
	Counter/Timer 2 clock in	I	N/A	EMIOTTC0CLKI2	0
	Counter/Timer 2 wave out	O	N/A	EMIOTTC0WAVEO2	~
TTC1	Counter/Timer 0 clock in	I	17, 29, 41	EMIOTTC1CLKI0	0
	Counter/Timer 0 wave out	O	16, 28, 40	EMIOTTC1WAVEO0	~
	Counter/Timer 1 clock in	I	N/A	EMIOTTC1CLKI1	0
	Counter/Timer 1 wave out	O	N/A	EMIOTTC1WAVEO1	~
	Counter/Timer 2 clock in	I	N/A	EMIOTTC1CLKI2	0
	Counter/Timer 2 wave out	O	N/A	EMIOTTC1WAVEO2	~

思考题