

嵌入式体系结构基于ZYNQ

第三讲

- PS GPIO和PL GPIO
- GPIO输出
- GPIO输入

- Zynq上PS的MIO数量54
- EMIO接口可将PS的GPIO连接到PL
- 每一位可单独指定方向和产生中断

ZYNQ-SoC

PS GPIO

Re-customize IP

ZYNQ7 Processing System (5.5)

Documentation

Presets

IP Location

Import XPS Settings

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Zynq Block Design

PS-PL Configuration

Peripheral I/O Pins

MIO Configuration

Clock Configuration

DDR Configuration

SMC Timing Calculation

Interrupts

MIO Configuration

Summary Report

Bank 0 I/O Voltage LVC MOS 3.3V

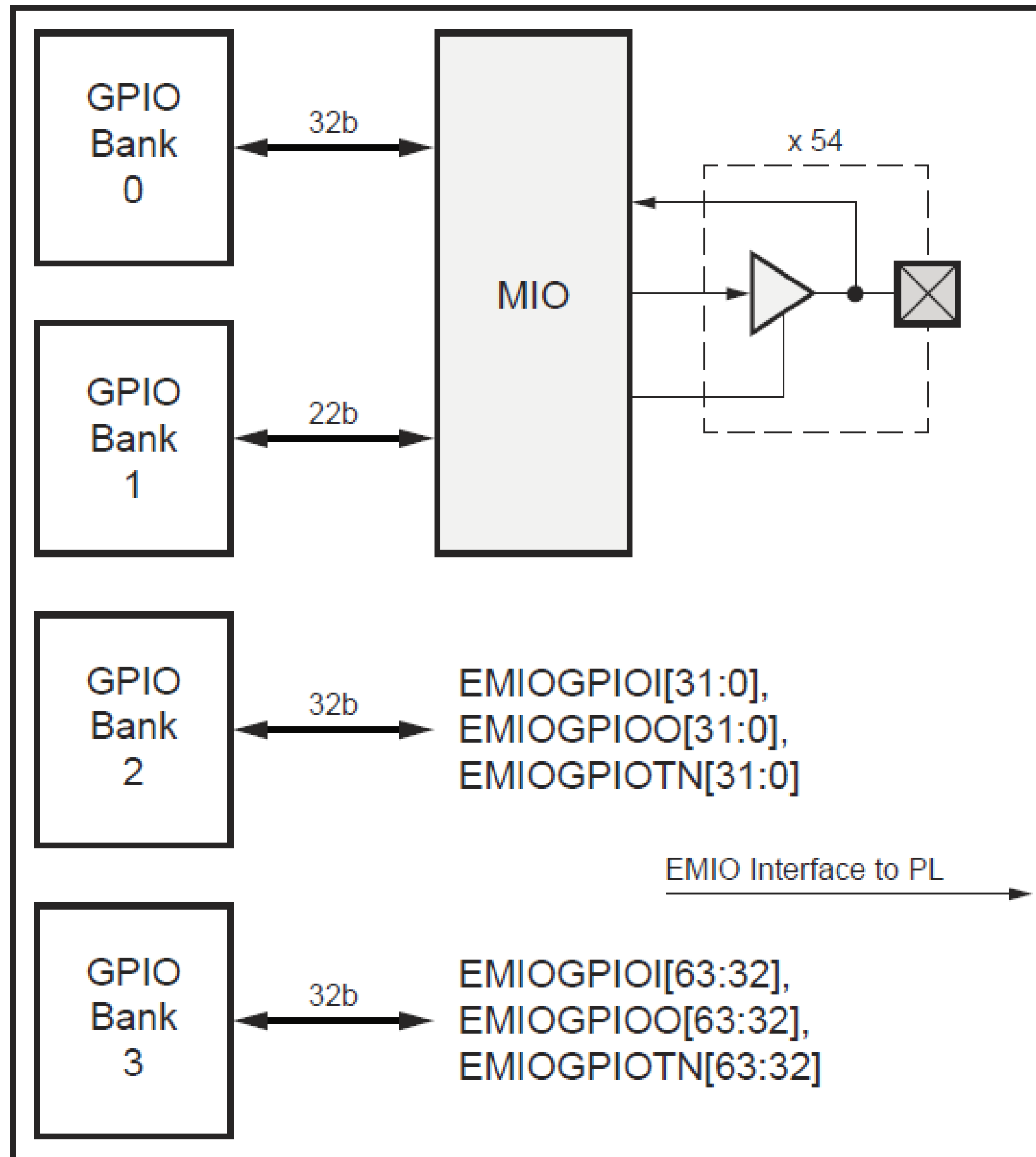
Bank 1 I/O Voltage LVC MOS 1.8V

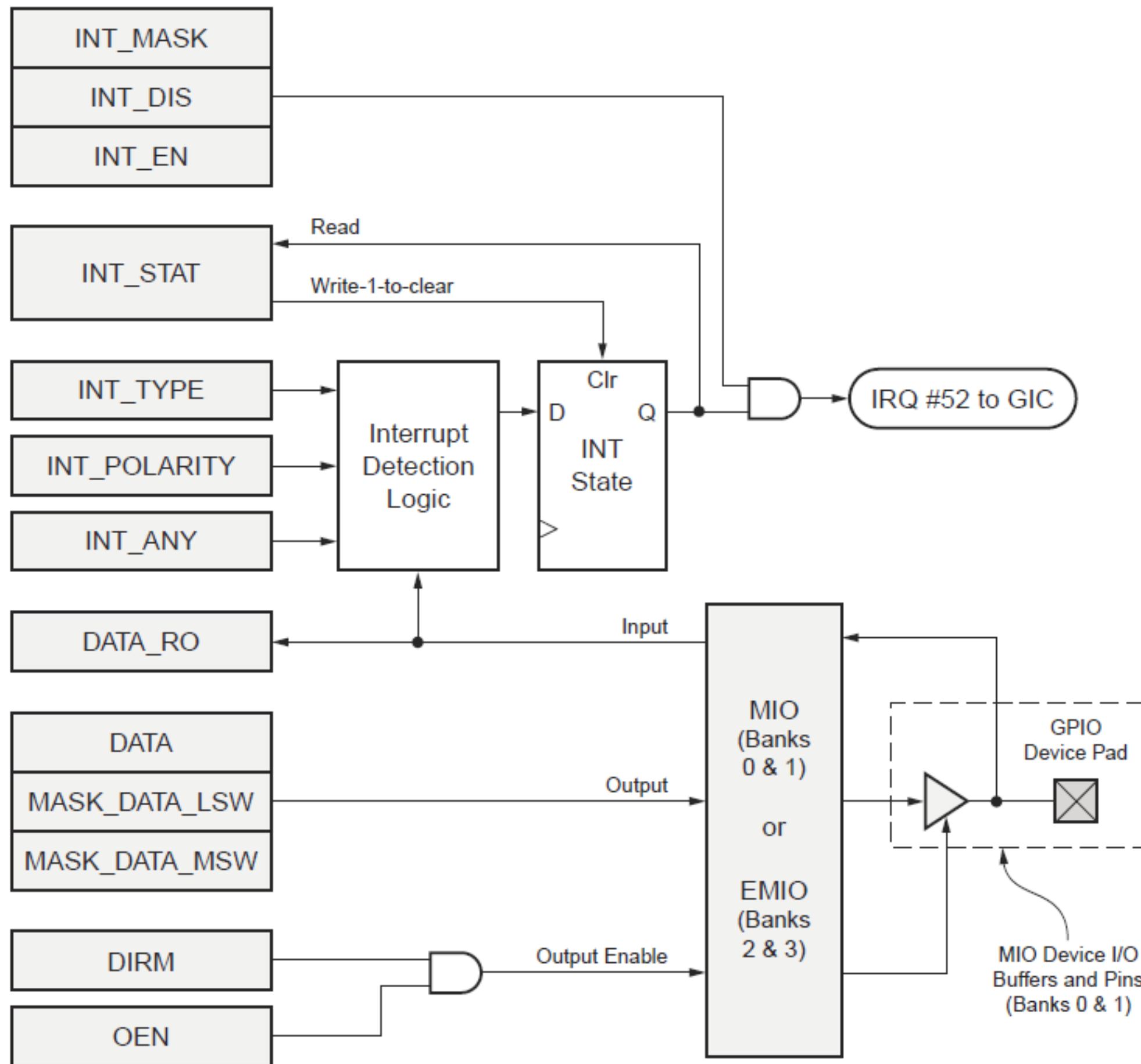
Search: Q-

Peripheral	IO	Signal	IO Type	Speed	Pullup
GPIO	MIO 42	gpio[42]	LVC MOS 1.8V	slow	enabled
GPIO	MIO 43	gpio[43]	LVC MOS 1.8V	slow	enabled
GPIO	MIO 44	gpio[44]	LVC MOS 1.8V	slow	enabled
GPIO	MIO 45	gpio[45]	LVC MOS 1.8V	slow	enabled
GPIO	MIO 46	gpio[46]	LVC MOS 1.8V	slow	enabled
GPIO	MIO 47	gpio[47]	LVC MOS 1.8V	slow	enabled
GPIO	MIO 48	gpio[48]	LVC MOS 1.8V	slow	enabled
GPIO	MIO 49	gpio[49]	LVC MOS 1.8V	slow	enabled
GPIO	MIO 52	gpio[52]	LVC MOS 1.8V	slow	enabled
GPIO	MIO 53	gpio[53]	LVC MOS 1.8V	slow	enabled
<input checked="" type="checkbox"/> EMIO GPIO (Width)	24				
> <input type="checkbox"/> ENET Reset					
> <input checked="" type="checkbox"/> USB Reset					

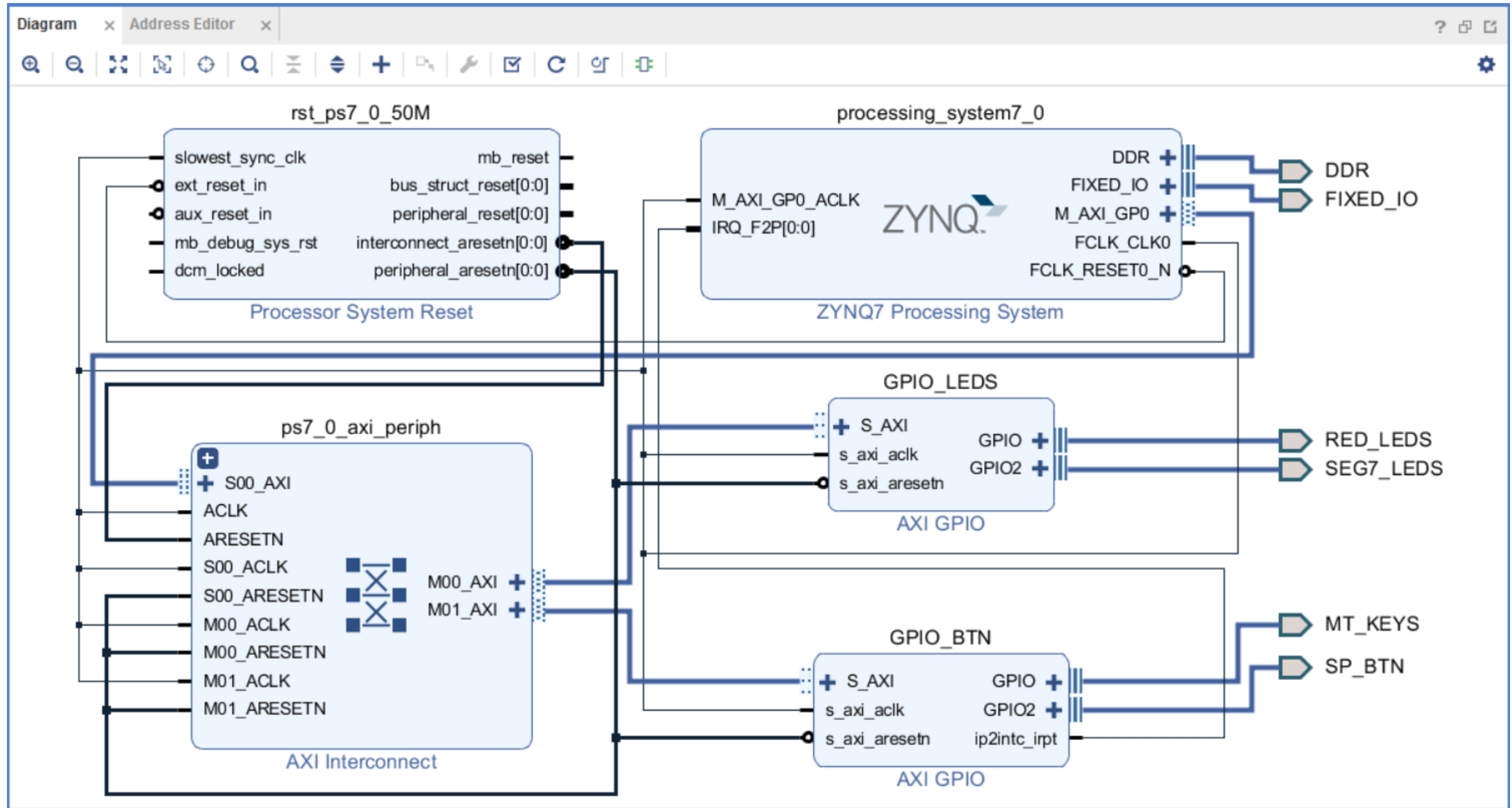
OK

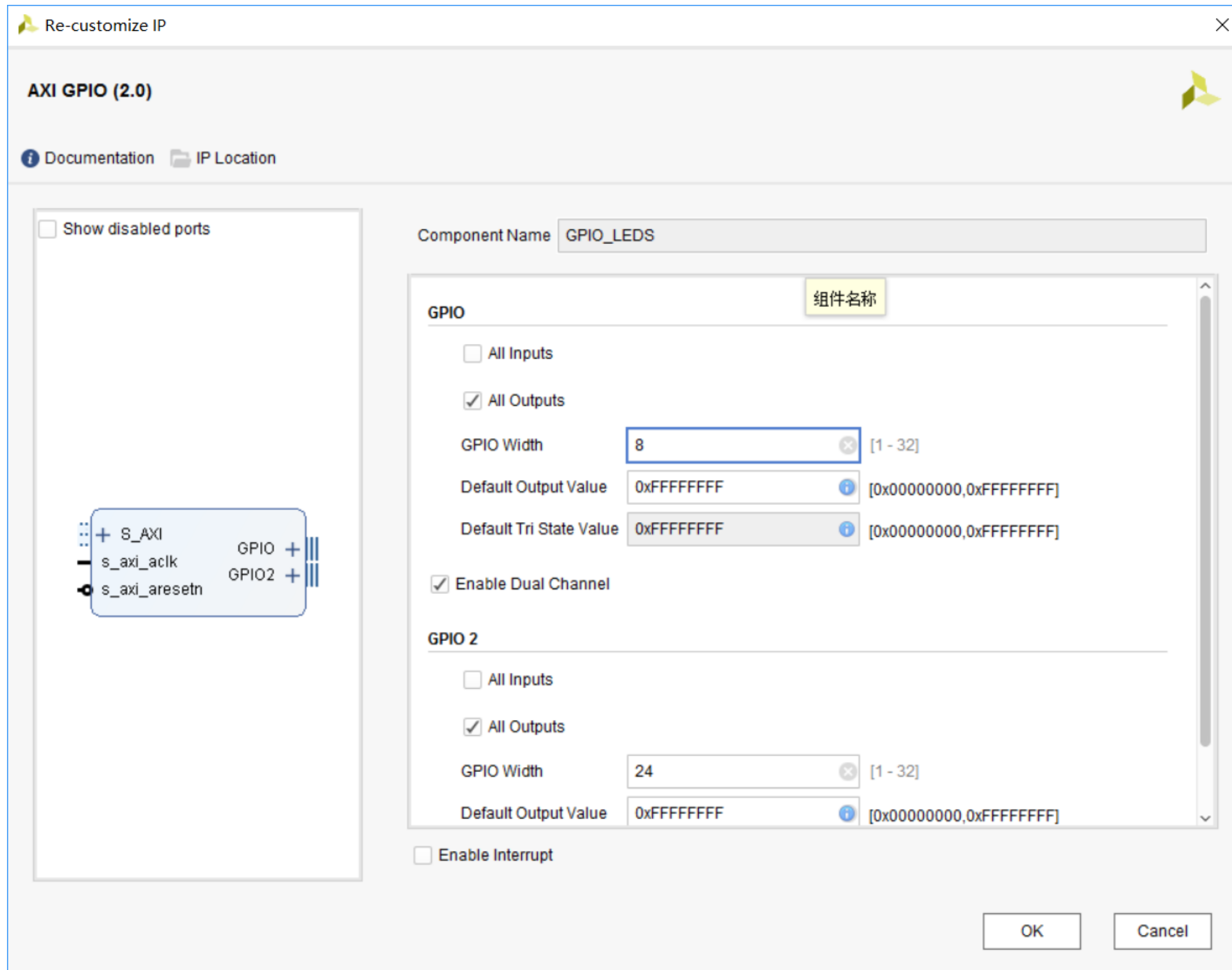
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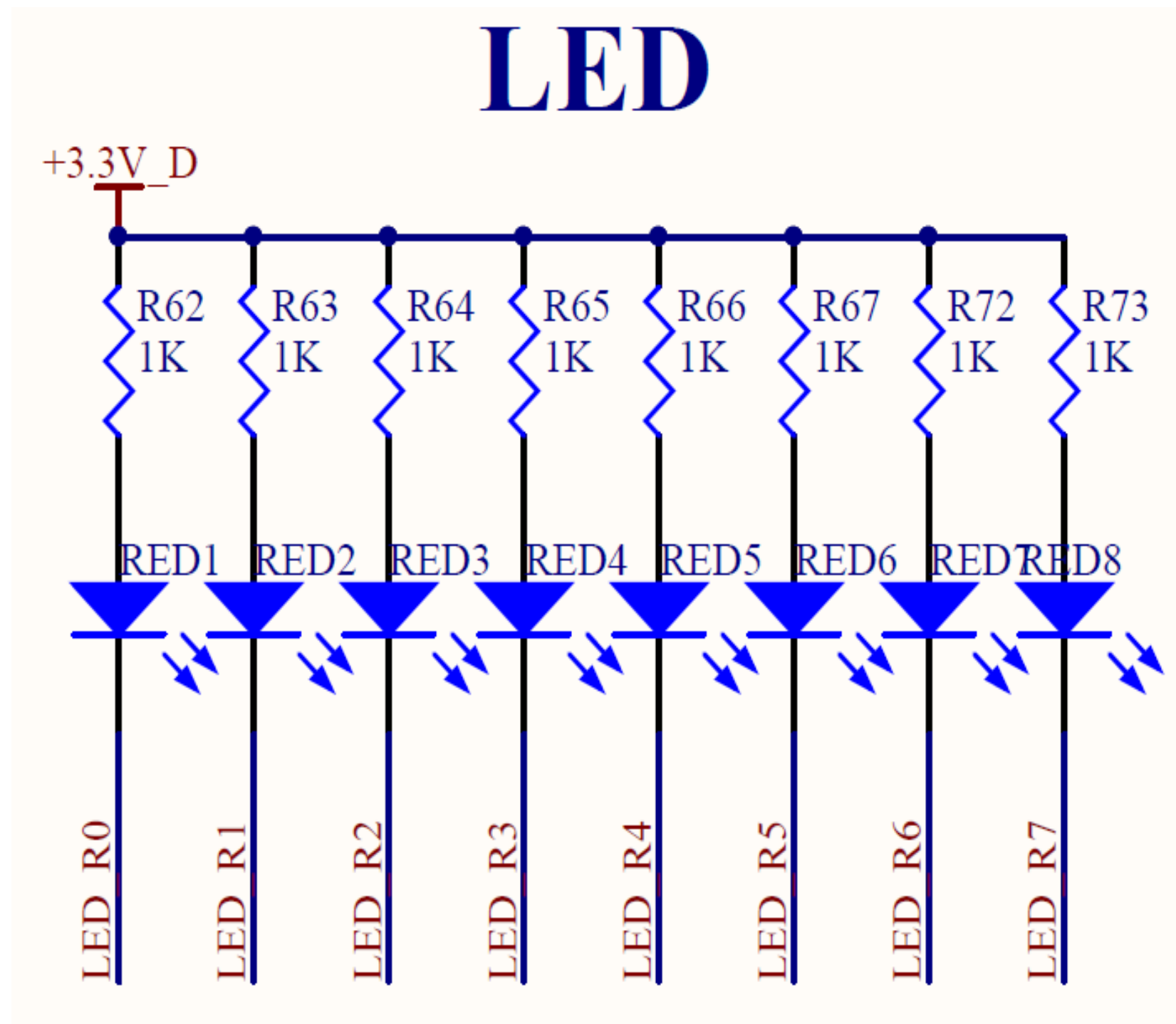
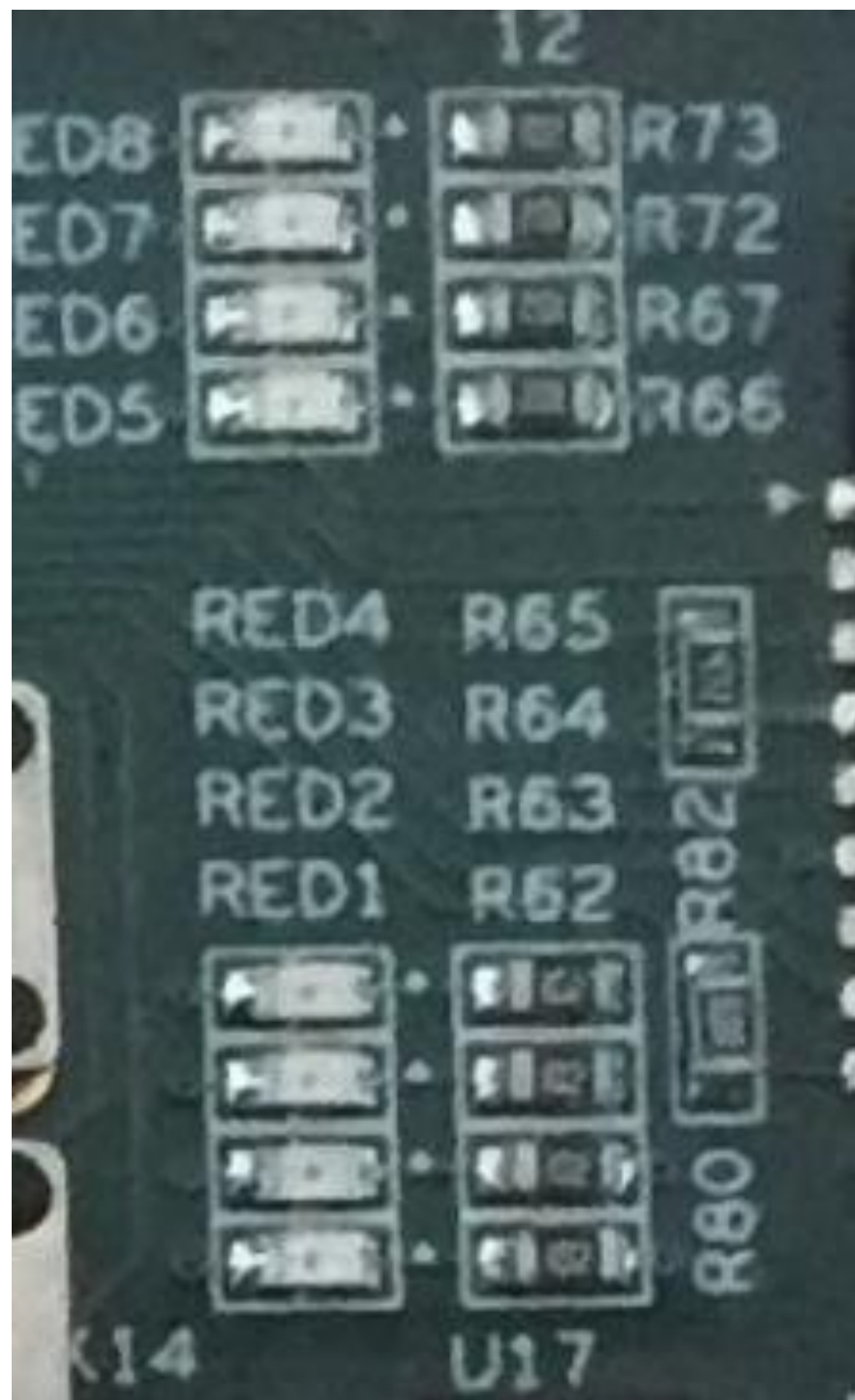


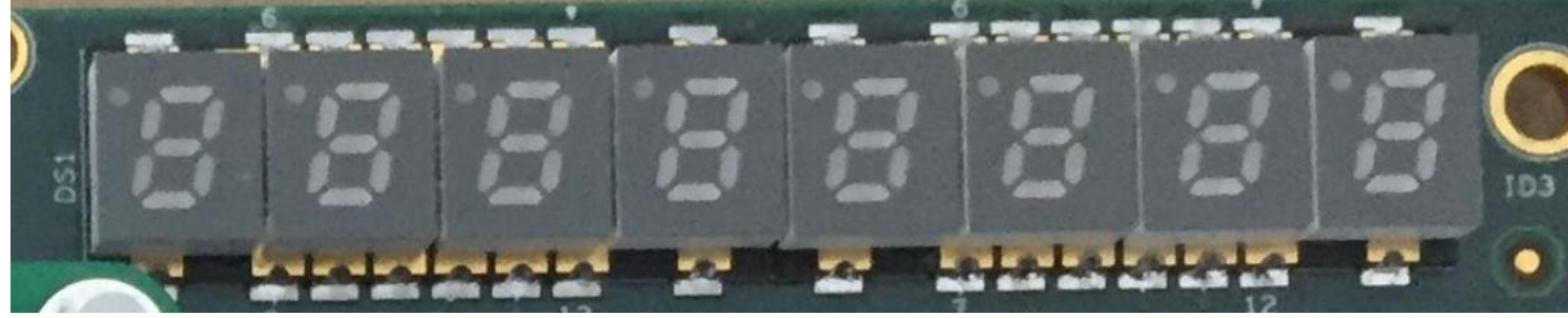


- 54位GPIO作为设备控制引脚
输出具有三态功能
- 192位GPIO通过EMIO连接到PL
其中64位输入，128位输出
- 每一位可动态编程访问也可分组访问
- 每一位均可单独中断，并可以指定中断类型

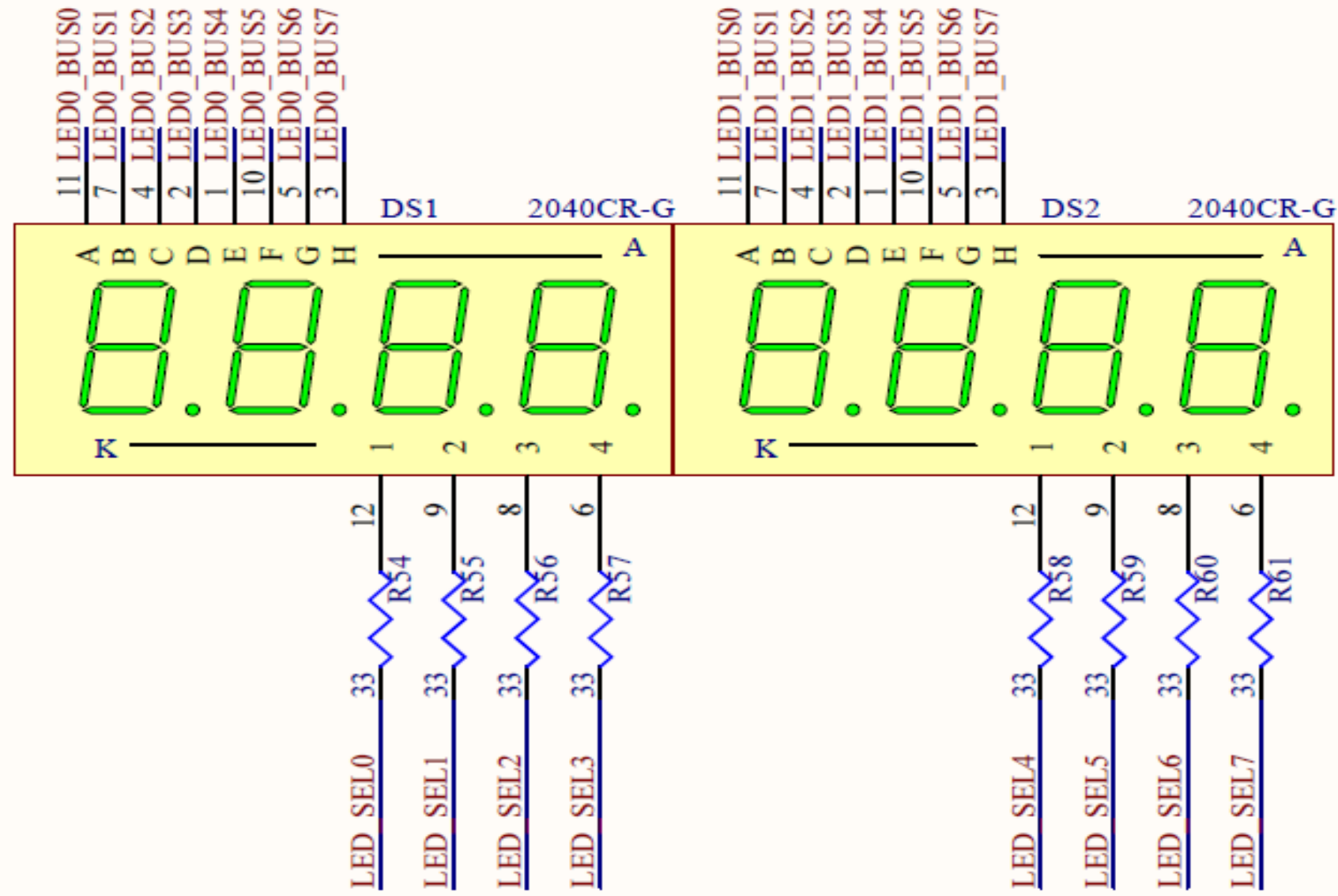


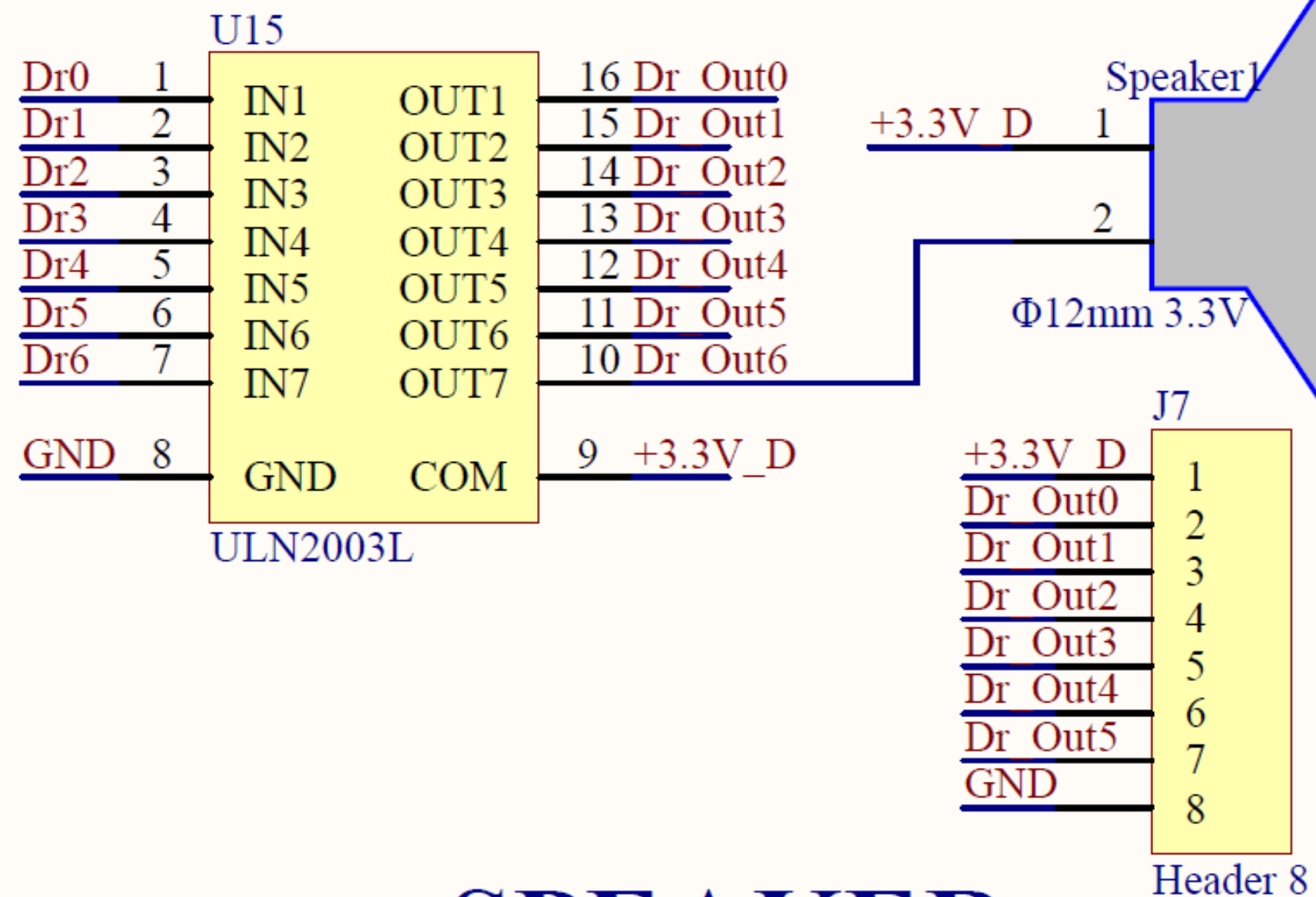
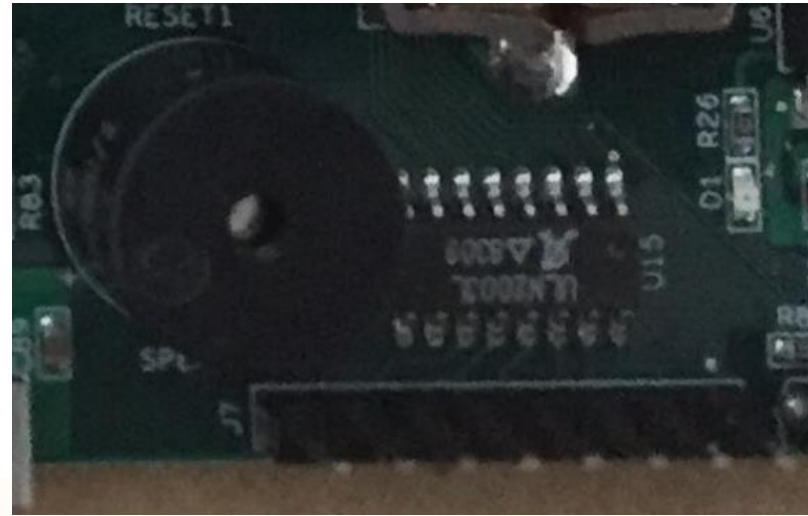






7 Segment LED

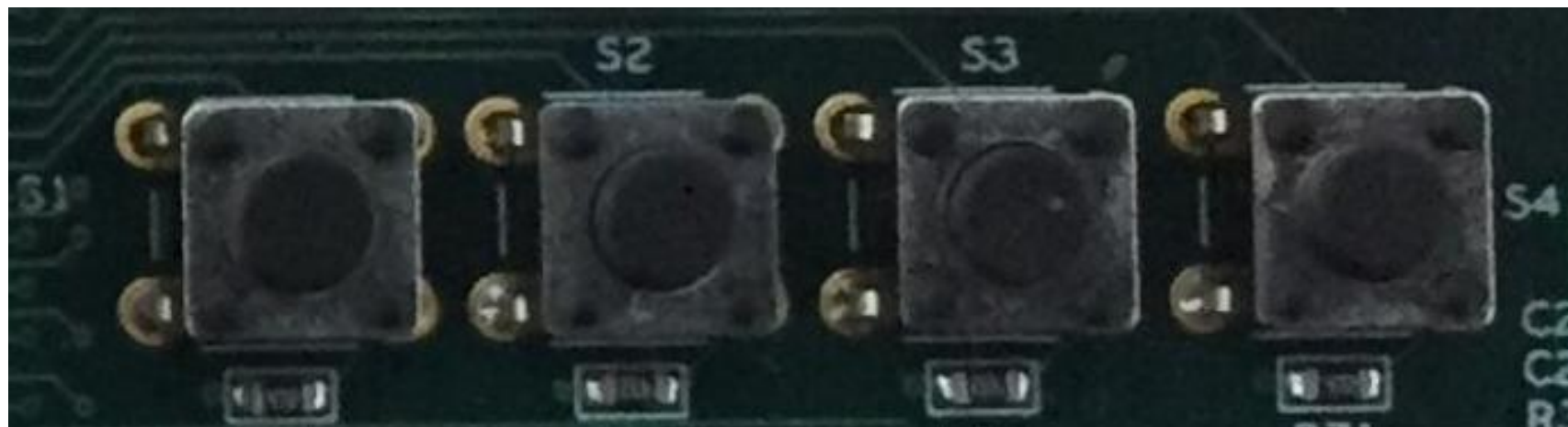




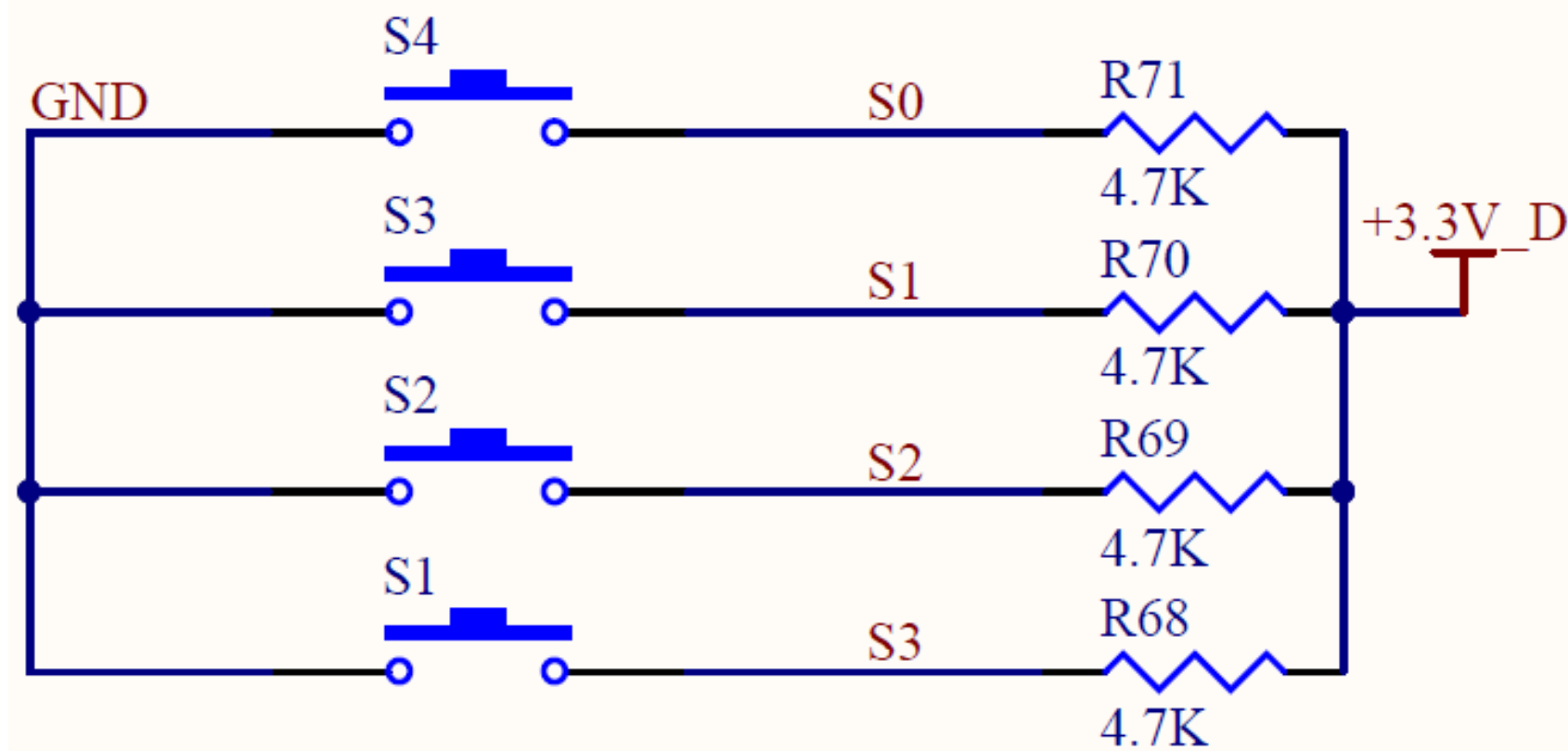
SPEAKER

ZYNQ-SoC

GPIO 输入

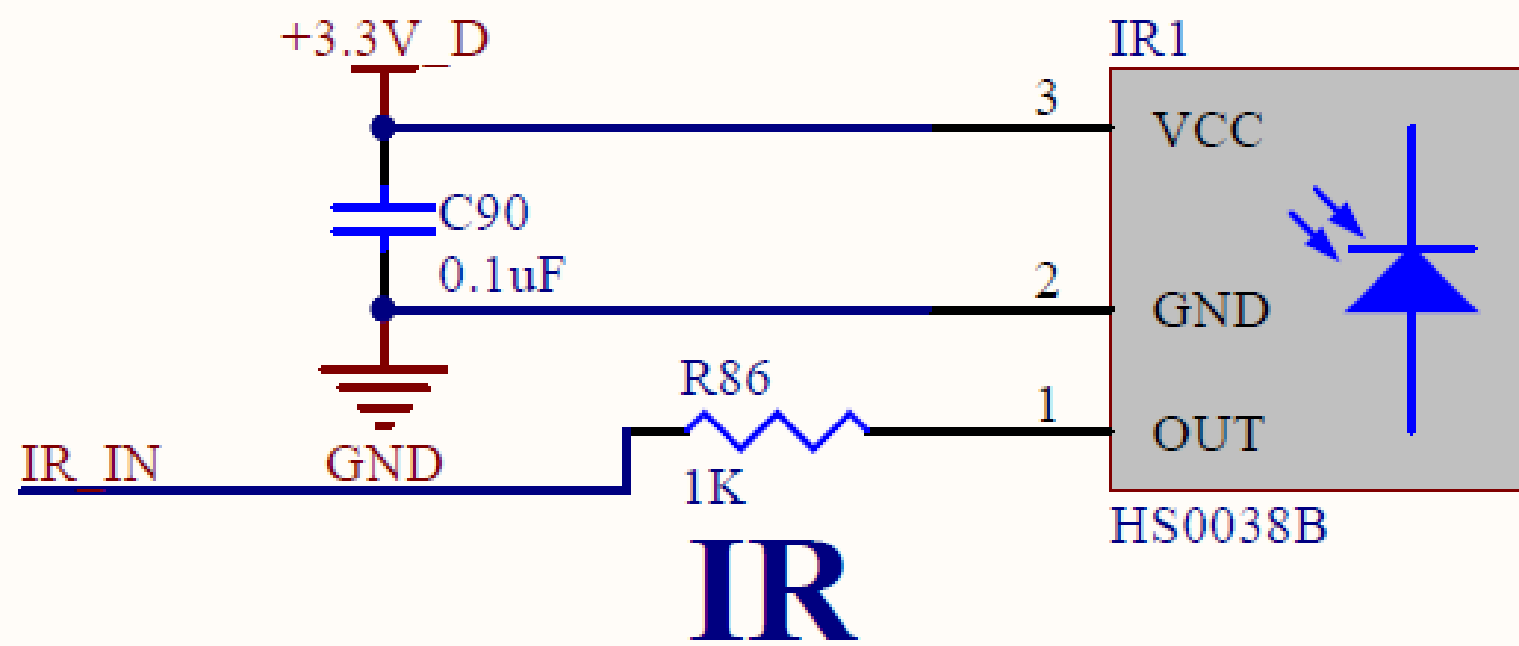


Button



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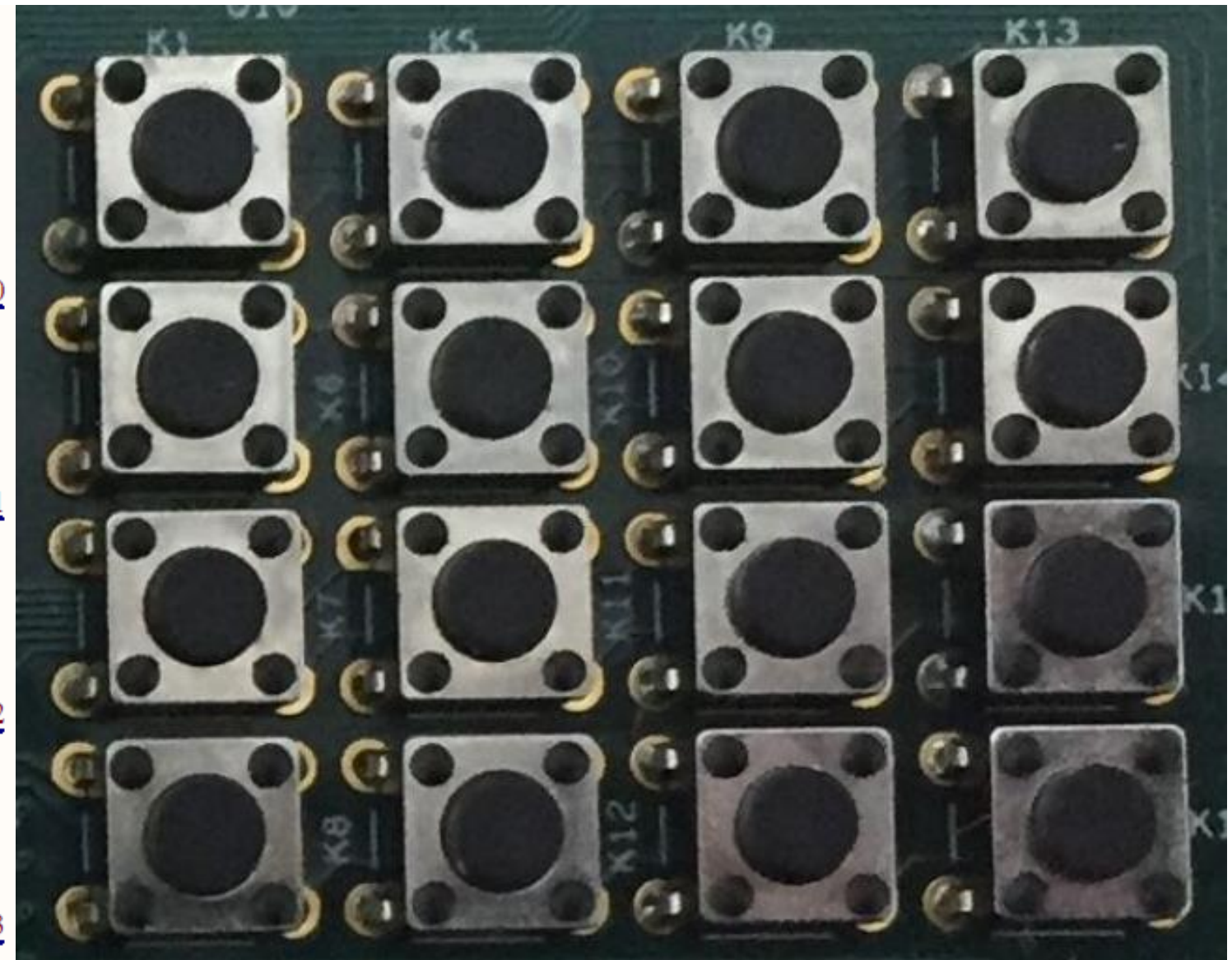
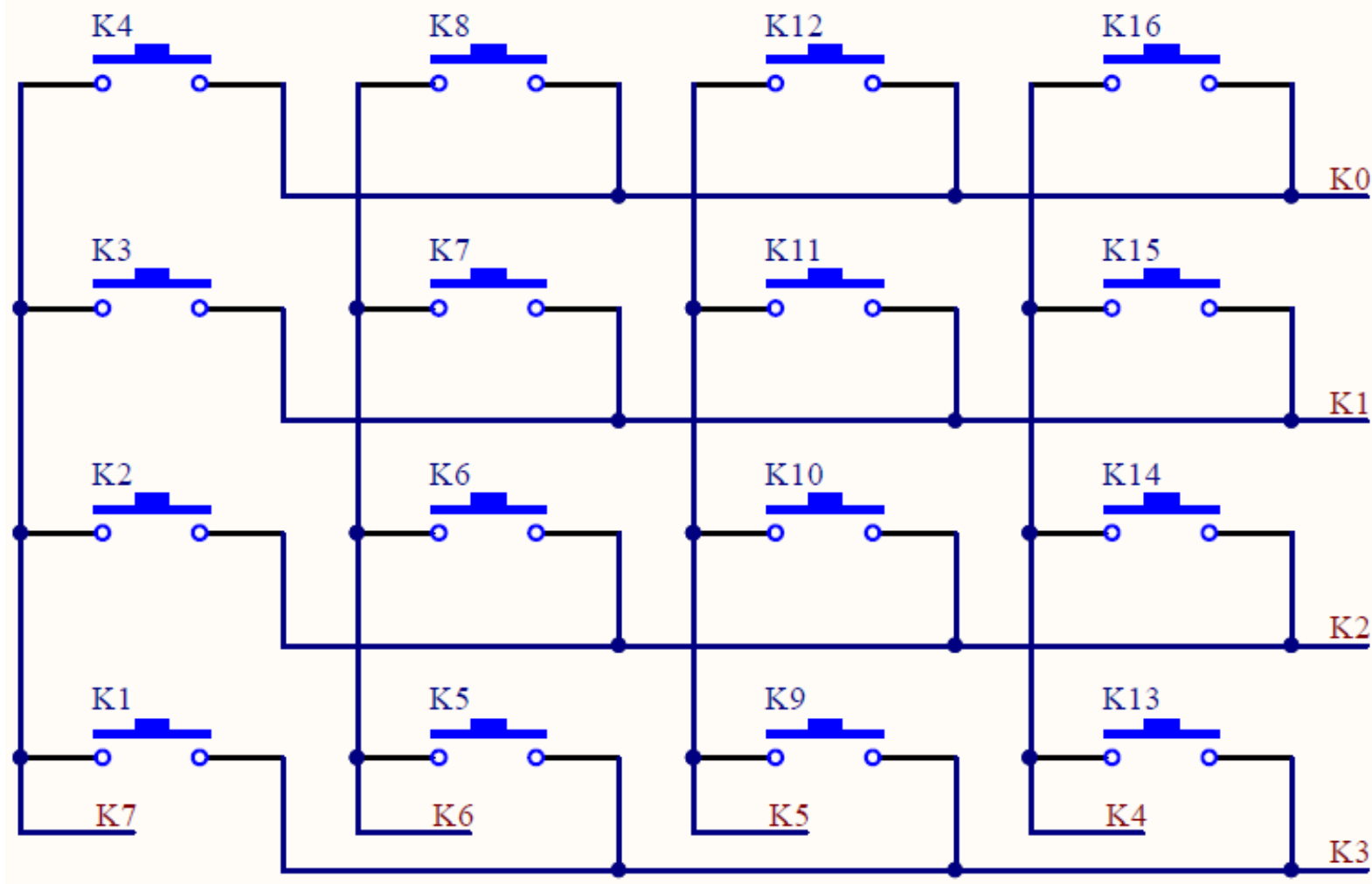
GPIO 输入



ZYNQ-SoC

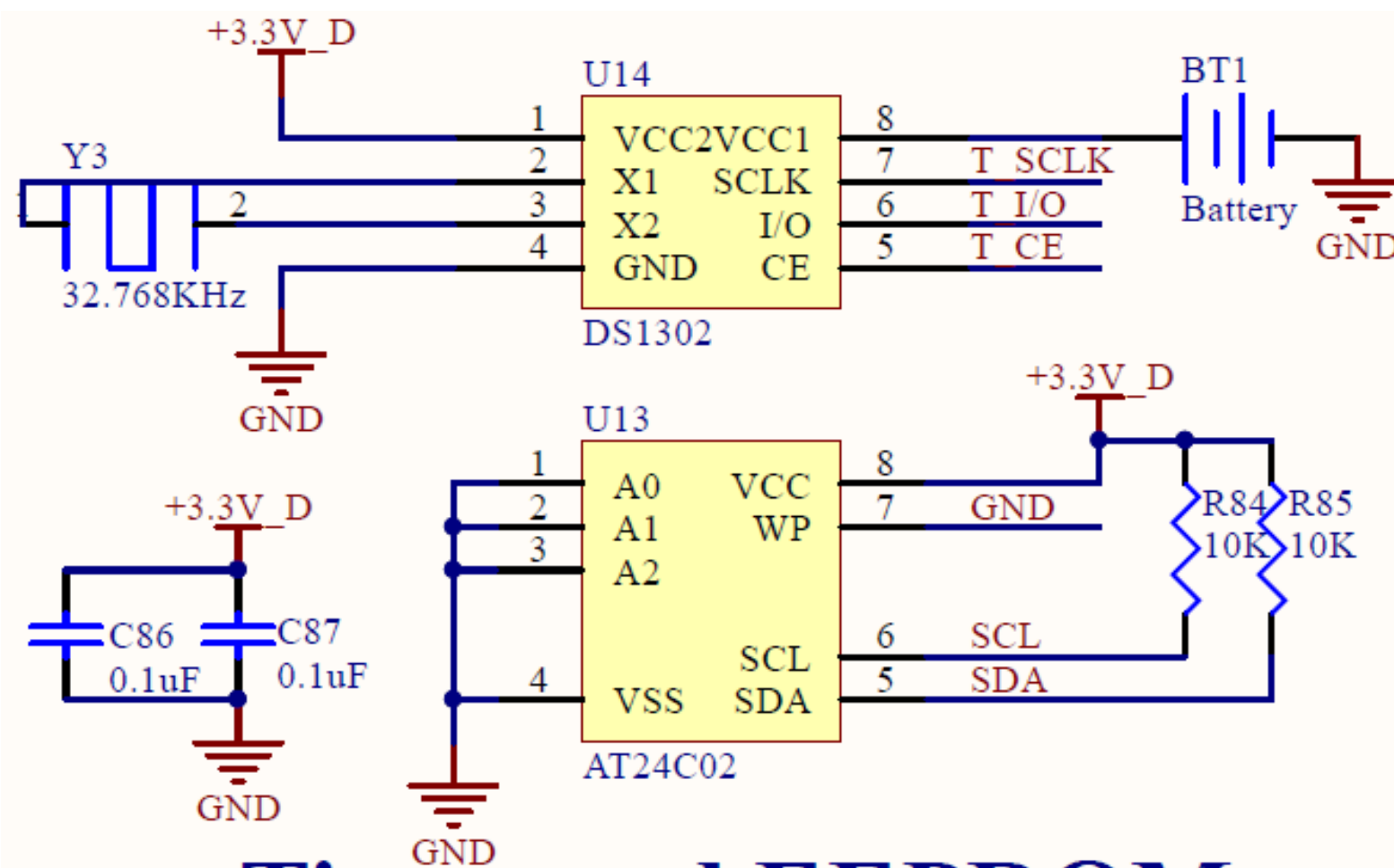
GPIO 双向

Matrix keyboard

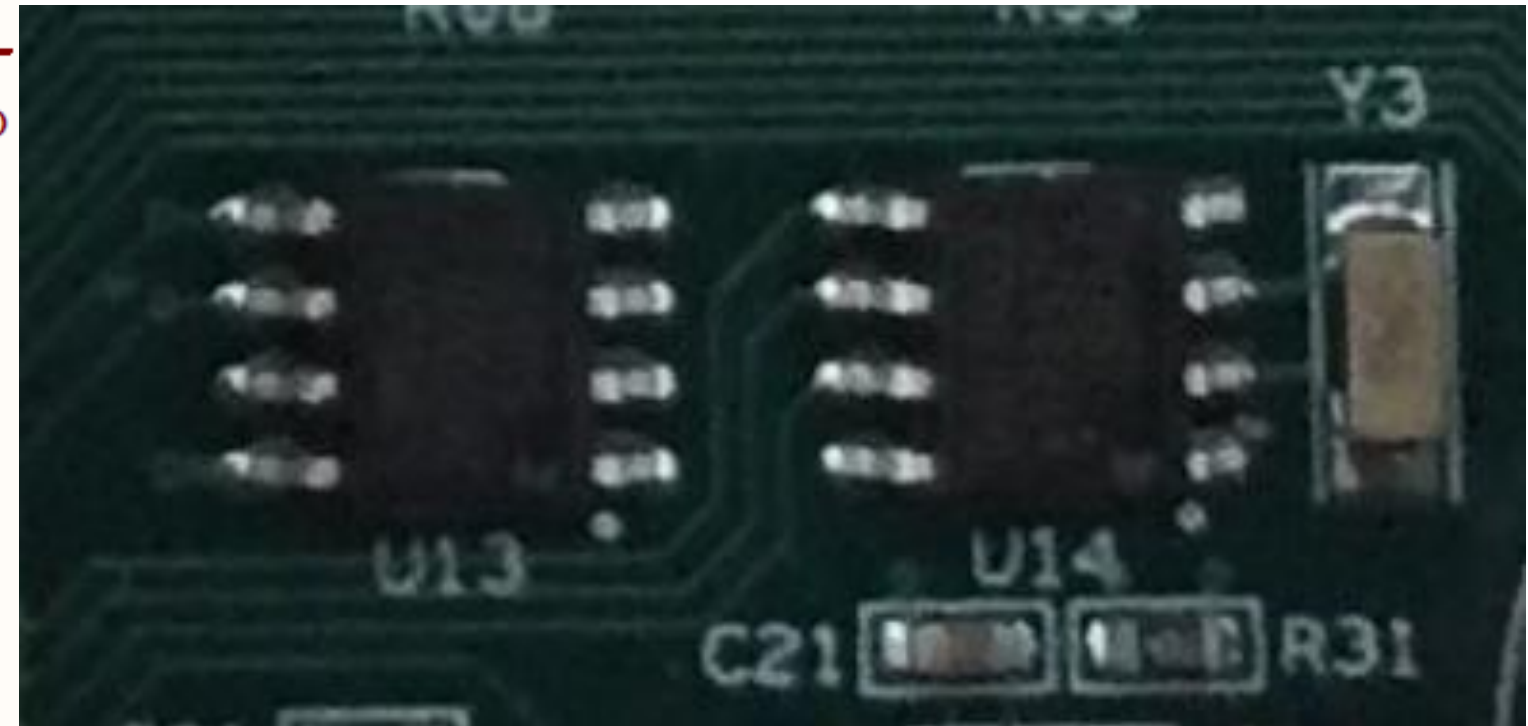


ZYNQ-SoC

GPIO 双向



Timer and EEPROM



思考题