CSE 3015 DIGITAL LOGIC DESIGN – PROJECT PART #1

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INSTRUCTION SET ARCHITECTURE

	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADD	0	0	DST				SRC1				SRC2				0000			
AND	0	0	DST				SRC1				SRC2				0001			
OR	0	0	DST				SRC1				SRC2				0010			
XOR	0	0	DST				SRC1				SRC2				0011			
ADDI	IMM						DST				SRC1				0100			
ANDI	IMM						DST				SRC1				0101			
ORI	IMM						DST				SRC1				0110			
XORI	IMM						DST				SRC1				0111			
JUMP	ADDR (PC RELATIVE)														1000			
BGT	ADDR (PC RELATIVE)						OP1				OP2				1001			
BEQ	ADDR (PC RELATIVE)						OP1				OP2				1010			
BGE	ADDR (PC RELATIVE)						OP1				OP2				1011			
BLT	ADDR (PC RELATIVE)						OP1				OP2				1100			
LD	ADDR (DATA MEMORY ADDRESS)										DST				1101			
BLE	ADDR (PC RELATIVE)						OP1				OP2				1110			
ST	ADDR (DATA MEMORY ADDRESS)										SRC				1111			