6. Using formal methods to generate a program

Hardware design (VHDL, Verilog)

- ✓ Used by semi-conductor companies such as Intel

Critical embedded software (B/Z, Lustre/Esterel)

- ✓ Urban Transportation
  (METEOR Metro Line 14 in Paris by Alstom)
- ✓ Rail transportation (Eurostar)
- ✓ Aeronautic (Airbus, Eurocopter, Dassault)
- ✓ Nuclear plants (Schneider Electric)

Pros and cons of using formal methods

✓ Nothing better than a mathematical proof

➡ A code "proven safe" is safe

◉ Development is time and effort (and so money) consuming

➡ Should be motivated by the risk analysis

◉ Do not prevent from specification bugs

➡ Example of network protocols