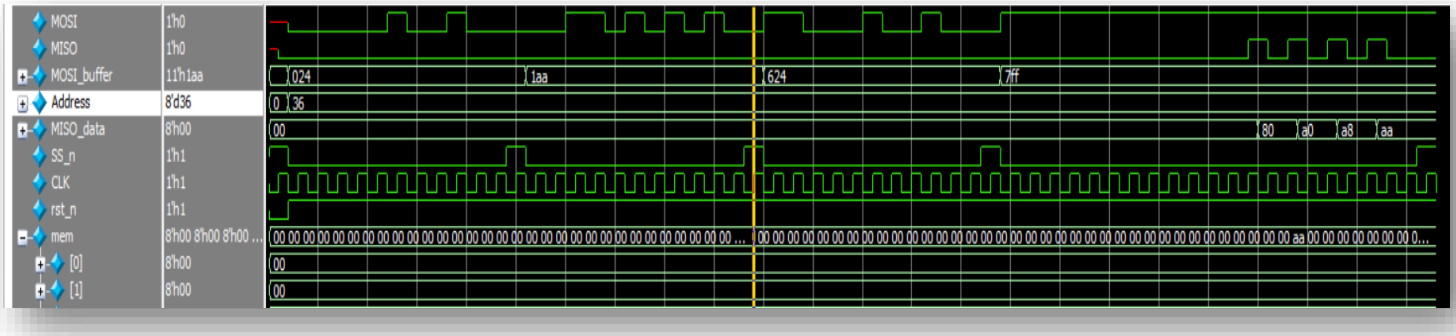
SPI Wrapper – Master to Ram comnunication

Table of Contents

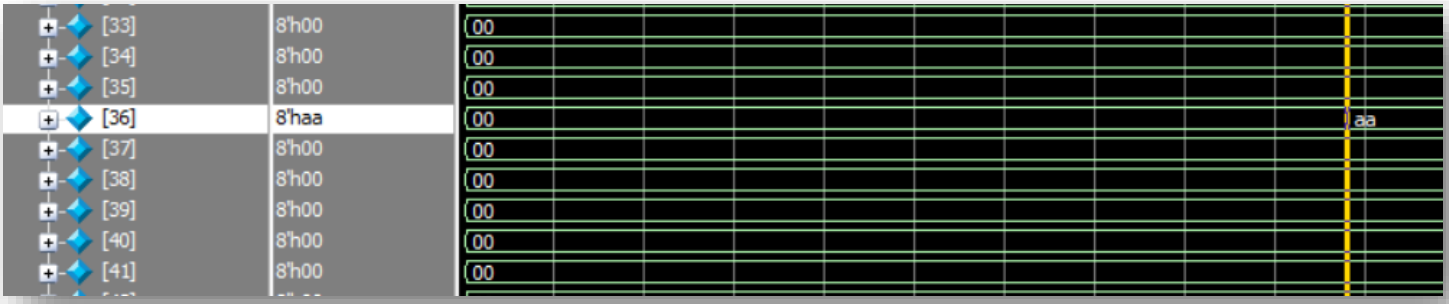
Team Members:

Name	Group Num:
Mina Hakim	**Group 2**
Mark Tamer	**Group 3**

1. QuestaSim Wavefrom:



Data Written (0xaa) at Address (36):



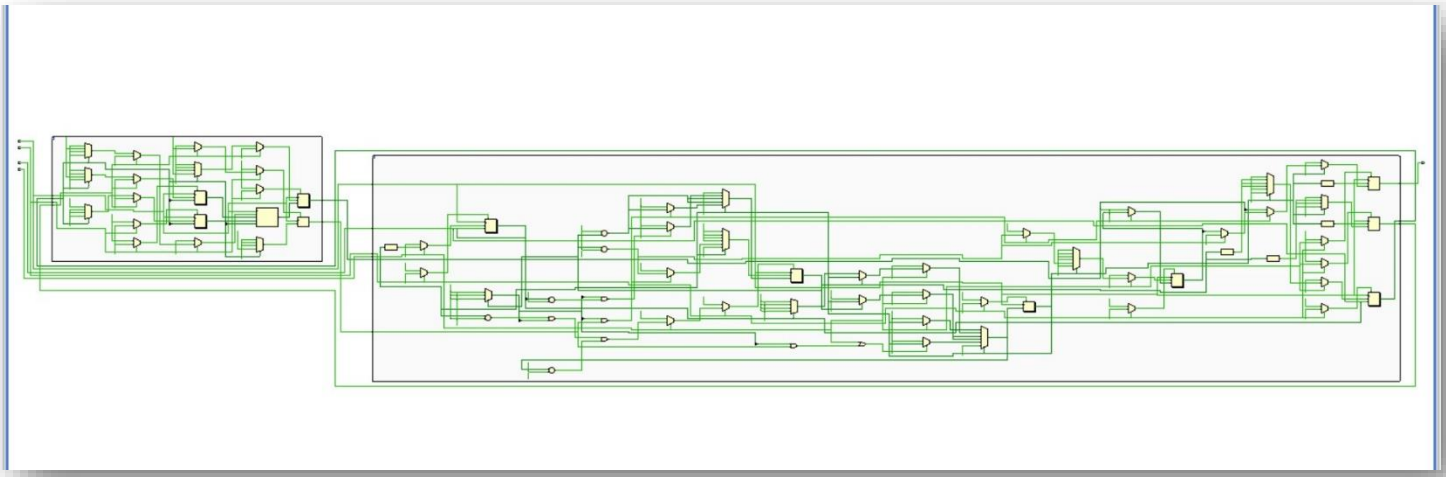
2. QuestaLint

Name	Count
Resolved(verified, fixed, waived)	5
Warning	1
seq_block_has_duplicate_assign	1
Info	4
always_signal_assign_large	1
line_char_large	1
multi_ports_in_single_line	2

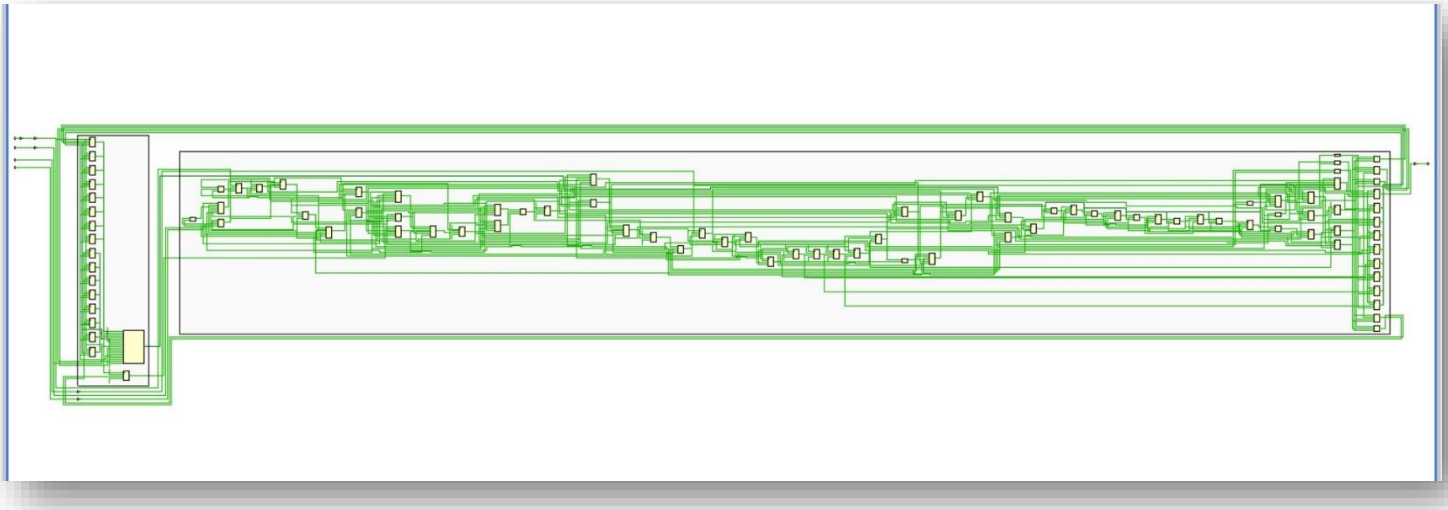
3. Synthesis

A. Sequential Encoding:

Elaboration Schematic:



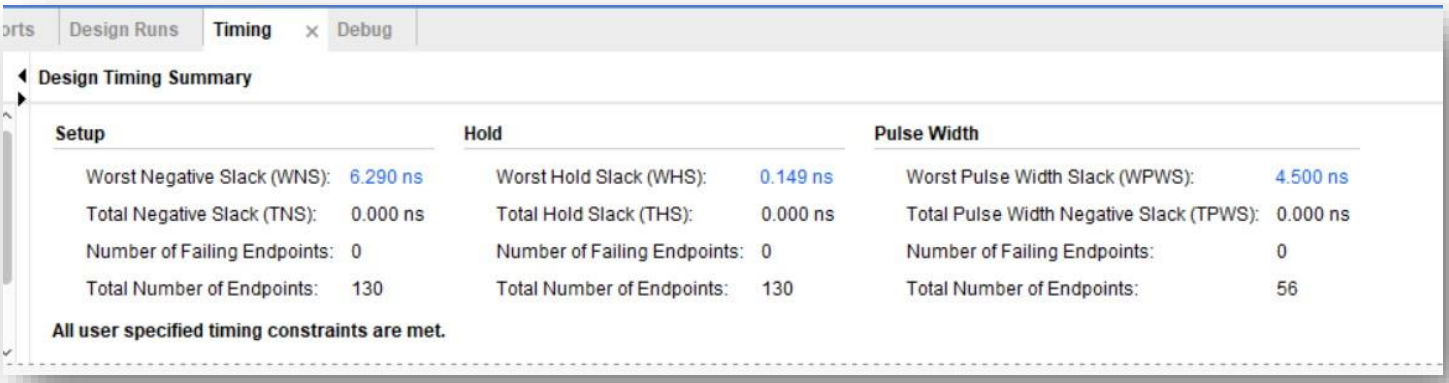
Synthesis Schematic:



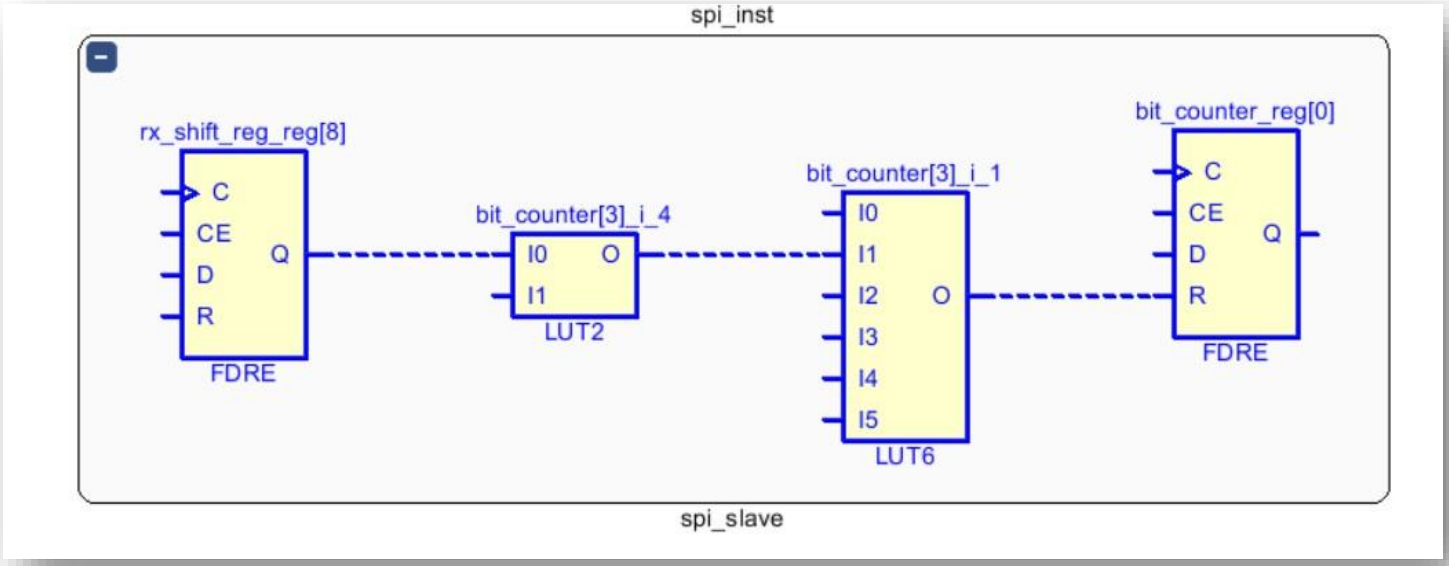
Synthesis Report:

```
87  ---------------------------------------------------------------------------------
88  INFO: [Synth 8-802] inferred FSM for state register 'state_reg' in module 'spi_slave'
89  INFO: [Synth 8-5544] ROM "rx_data" won't be mapped to Block RAM because address size (4) smaller than threshold (5)
90  INFO: [Synth 8-5544] ROM "miso" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
91  INFO: [Synth 8-5544] ROM "rx_valid" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
92  INFO: [Synth 8-5544] ROM "rx_shift_reg" won't be mapped to Block RAM because address size (3) smaller than threshold (5
93  INFO: [Synth 8-5544] ROM "next_state" won't be mapped to Block RAM because address size (2) smaller than threshold (5)
94  ---------------------------------------------------------------------------------------------------
95  |                   State |                     New Encoding |               Previous Encoding
96  ---------------------------------------------------------------------------------------------------
97  |                    IDLE |                              000 |                              000
98  |                 CHK_CMD |                              001 |                              001
99  |                   WRITE |                              010 |                              011
100 |                READ_ADD |                              011 |                              010
101 |               READ_DATA |                              100 |                              110
102 ---------------------------------------------------------------------------------------------------
```

Timing Report:

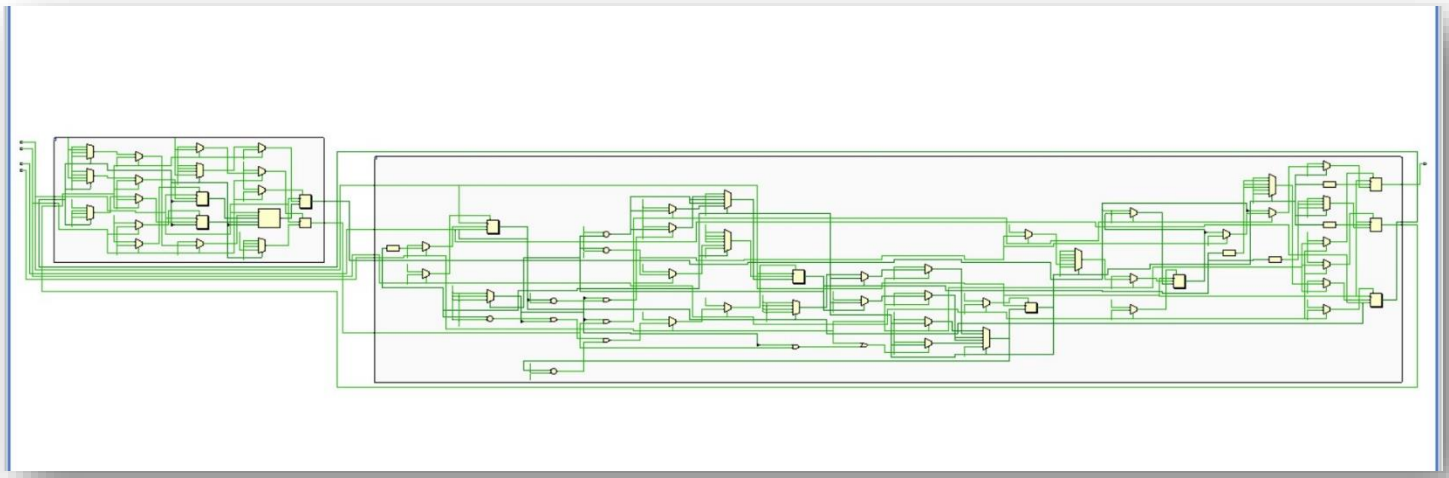


Critical Path:

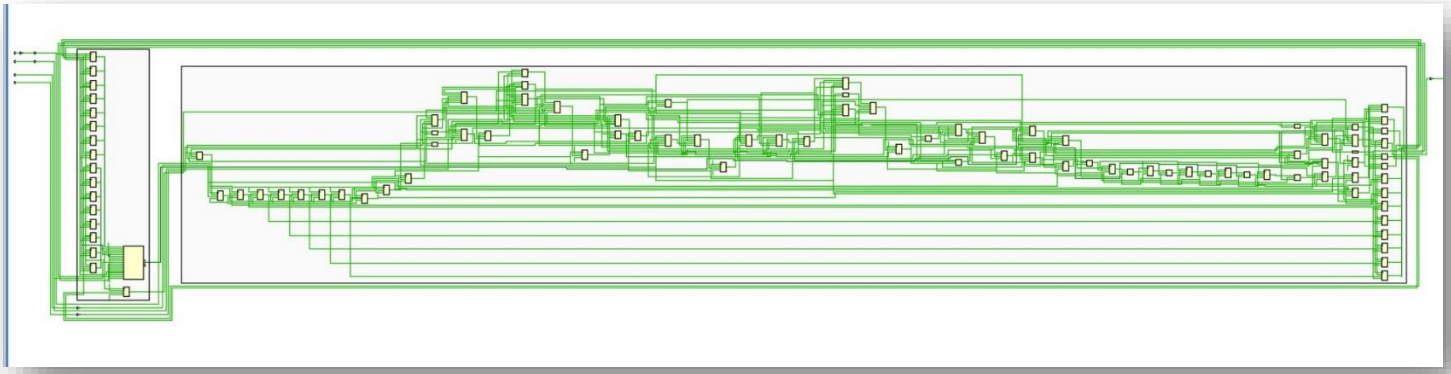


B. Gray Encoding:

Elaboration Schematic:



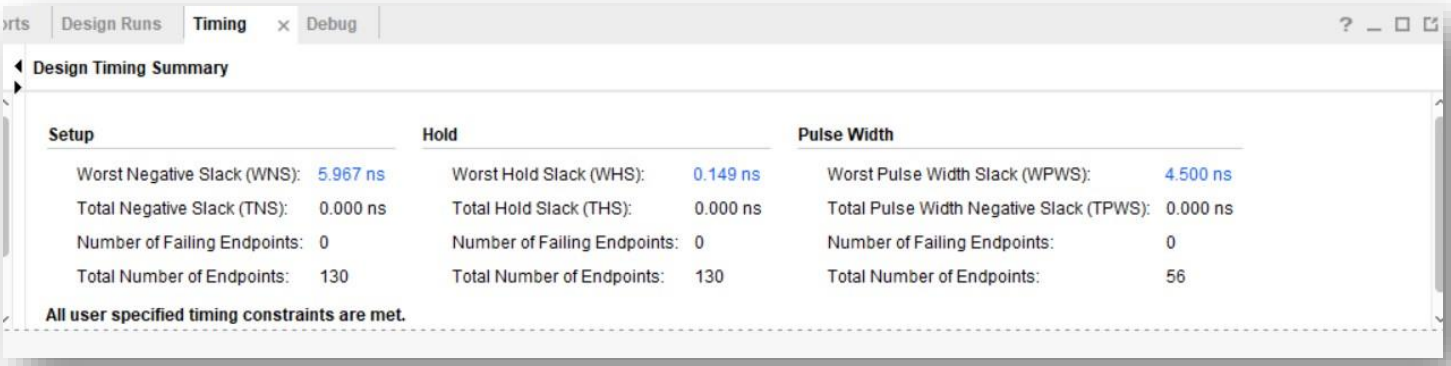
Synthesis Schematic:



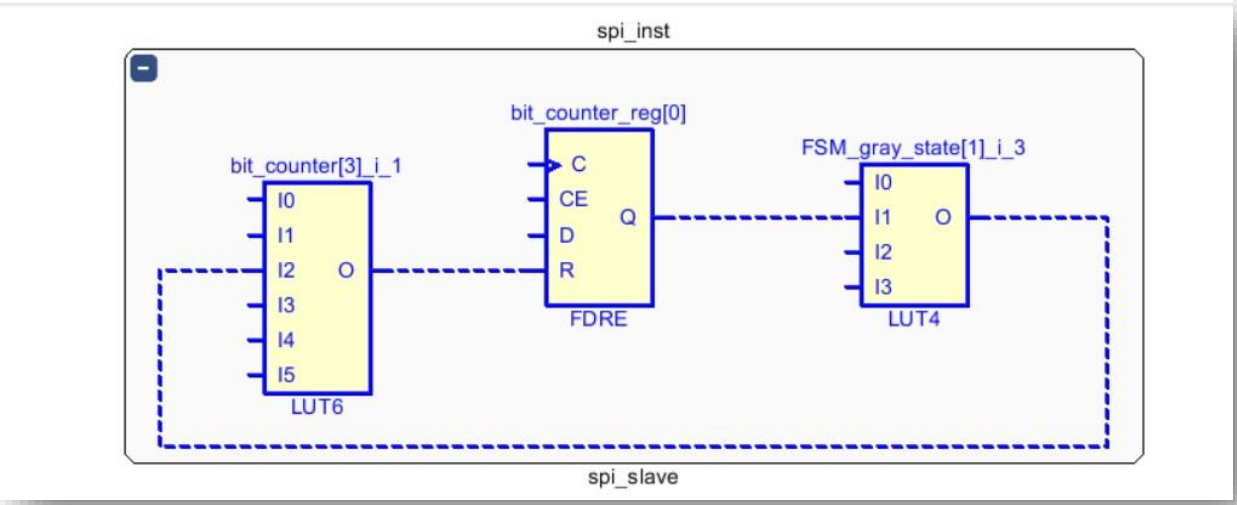
Synthesis Report:

```
INFO: [Synth 8-5544] ROM "rx_data" won't be mapped to Block RAM because address size (4) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "miso" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "rx_valid" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "rx_shift_reg" won't be mapped to Block RAM because address size (3) smaller than threshold (5
INFO: [Synth 8-5544] ROM "next_state" won't be mapped to Block RAM because address size (2) smaller than threshold (5)
---------------------------------------------------------------------------------------------------
                   State |                     New Encoding |               Previous Encoding
---------------------------------------------------------------------------------------------------
                    IDLE |                              000 |                              000
                 CHK_CMD |                              001 |                              001
                   WRITE |                              011 |                              011
                READ_ADD |                              010 |                              010
               READ_DATA |                              111 |                              110
---------------------------------------------------------------------------------------------------
INFO: [Synth 8-3354] encoded FSM with state register 'state_reg' using encoding 'gray' in module 'spi_slave'
---------------------------------------------------------------------------------------------------
```

Timing Report:

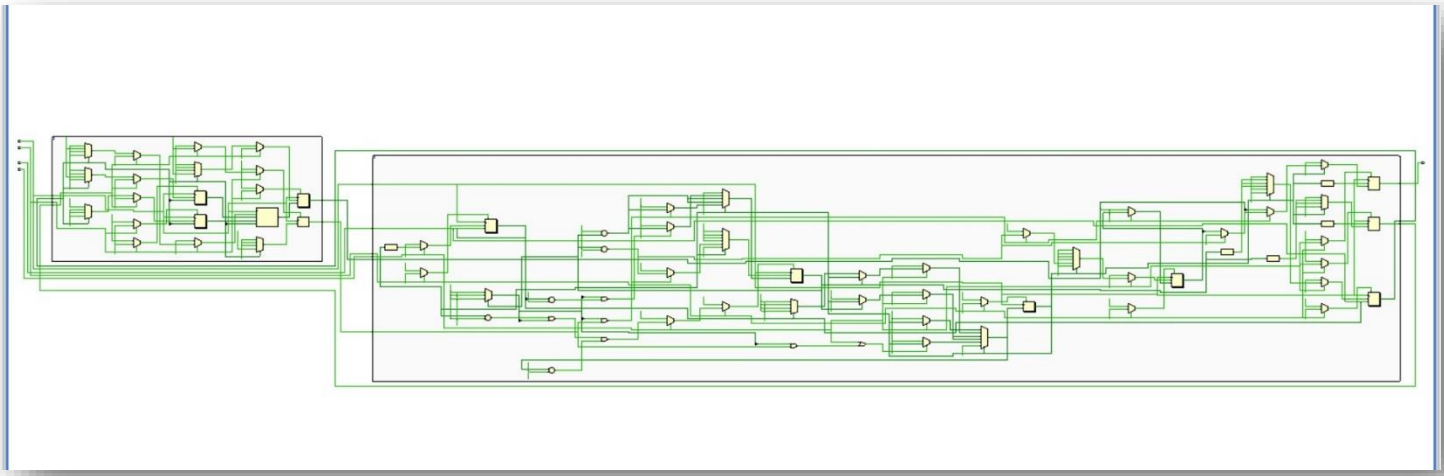


Critical Path:

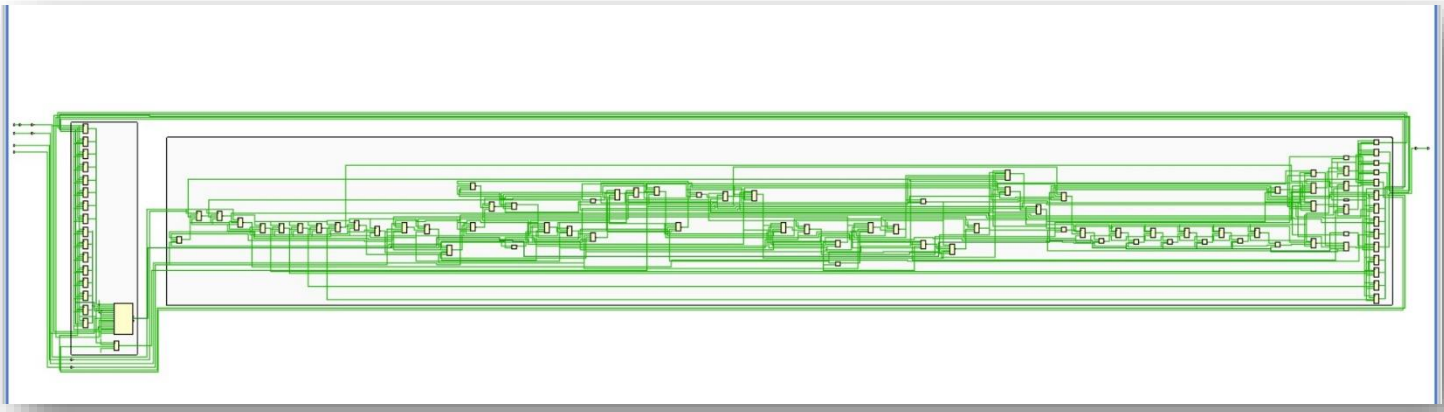


C. One Hot Encoding:

Elaboration Schematic:



Synthesis Schematic:



Synthesis Report:

```
INFO: [Synth 8-5544] ROM "miso" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "rx_valid" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "rx_shift_reg" won't be mapped to Block RAM because address size (3) smaller than threshold (
INFO: [Synth 8-5544] ROM "next_state" won't be mapped to Block RAM because address size (2) smaller than threshold (5)
---------------------------------------------------------------------------------------------------
                   State |                     New Encoding |               Previous Encoding
---------------------------------------------------------------------------------------------------
                    IDLE |                            00001 |                              000
                 CHK_CMD |                            00010 |                              001
                   WRITE |                            00100 |                              011
                READ_ADD |                            01000 |                              010
               READ_DATA |                            10000 |                              110
---------------------------------------------------------------------------------------------------
INFO: [Synth 8-3354] encoded FSM with state register 'state_reg' using encoding 'one-hot' in module 'spi_slave'
---------------------------------------------------------------------------------------------------
```

Timing Report:

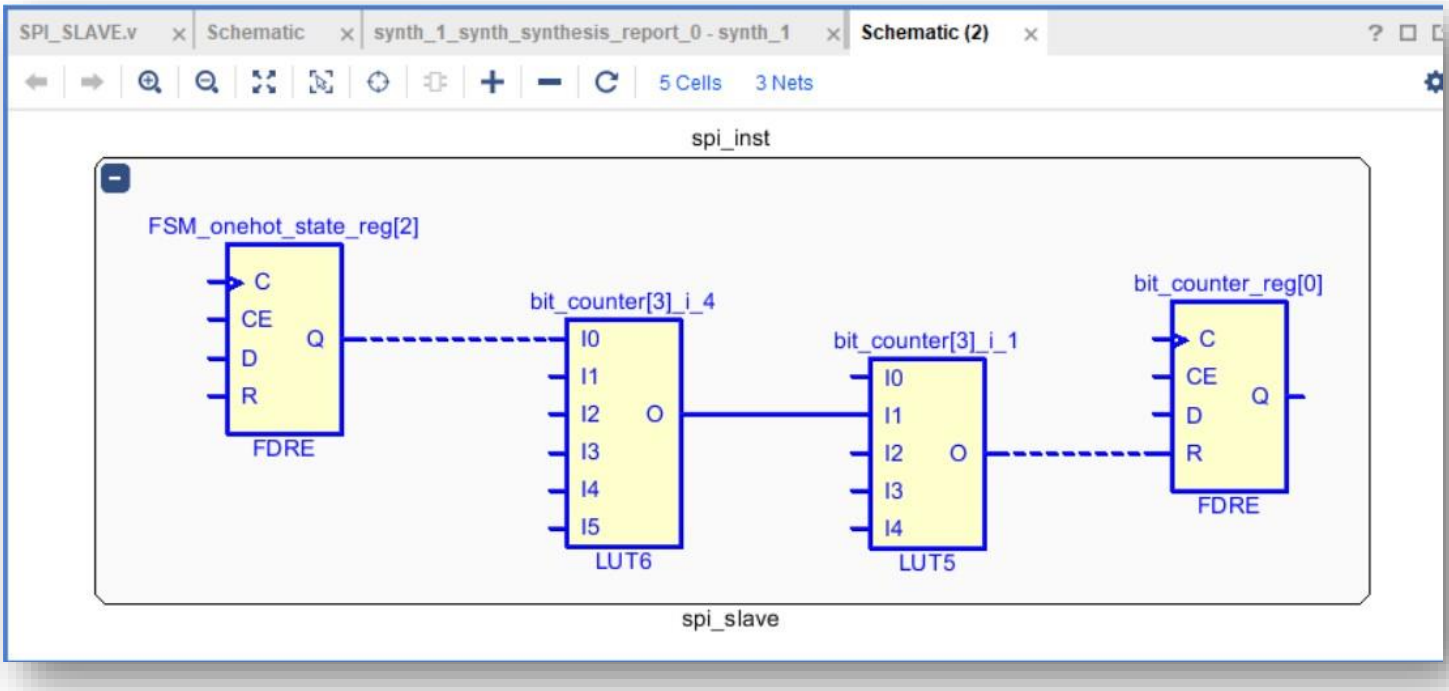
ts | Design Runs | **Timing** | Debug

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.293 ns	Worst Hold Slack (WHS):	0.149 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	132	Total Number of Endpoints:	132	Total Number of Endpoints:	58

All user specified timing constraints are met.

Critical Path:



4. Implementation:

Sequential Encoding:

Utilization report:

Reports | Design Runs | Power | Methodology | Timing | **Utilization** ×

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N slave_ram_top_module	36	53	17	36	13	0.5	5	1
ram_inst (ram)	1	17	4	1	0	0.5	0	0
spi_inst (spi_slave)	35	36	16	35	13	0	0	0

Timing report:

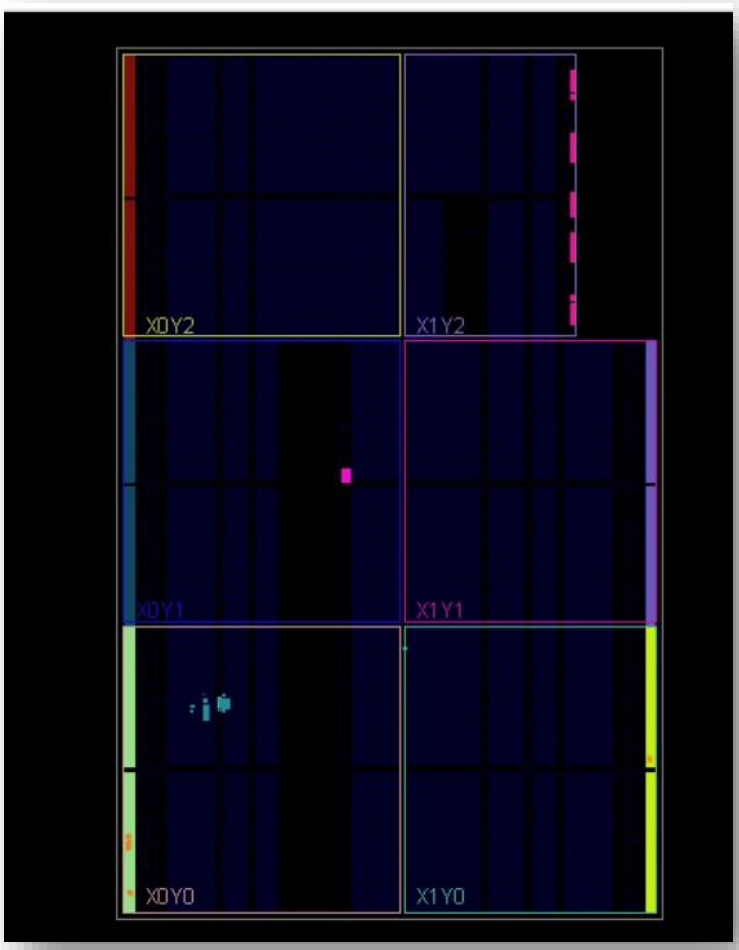
rts | Design Runs | Power | Methodology | **Timing** ×

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.987 ns	Worst Hold Slack (WHS):	0.101 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	131	Total Number of Endpoints:	131	Total Number of Endpoints:	56

All user specified timing constraints are met.

FPGA device snippet:



Gray Encoding:

Utilization report:

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N slave_ram_top_module	41	53	18	41	13	0.5	5	1
ram_inst (ram)	1	17	4	1	0	0.5	0	0
spi_inst (spi_slave)	40	36	16	40	13	0	0	0

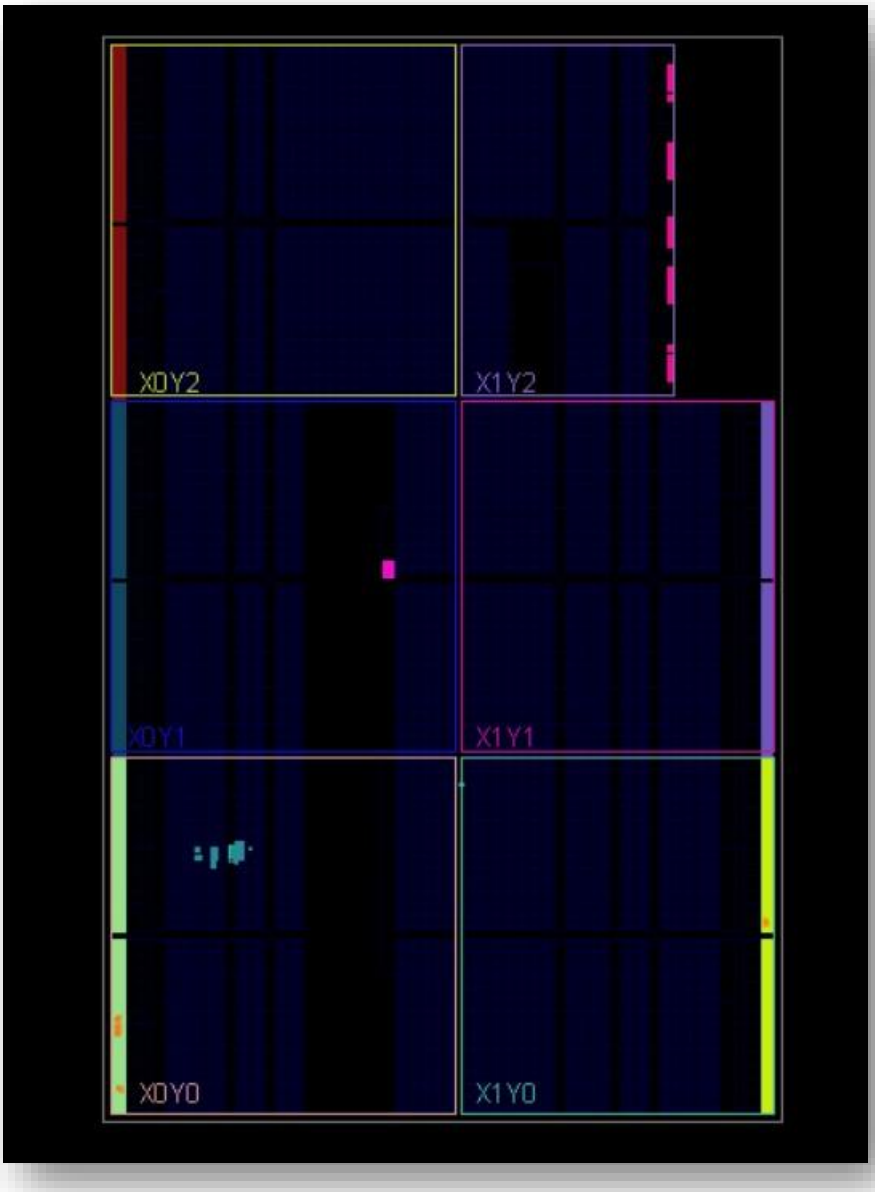
Timing report:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.998 ns	Worst Hold Slack (WHS):	0.044 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	131	Total Number of Endpoints:	131	Total Number of Endpoints:	56

All user specified timing constraints are met.

FPGA device snippet:



One Hot Encoding:

Utilization report:

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N slave_ram_top_module	38	55	19	38	13	0.5	5	1
ram_inst (ram)	1	17	3	1	0	0.5	0	0
spi_inst (spi_slave)	37	38	17	37	13	0	0	0

Timing report:

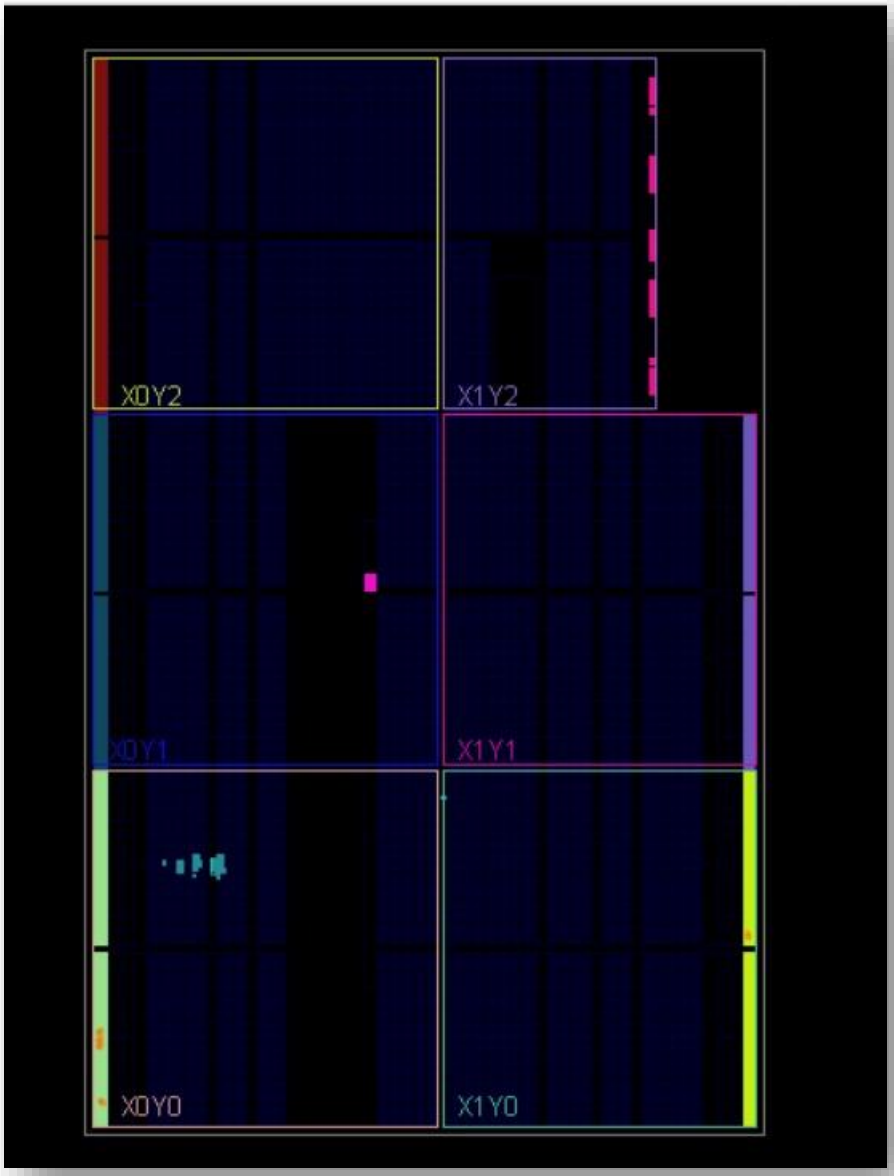
s | Design Runs | Power | Methodology | Timing

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.667 ns	Worst Hold Slack (WHS):	0.067 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	133	Total Number of Endpoints:	133	Total Number of Endpoints:	58

All user specified timing constraints are met.

FPGA device snippet:



5. "Messages" Tab:

Note: Critical Warning due to hold time violation from debug cores