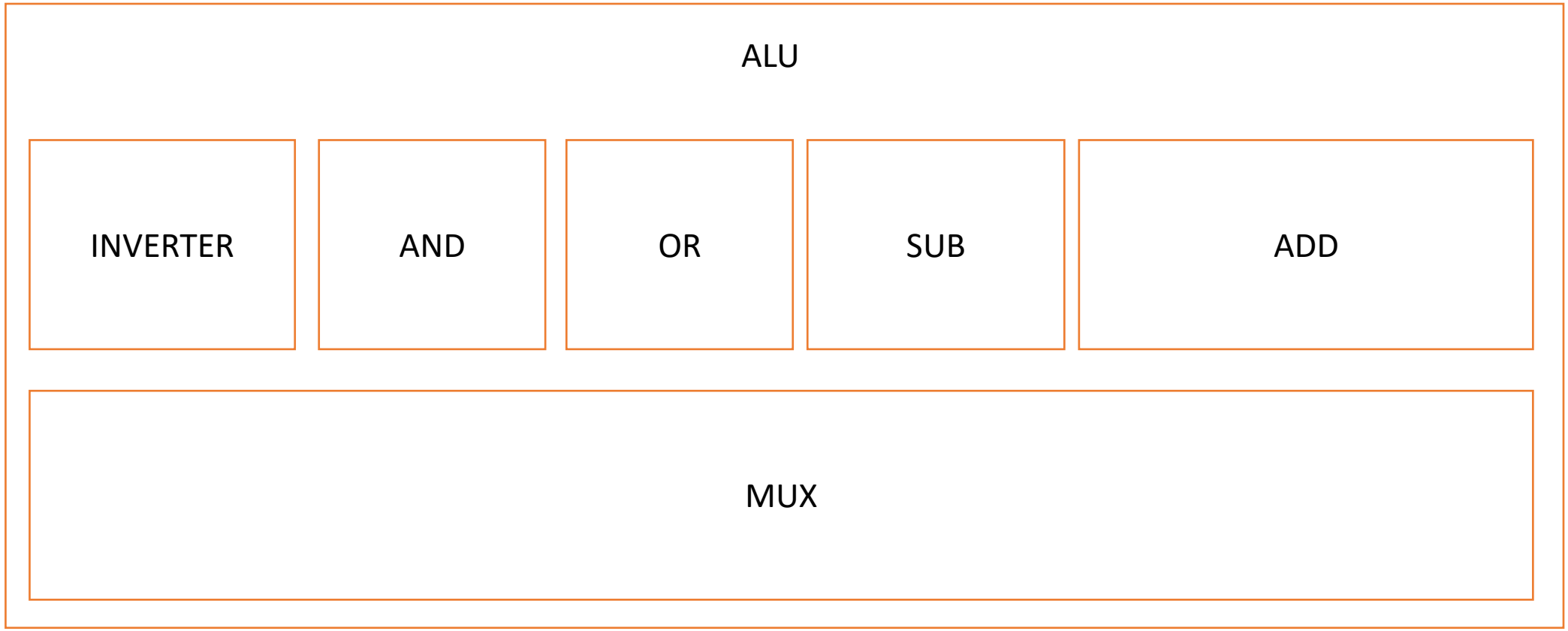
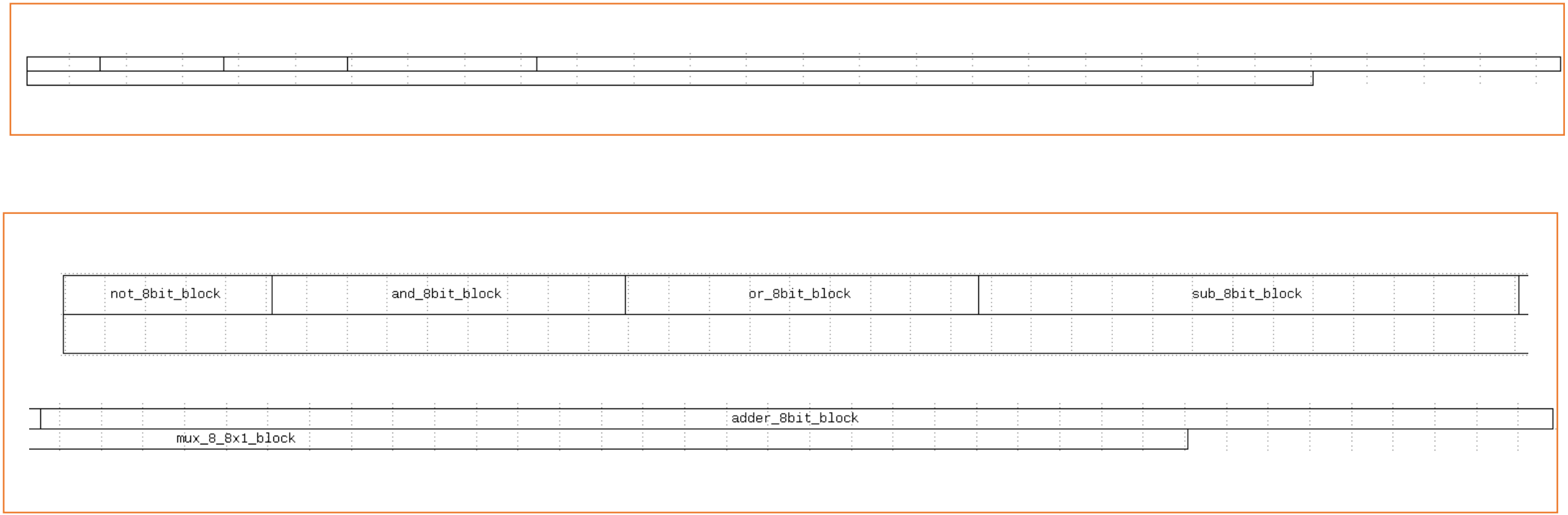
8-Bit ALU
Physical layout and pre-layout simulation

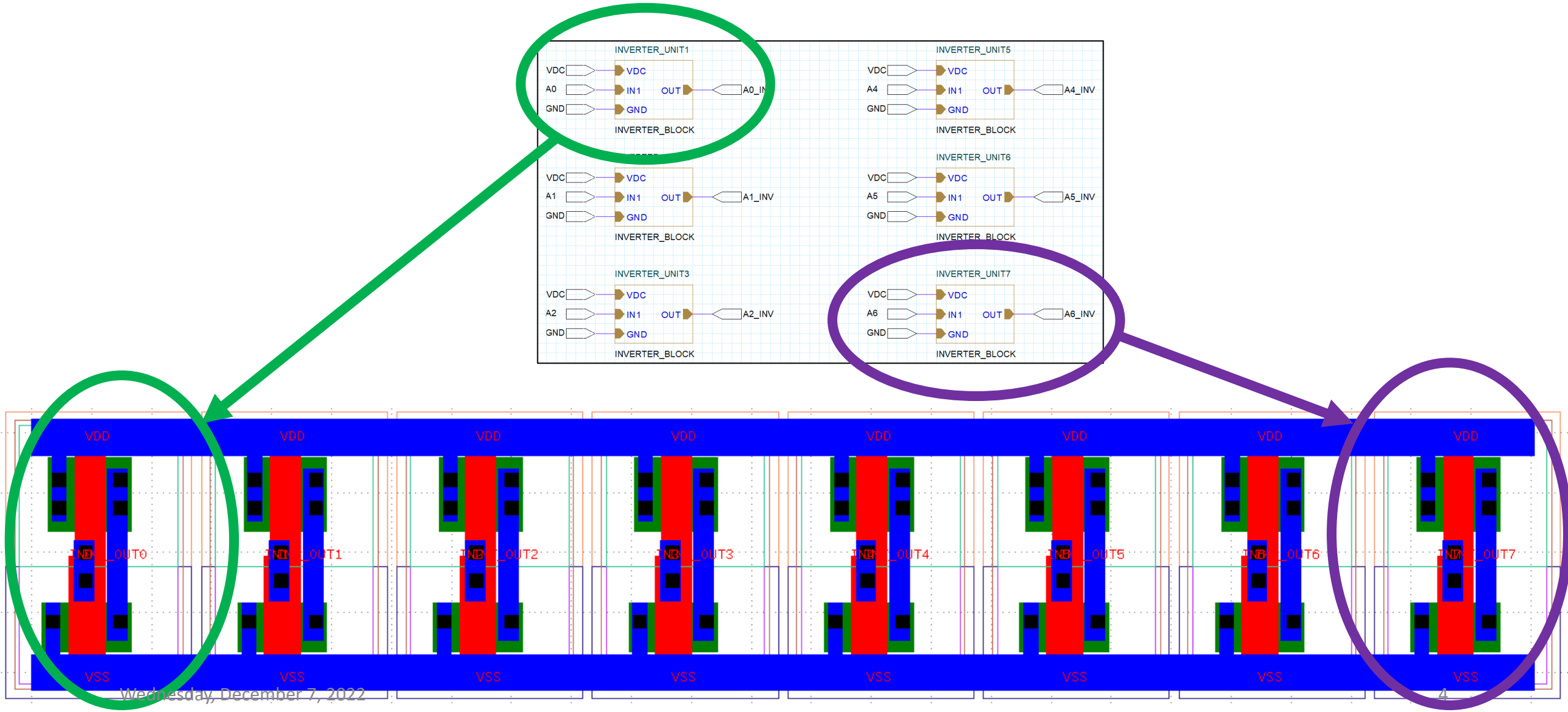
ALU - architectural top view



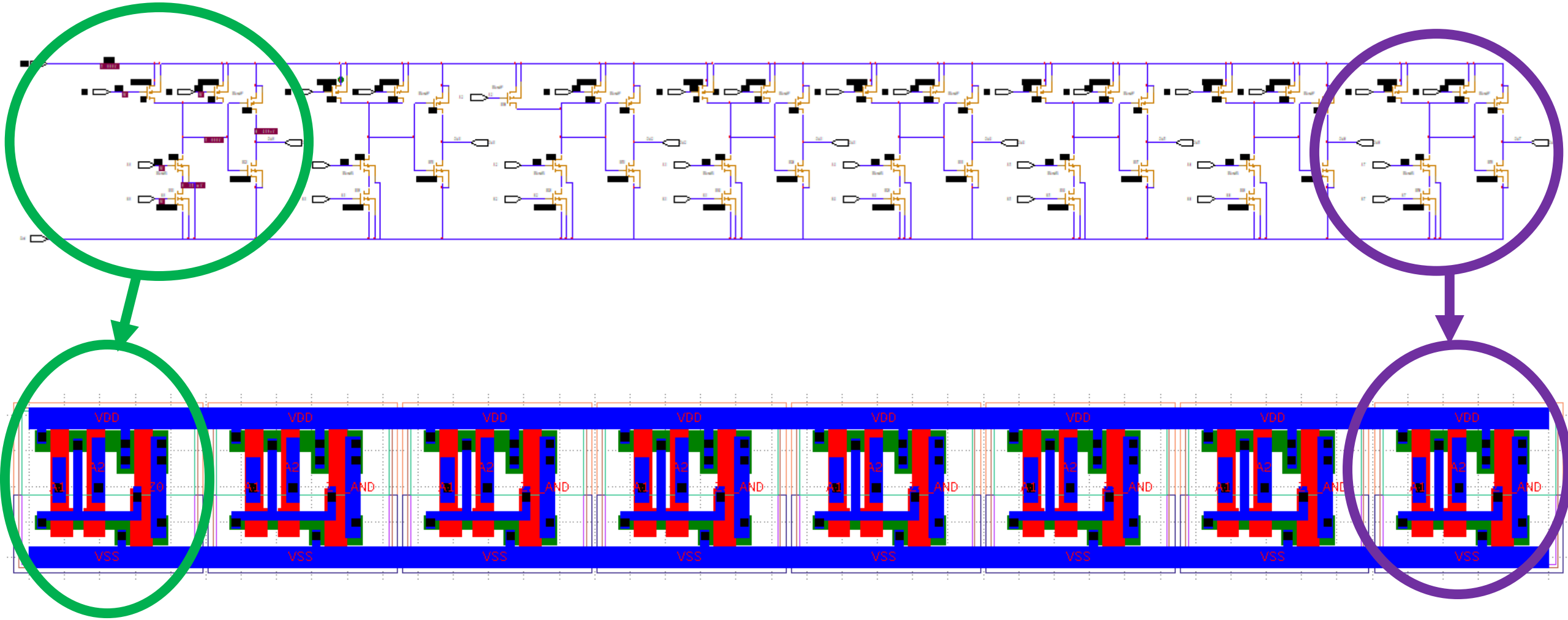
ALU - physical top view



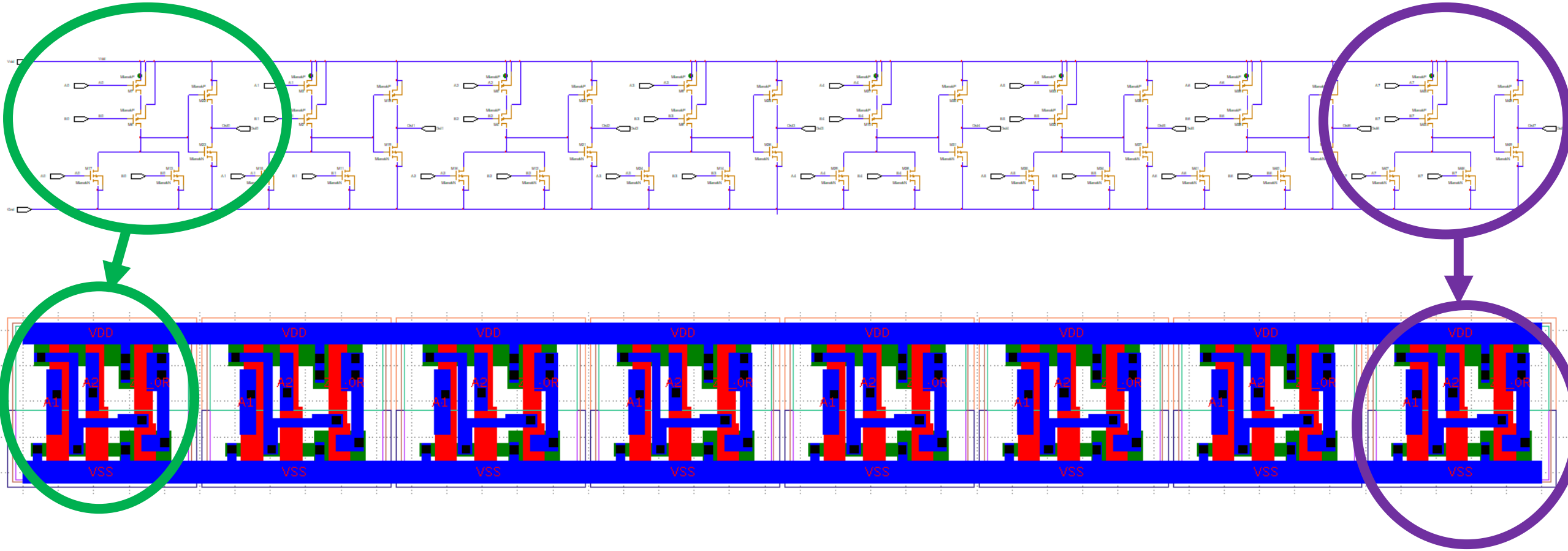
INVERTER 8-bit



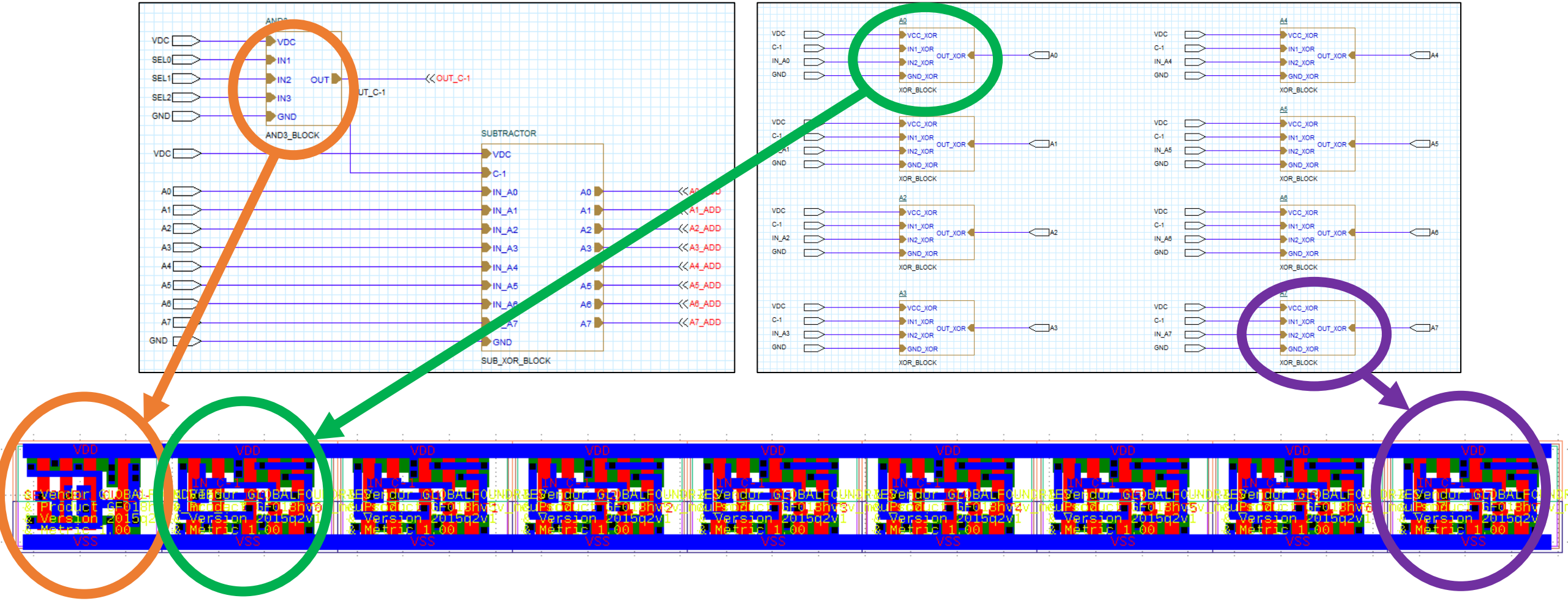
AND 8-bit



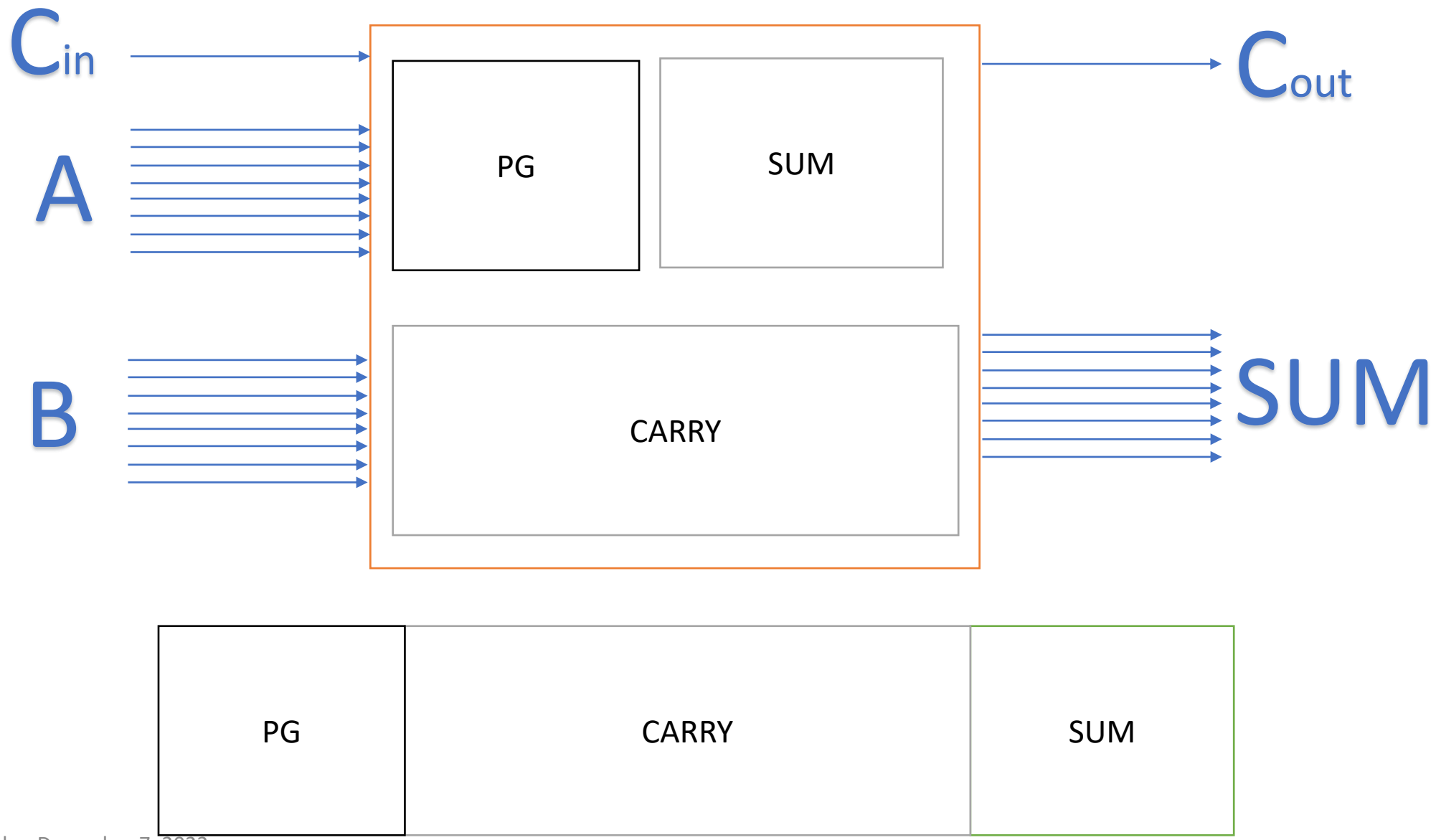
OR 8-bit



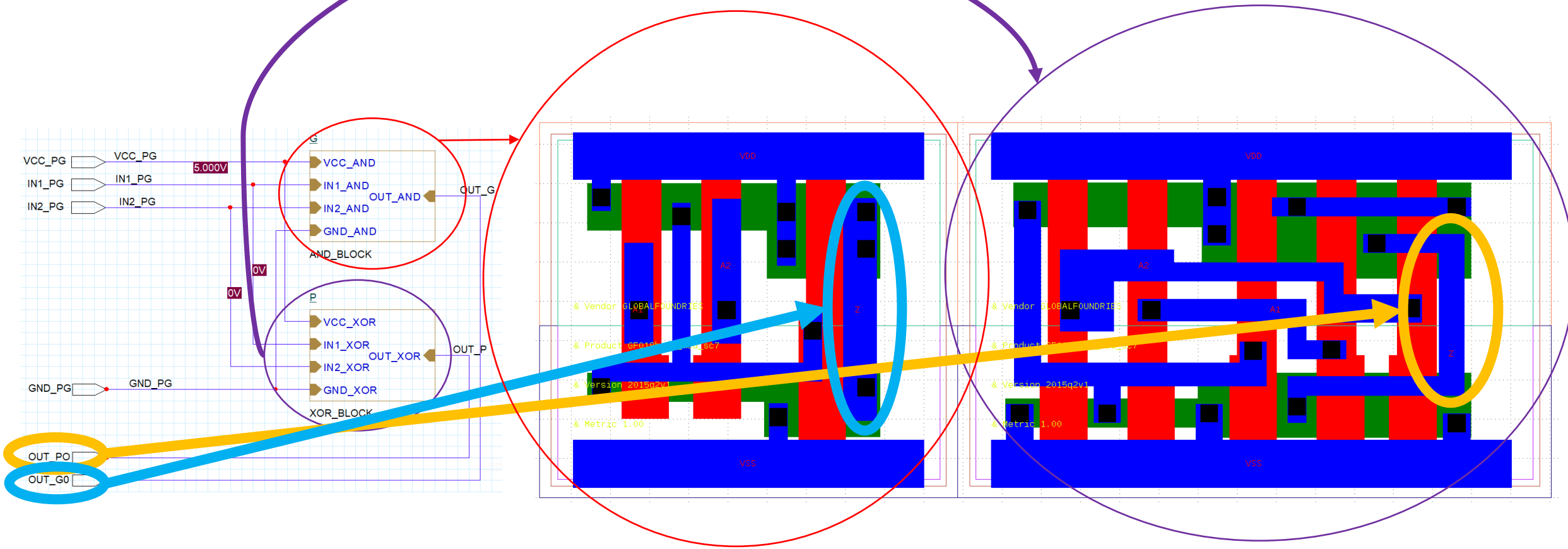
SUBTRACTOR 8-bit (Pseudo subtractor?)



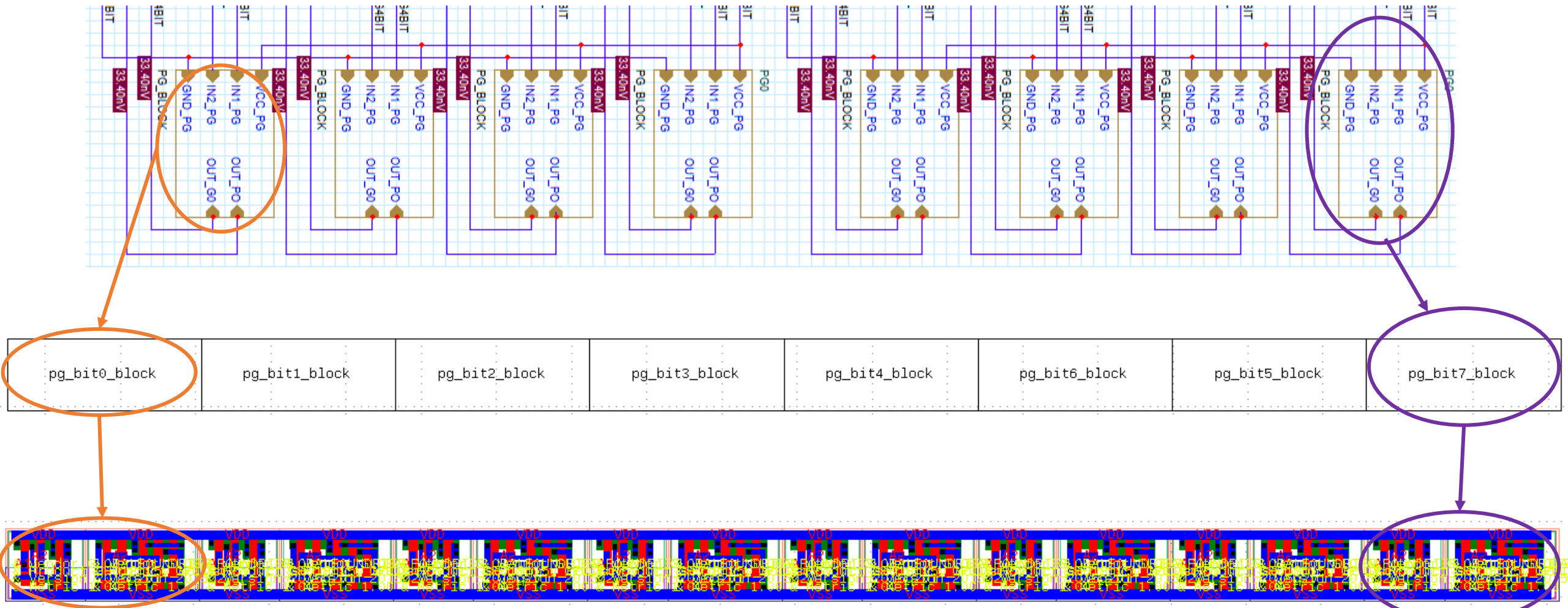
ADDER 8-bit



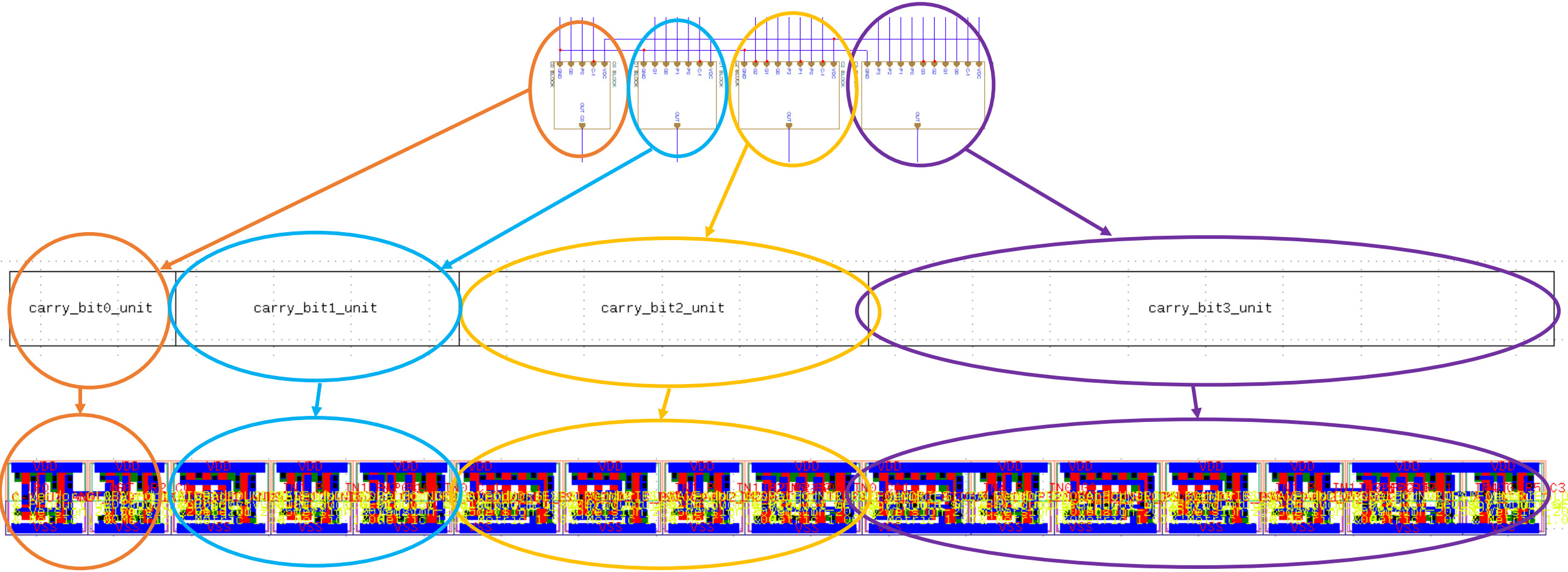
Propagate and Generate 1-bit



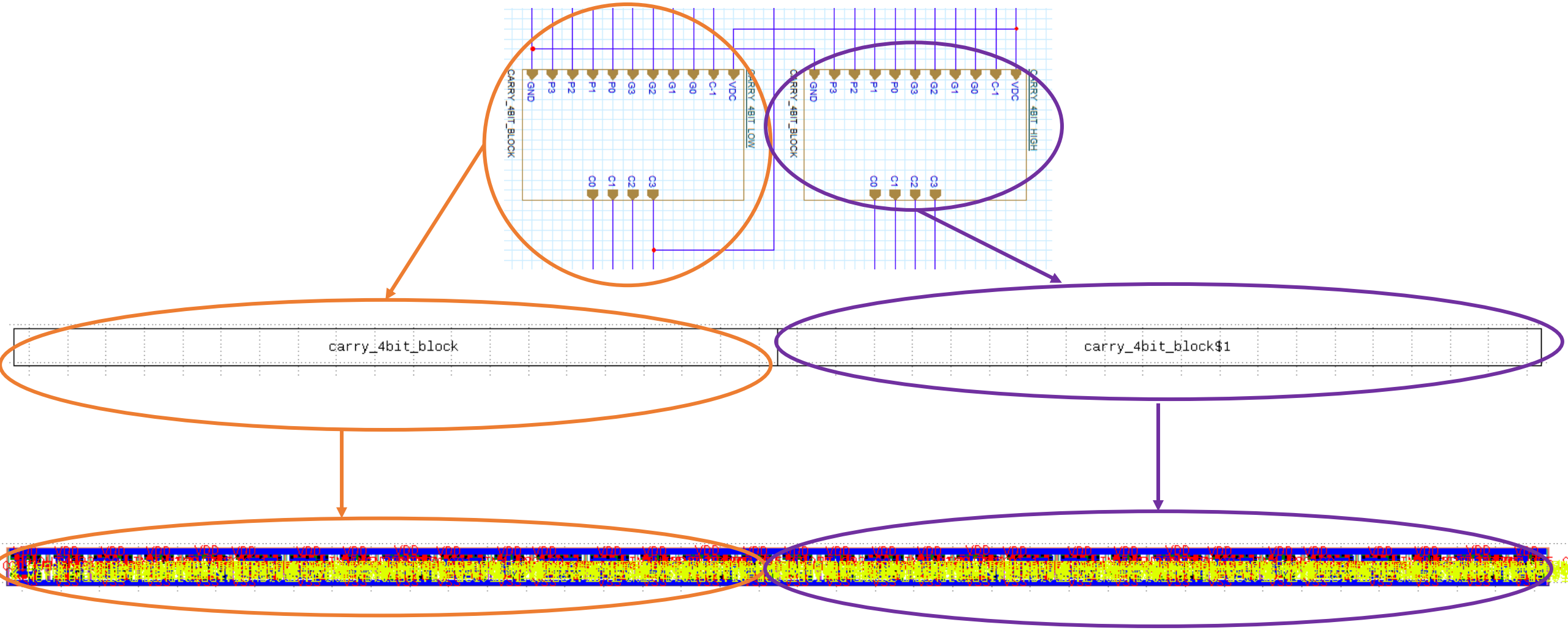
Propagate-Generate 4-bit



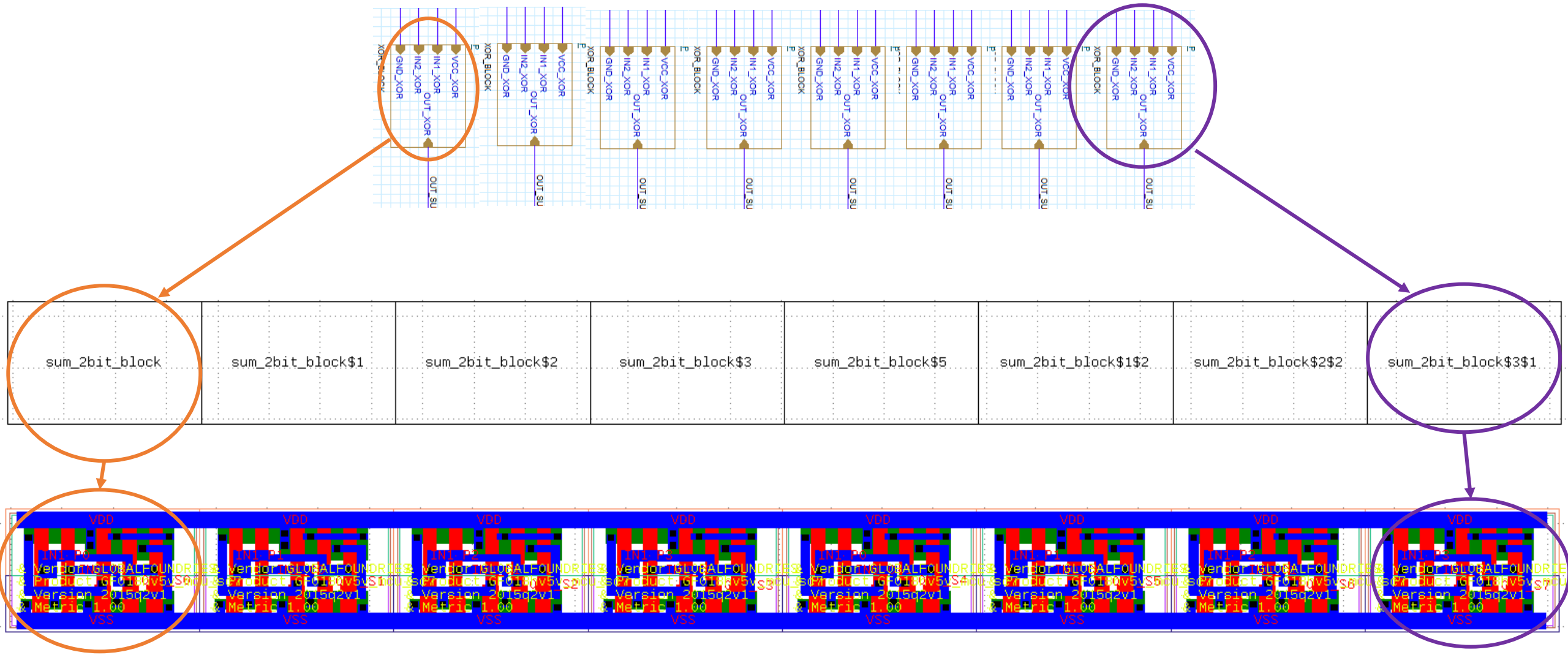
Carry Generator 4-bit



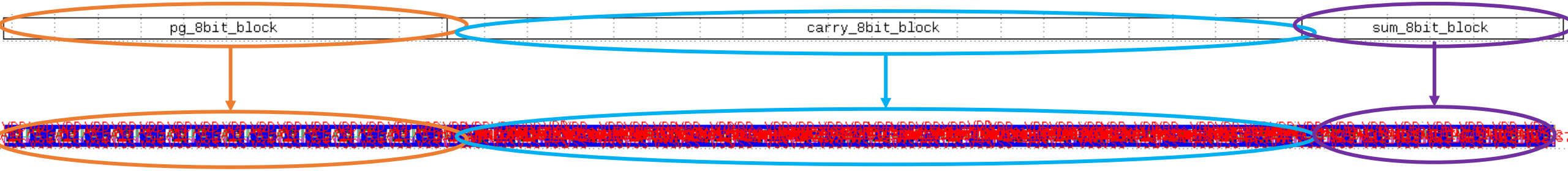
Carry Generator 8-bit



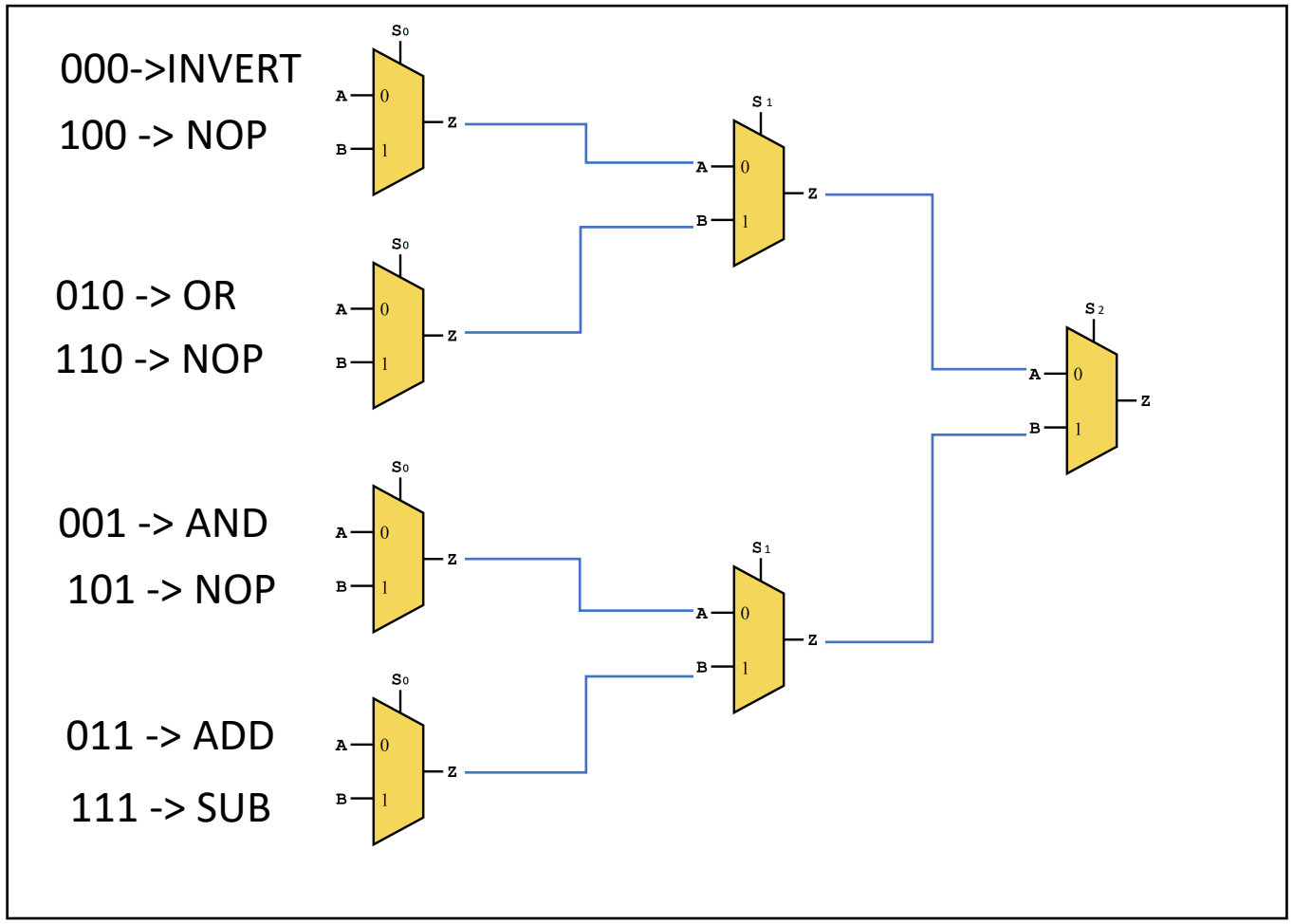
Sum 8-bit

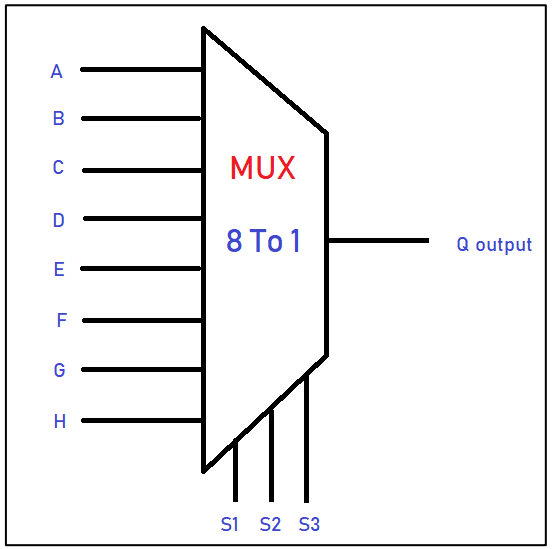

sum_2bit_block
sum_2bit_block$1
sum_2bit_block$2
sum_2bit_block$3
sum_2bit_block$5
sum_2bit_block$1$2
sum_2bit_block$2$2
sum_2bit_block$3$1
XOR_BLOCK
GND_XOR
IN2_XOR
IN1_XOR
VCC_XOR
OUT_XOR
VDD
VSS

Adder 8-bit

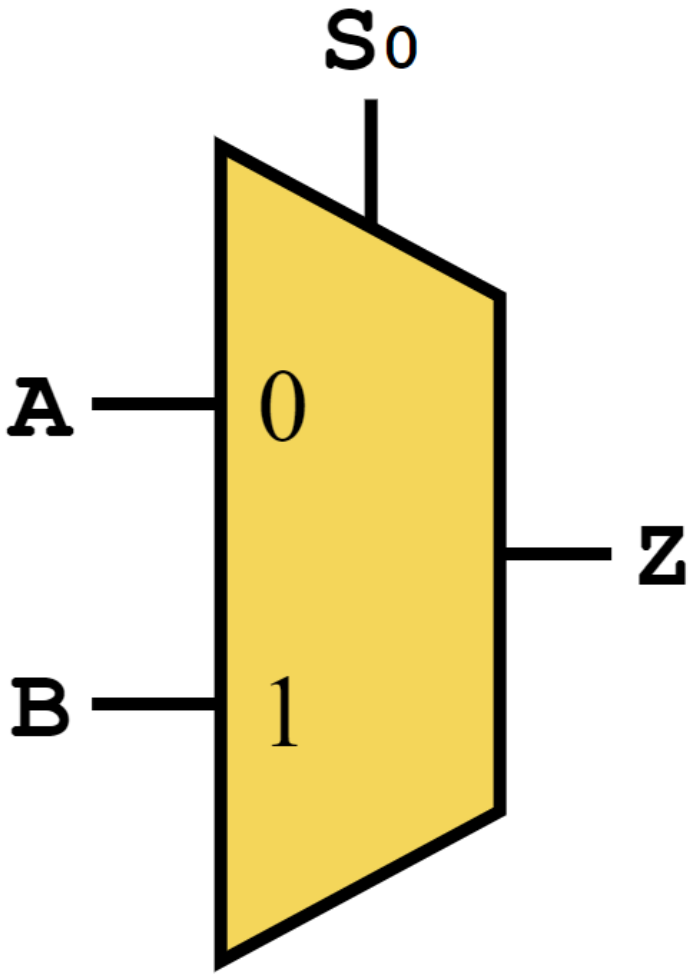


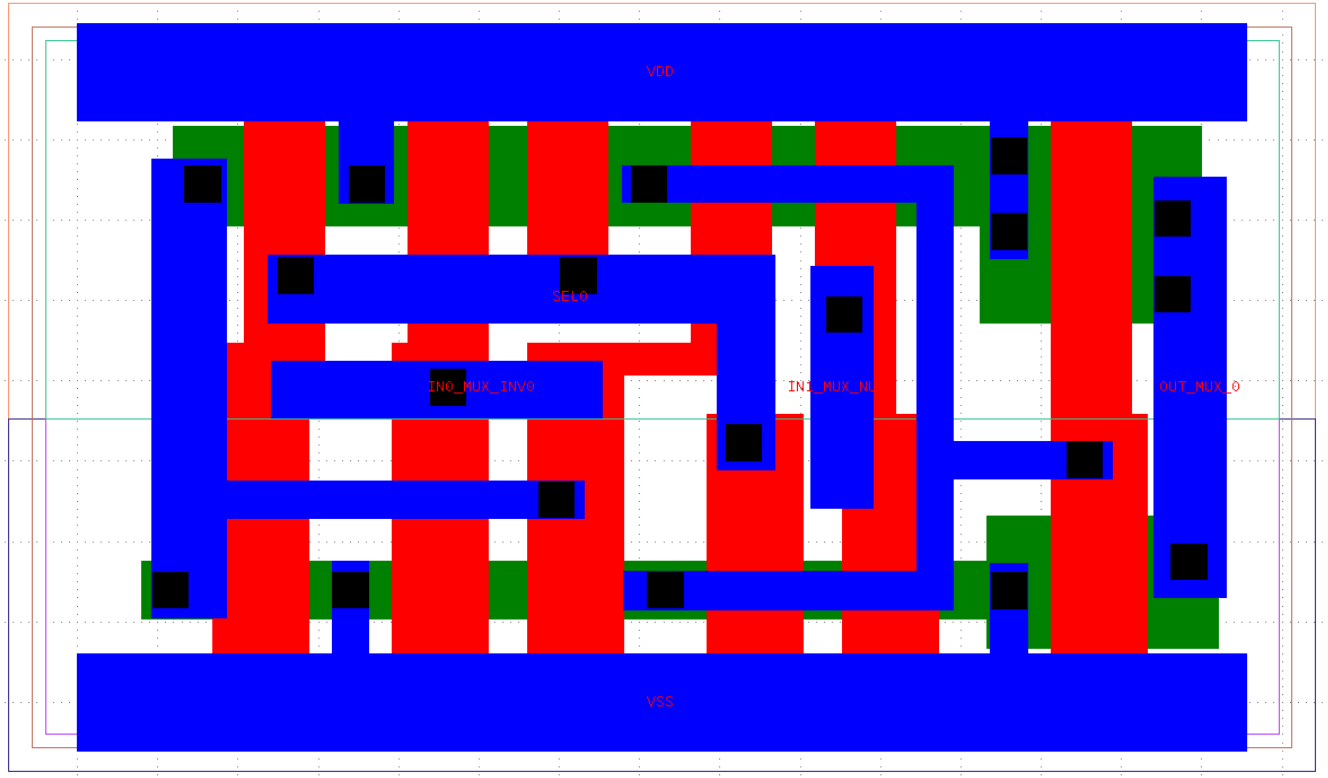
MUX


000->INVERT
100 -> NOP
010 -> OR
110 -> NOP
001 -> AND
101 -> NOP
011 -> ADD
111 -> SUB
S0
S1
S2
A
B
Z
0
1

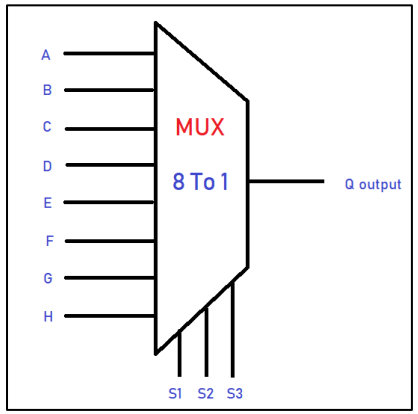

A
B
C
D
E
F
G
H
MUX
8 To 1
Q output
S1
S2
S3

MUX 2x1

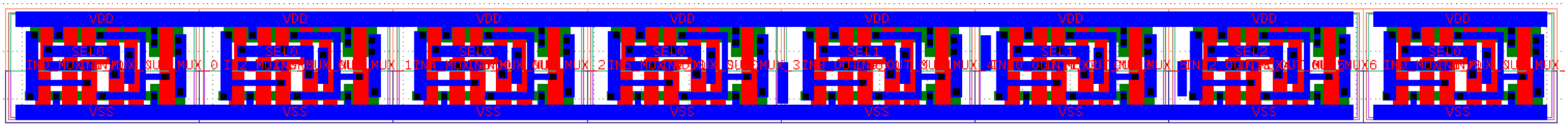




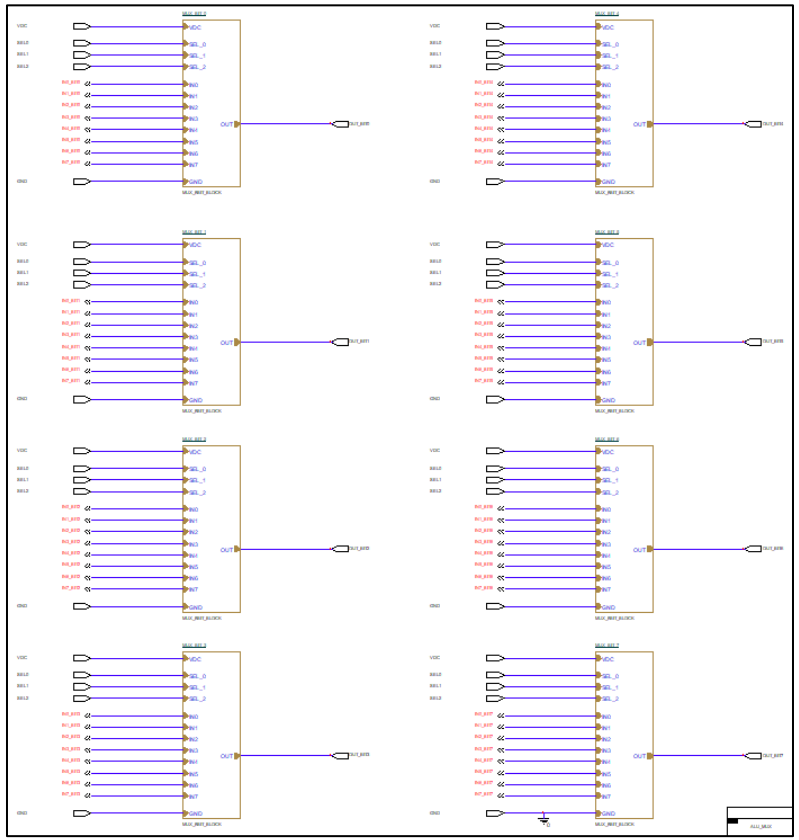
MUX 8x1

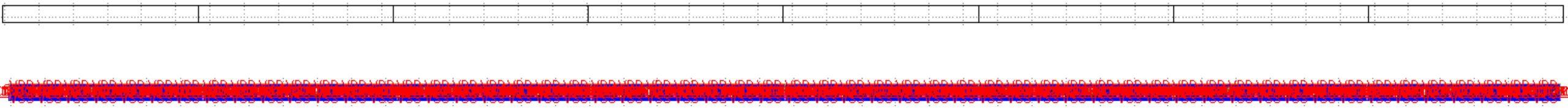


mux_2bit_block	mux_2bit_block$1	mux_2bit_block$2	mux_2bit_block$3	mux_2bit_block$4	mux_2bit_block$5	mux_2bit_block$6	mux_2bit_block$14

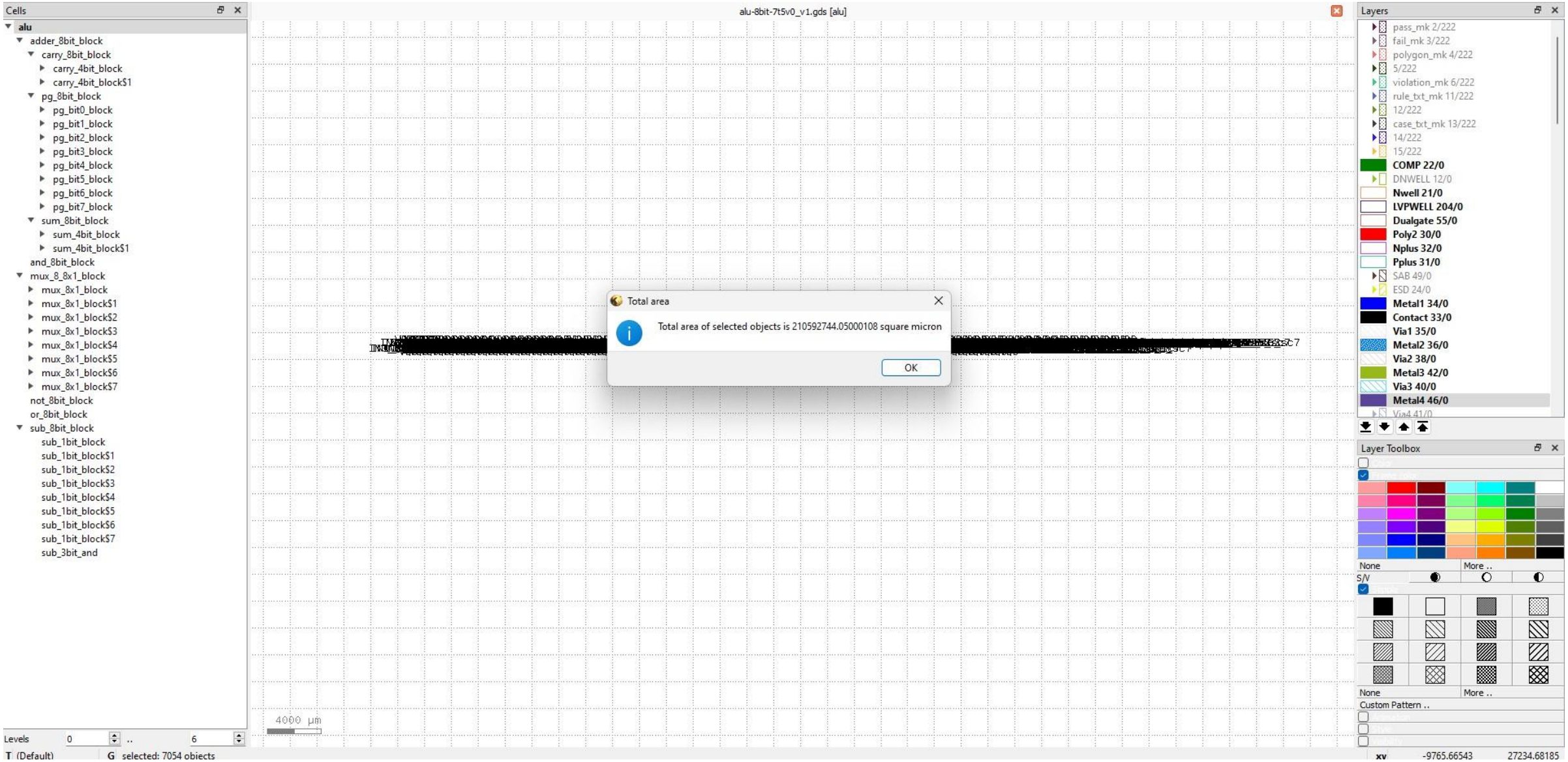


8(8x1) MUX

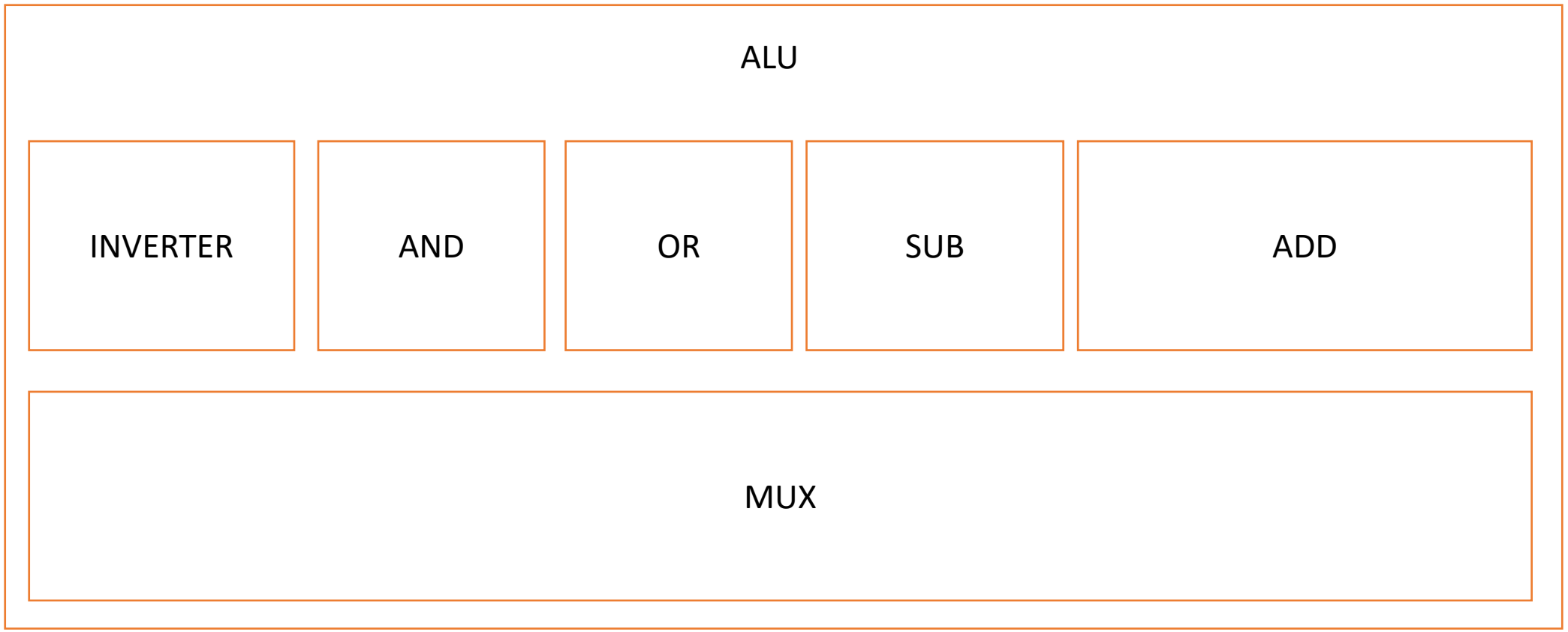


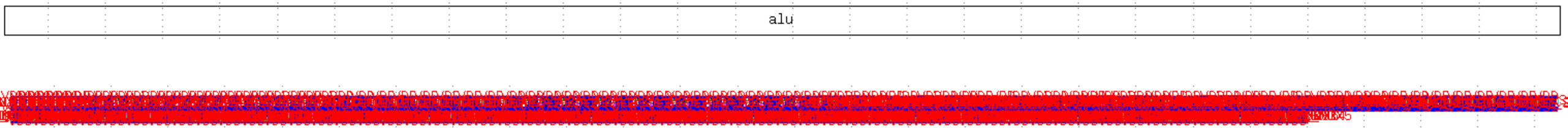


Area


Cells
alu
adder_8bit_block
carry_8bit_block
carry_4bit_block
carry_4bit_block$1
pg_8bit_block
pg_bit0_block
pg_bit1_block
pg_bit2_block
pg_bit3_block
pg_bit4_block
pg_bit5_block
pg_bit6_block
pg_bit7_block
sum_8bit_block
sum_4bit_block
sum_4bit_block$1
and_8bit_block
mux_8_8x1_block
mux_8x1_block
mux_8x1_block$1
mux_8x1_block$2
mux_8x1_block$3
mux_8x1_block$4
mux_8x1_block$5
mux_8x1_block$6
mux_8x1_block$7
not_8bit_block
or_8bit_block
sub_8bit_block
sub_1bit_block
sub_1bit_block$1
sub_1bit_block$2
sub_1bit_block$3
sub_1bit_block$4
sub_1bit_block$5
sub_1bit_block$6
sub_1bit_block$7
sub_3bit_and
Levels
0
6
T (Default)
G selected: 7054 objects
alu-8bit-7t5v0_v1.gds [alu]
Total area
Total area of selected objects is 210592744.05000108 square micron
OK
4000 µm
Layers
pass_mk 2/222
fail_mk 3/222
polygon_mk 4/222
5/222
violation_mk 6/222
rule_txt_mk 11/222
12/222
case_txt_mk 13/222
14/222
15/222
COMP 22/0
DNWELL 12/0
Nwell 21/0
LVPWELL 204/0
Dualgate 55/0
Poly2 30/0
Nplus 32/0
Pplus 31/0
SAB 49/0
ESD 24/0
Metal1 34/0
Contact 33/0
Via1 35/0
Metal2 36/0
Via2 38/0
Metal3 42/0
Via3 40/0
Metal4 46/0
Via4 41/0
Layer Toolbox
None
More ..
S/V
None
More ..
Custom Pattern ..
xy
-9765.66543
27234.68185

Complete ALU

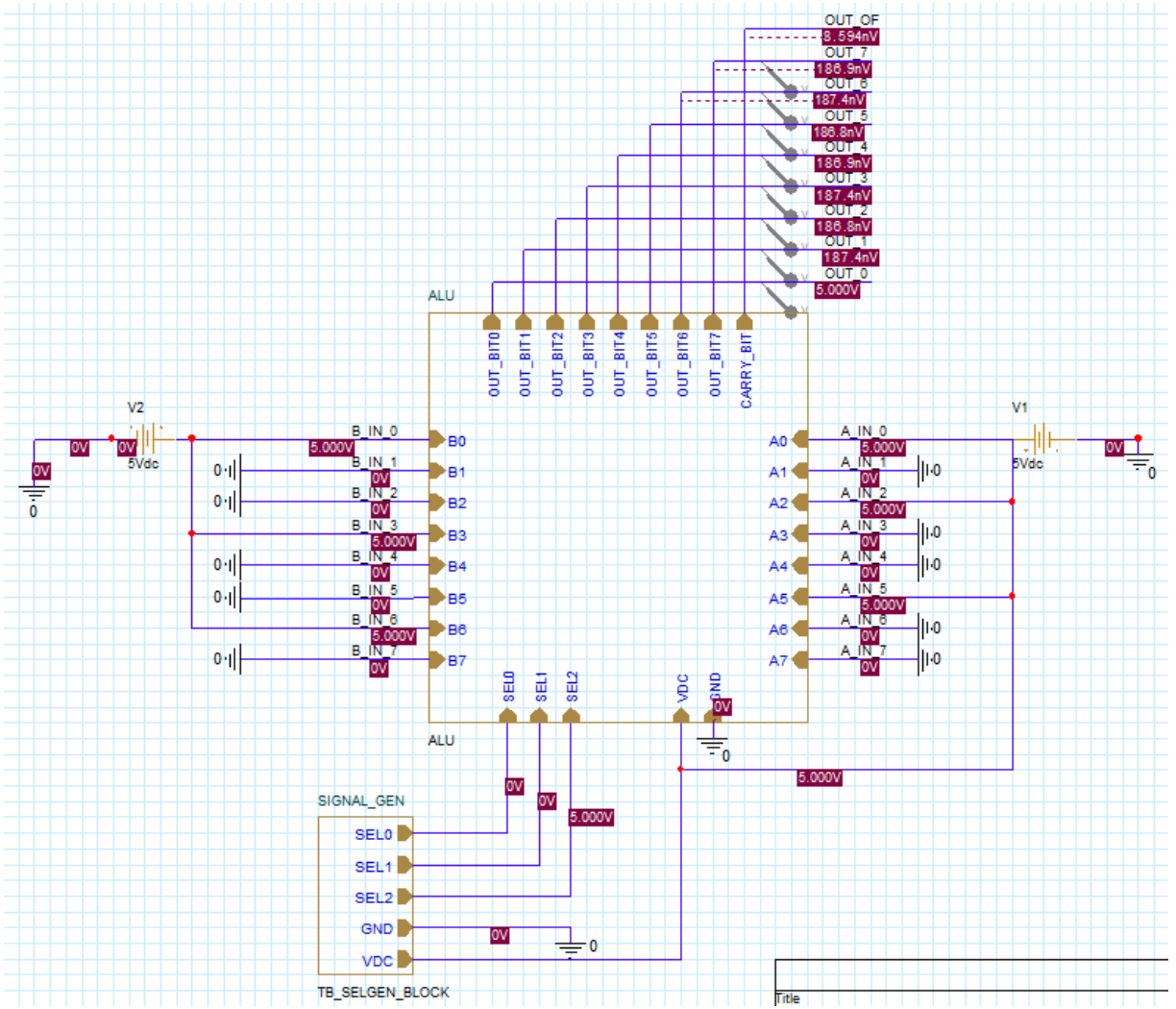




Test setup

B = 73

1 0 0 1 0 0 1 0



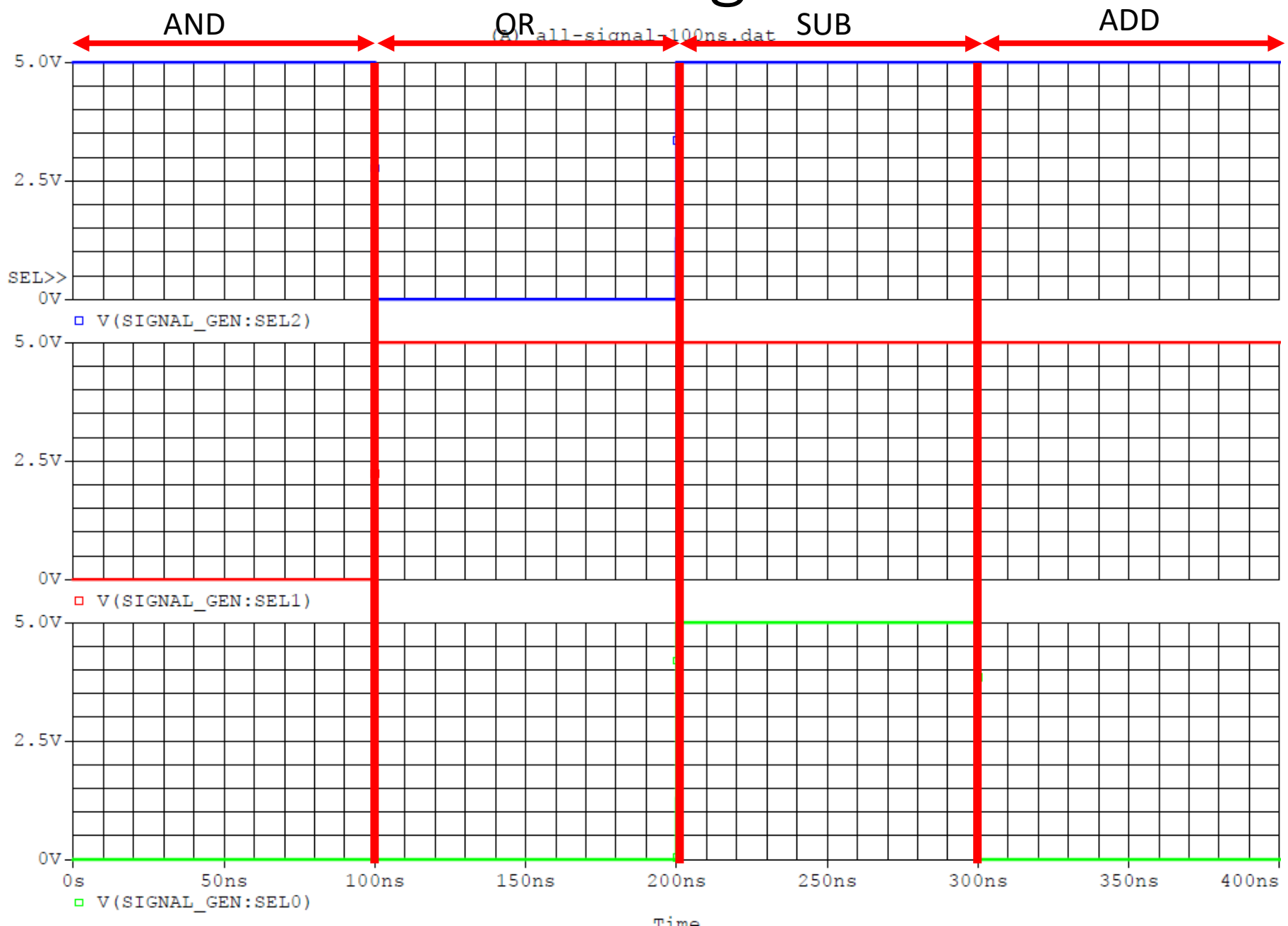
1 0 1 0 0 0 1 0 0

A = 37

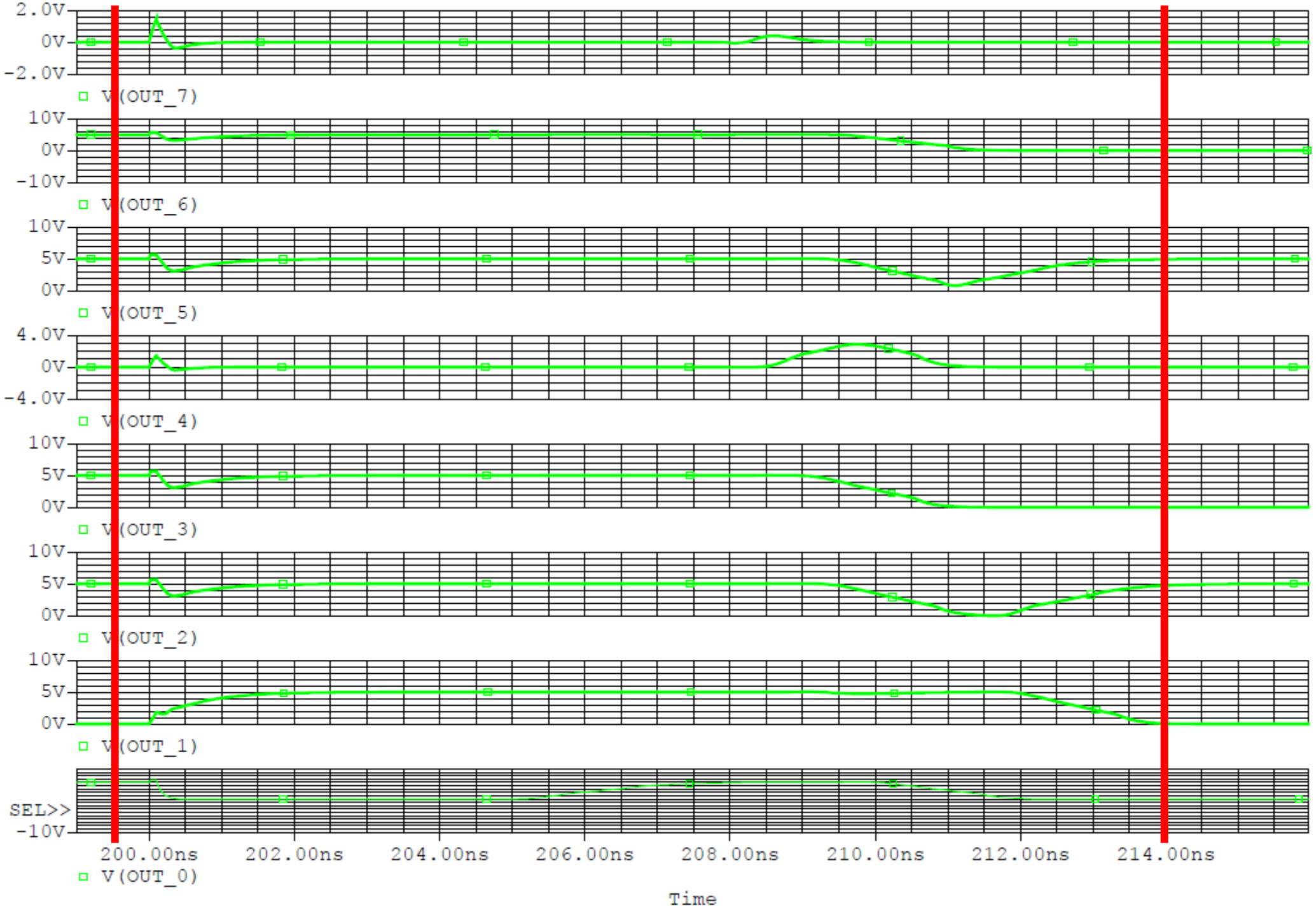
Input data configuration and output

BIT	7	6	5	4	3	2	1	0
B=37	0	0	1	0	0	1	0	1
A=73	0	1	0	0	1	0	0	1
G	0	0	0	0	0	0	0	1
P	0	1	1	0	1	1	0	0
C0								1
C1							0	
C2						0		
C3					0			
C4				0				
C5			0					
C6		0						
C7	0							
INVERT(EXP)	1	0	1	1	0	1	1	0
INVERT(OBSERVED)	1	0	1	1	0	1	1	0
ADD (EXP)	**0**	**1**	**1**	**0**	**1**	**1**	**1**	**0**
ADD (OBSERVED)	**0**	**1**	**1**	**0**	**1**	**1**	**1**	**0**
SUB (EXP)	0	0	1	0	0	1	0	0
SUB (OBSERVED)	0	0	1	0	0	1	0	0
OR (EXP)	0	1	1	0	1	1	0	1
OR (OBSERVED)	0	1	1	0	1	1	0	1
AND(EXP)	0	0	0	0	0	0	0	1
AND (OBSERVED)	0	0	0	0	0	0	0	1

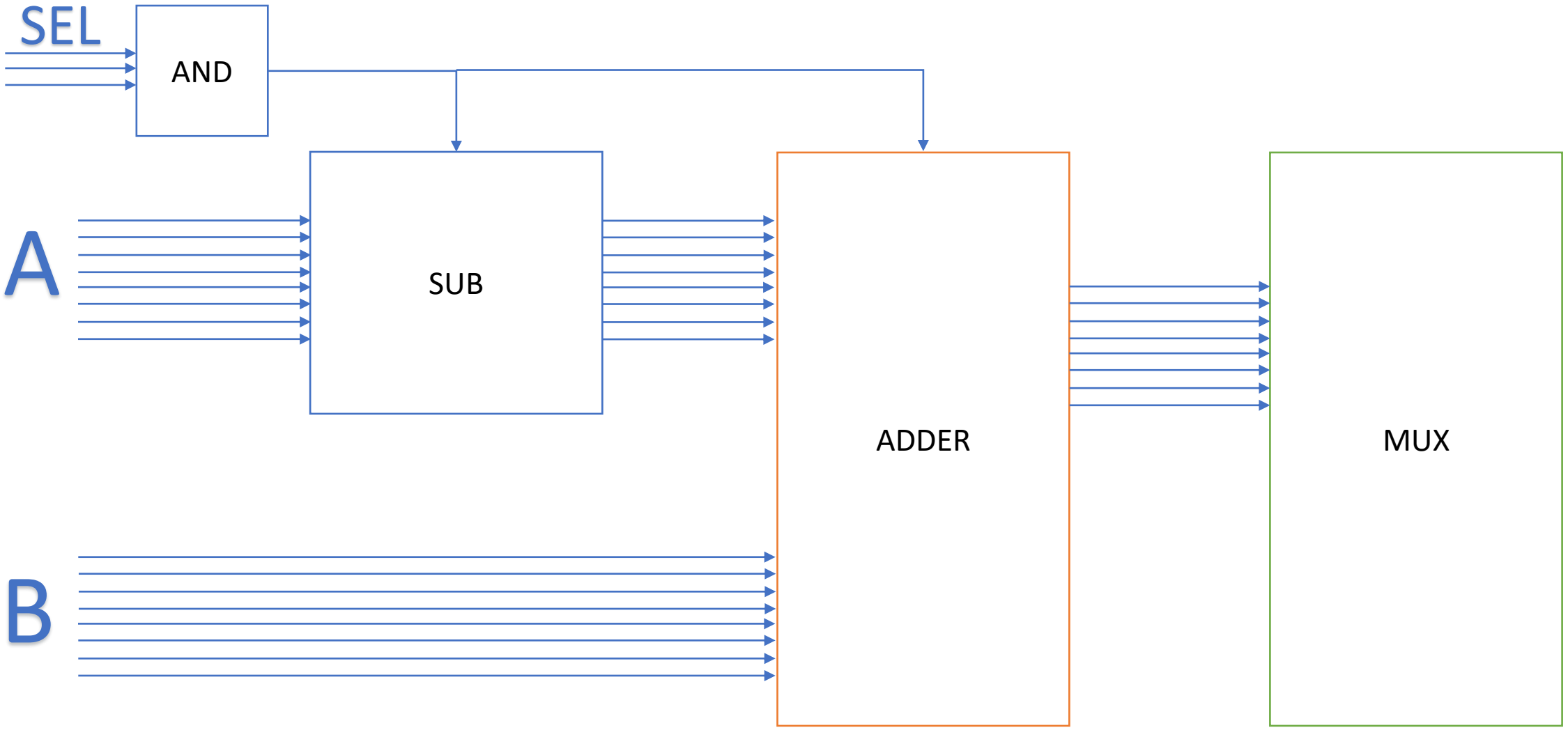
SELECT Signals



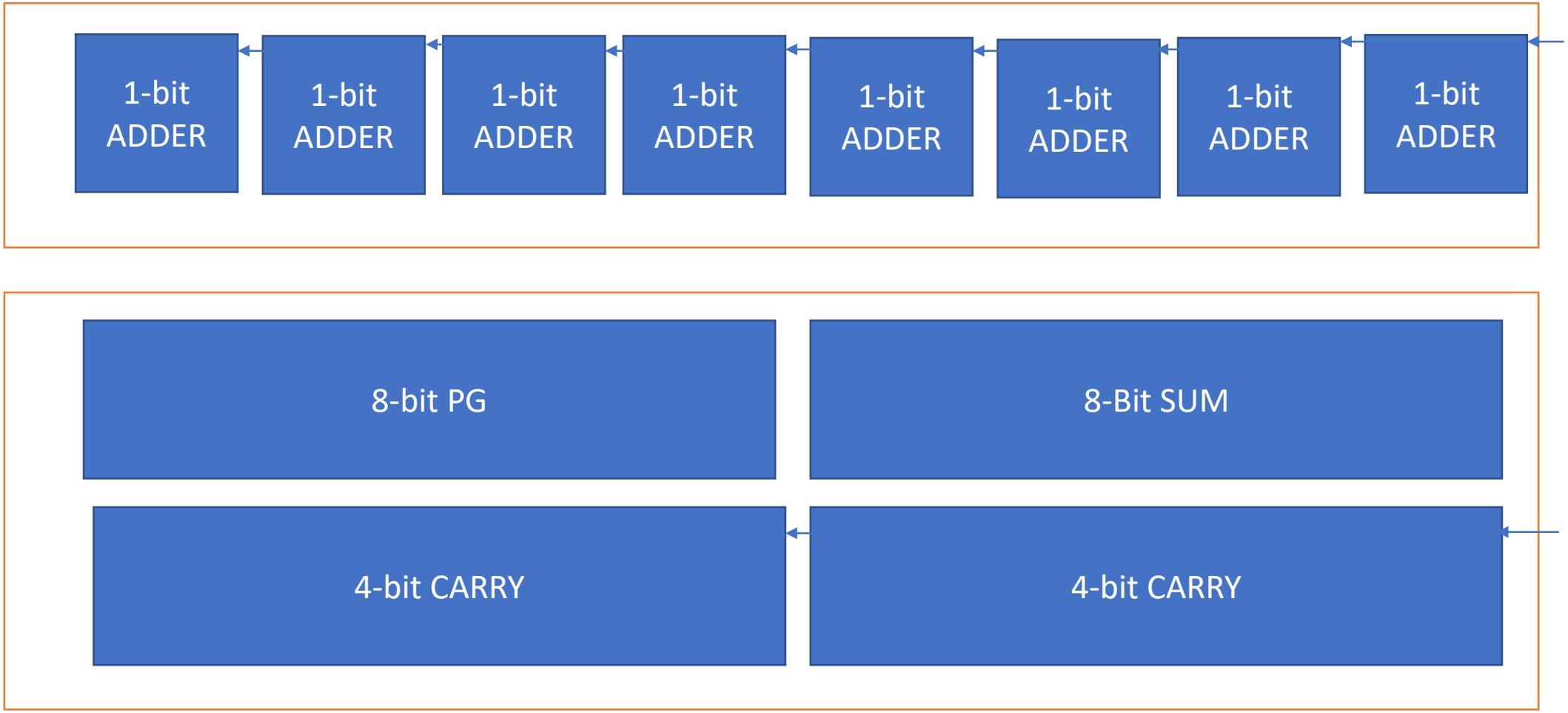

AND
OR
SUB
ADD
V(OUT_7)
V(OUT_6)
V(OUT_5)
V(OUT_4)
SEL>>
V(OUT_3)
V(OUT_2)
V(OUT_1)
V(OUT_0)
4.0V
0V
-4.0V
10V
-10V
5.0V
-5.0V
0s
50ns
100ns
150ns
200ns
250ns
300ns
350ns
400ns
Time


2.0V
0V
-2.0V
V(OUT_7)
10V
0V
-10V
V(OUT_6)
10V
5V
0V
V(OUT_5)
4.0V
0V
-4.0V
V(OUT_4)
10V
5V
0V
V(OUT_3)
10V
5V
0V
V(OUT_2)
10V
5V
0V
V(OUT_1)
SEL>>
-10V
200.00ns
202.00ns
204.00ns
206.00ns
208.00ns
210.00ns
212.00ns
214.00ns
V(OUT_0)
Time

Critical path



Ripple carry vs Carry Lookahead



Thank you

ELEG/CPEG 448