

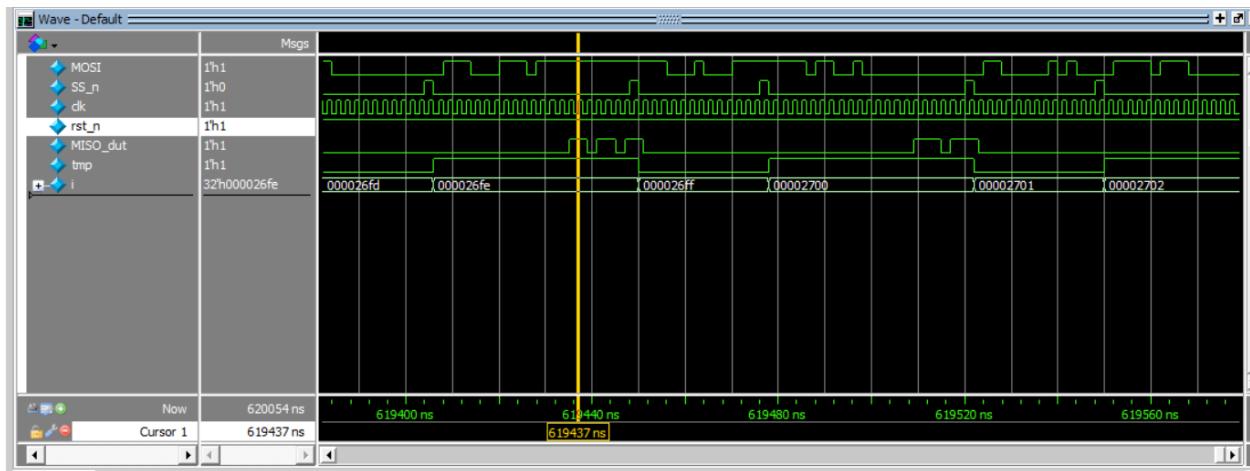
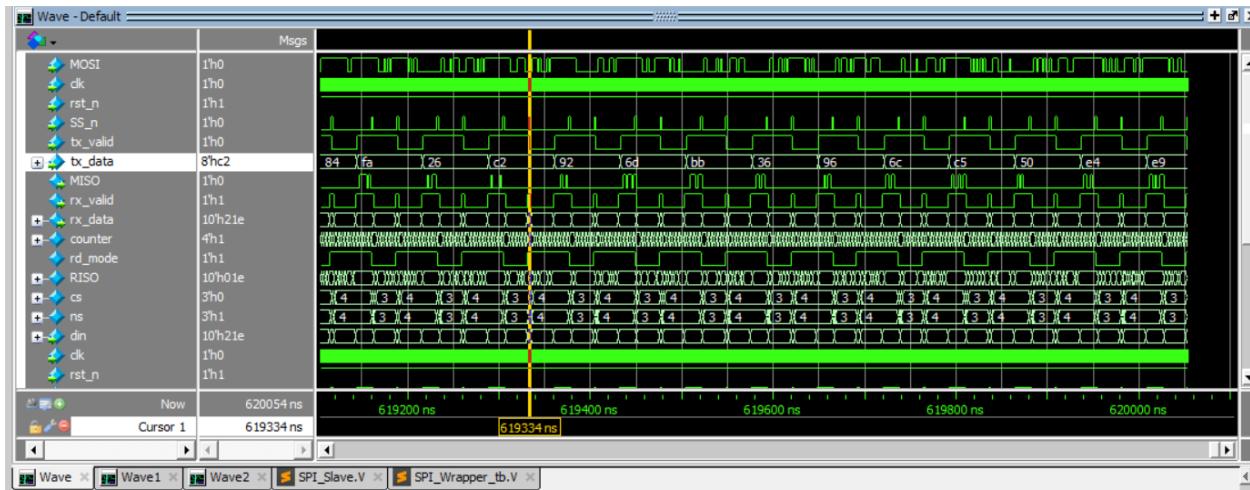
# SPI Slave with Single Port RAM Project:

Name	Team
Mina Ehab Mansour Salib	Core

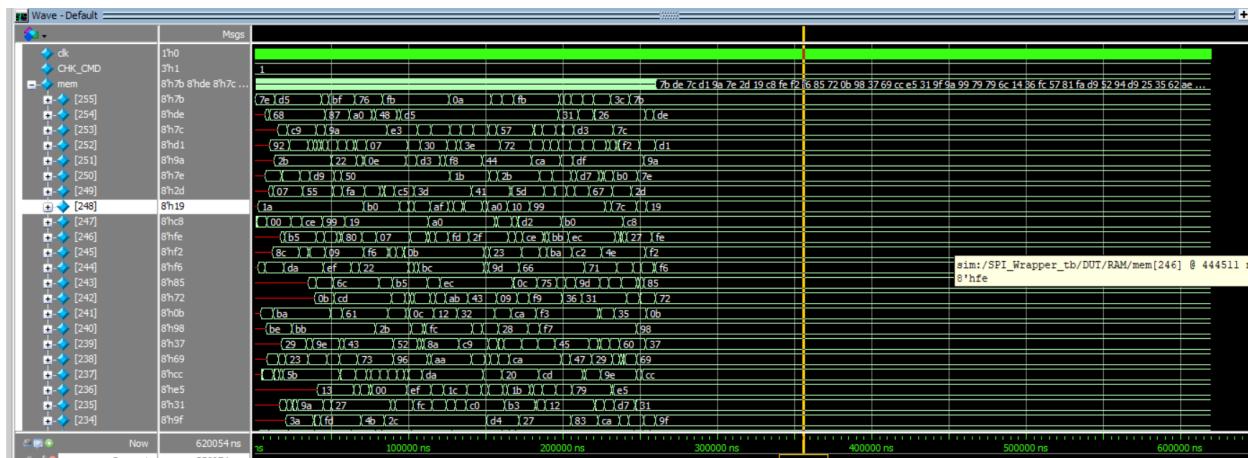
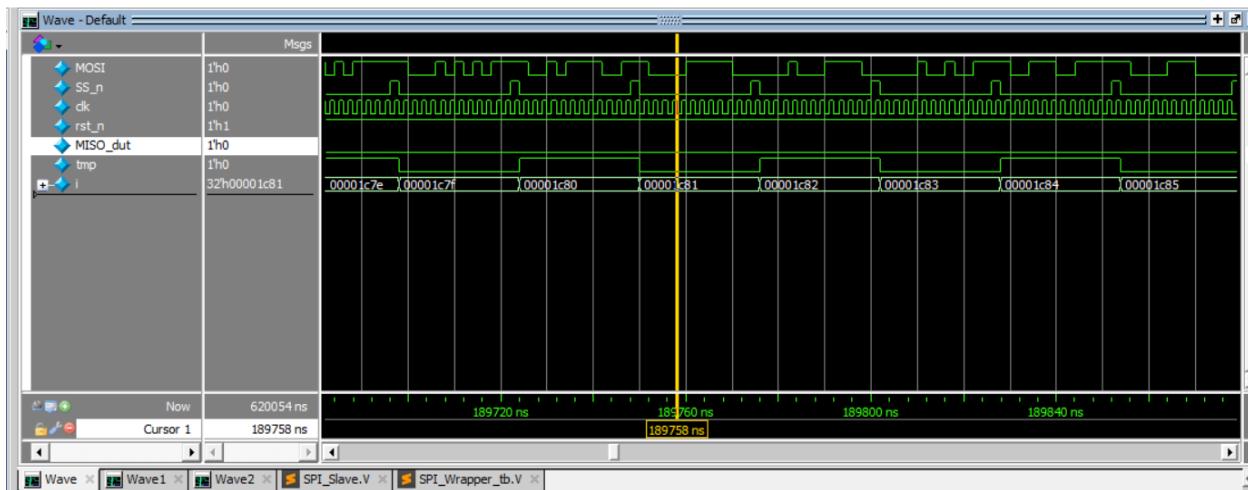
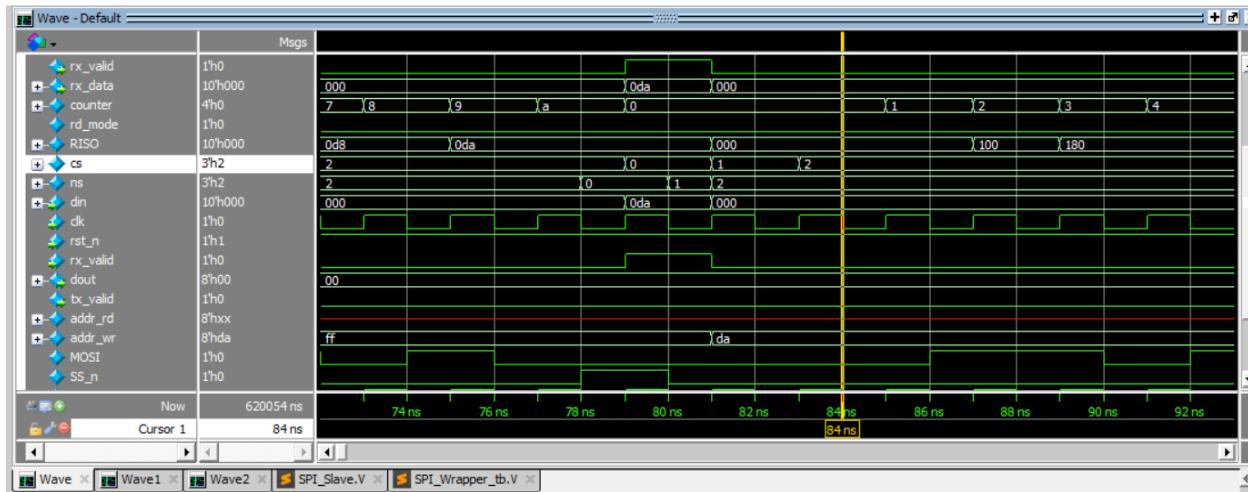
**Submitted to:** ENG. Kareem Waseem

## Simulations:

### Read operation

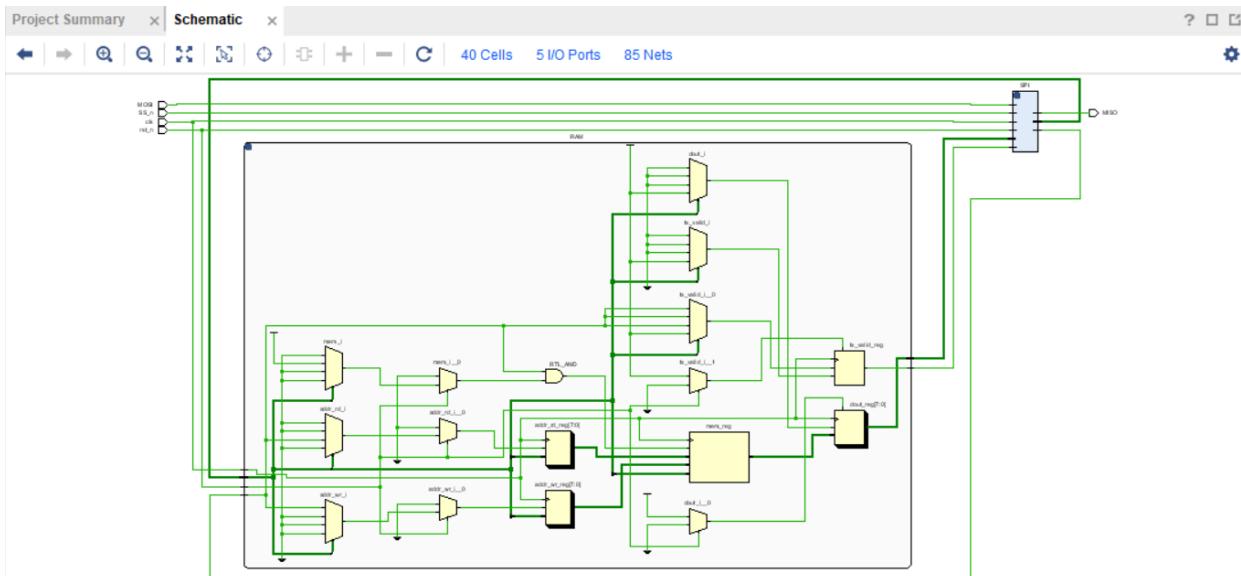
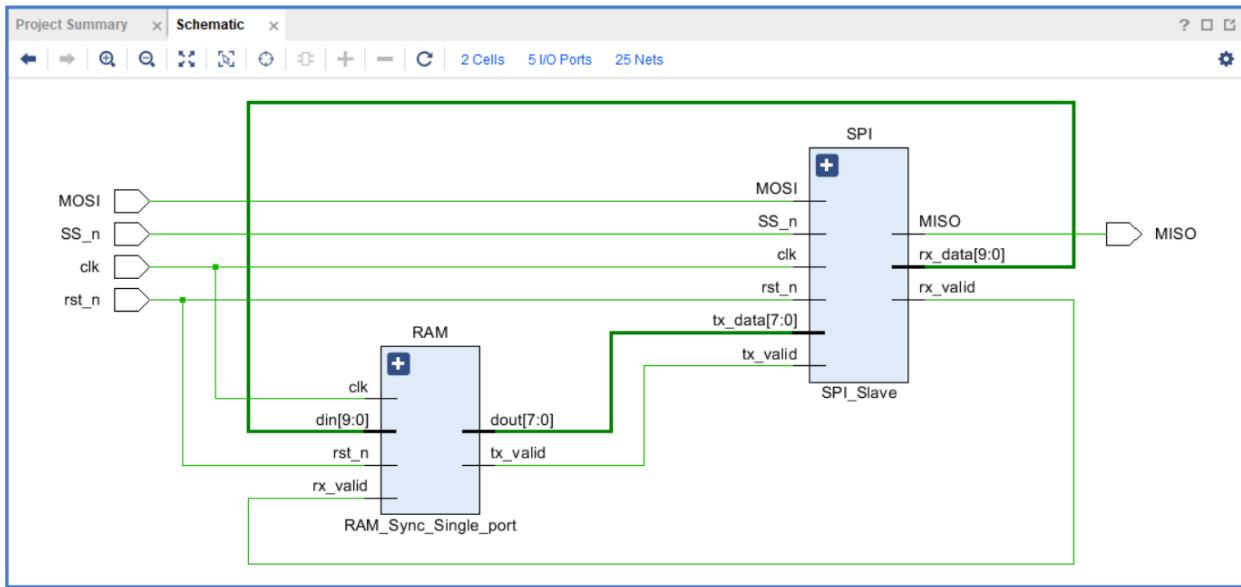


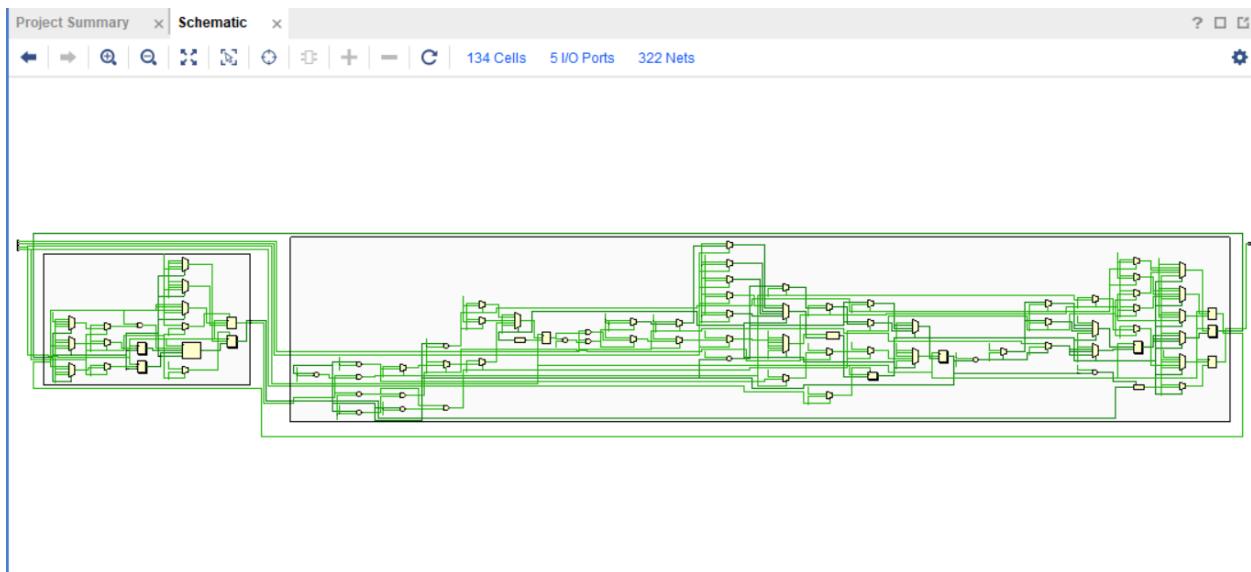
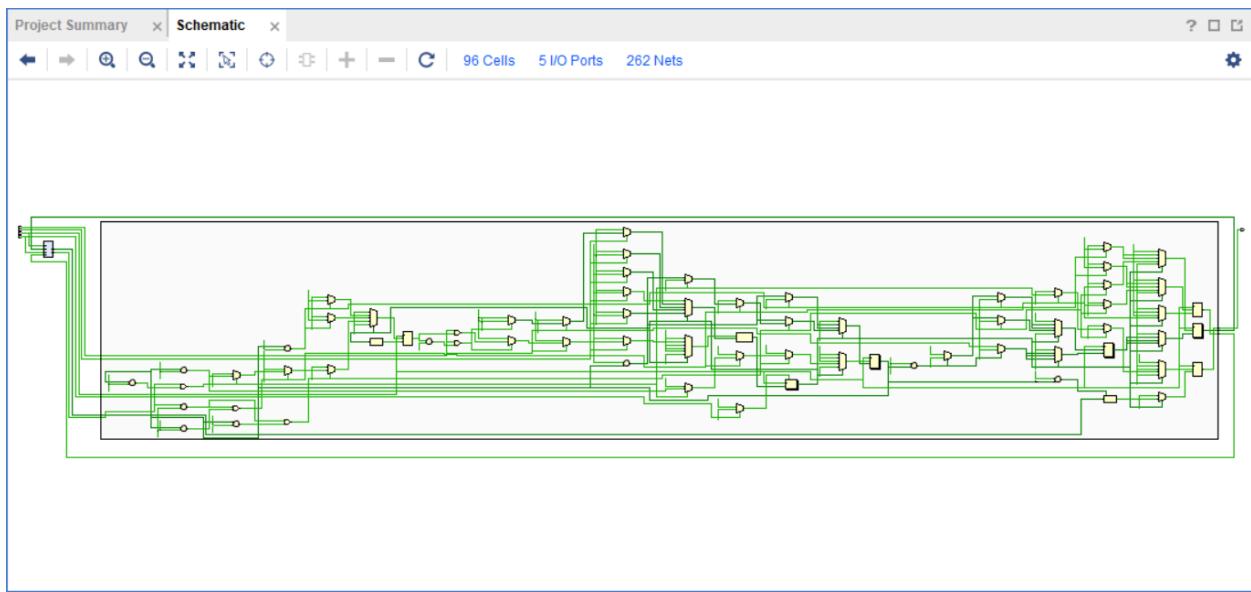
## Write operation



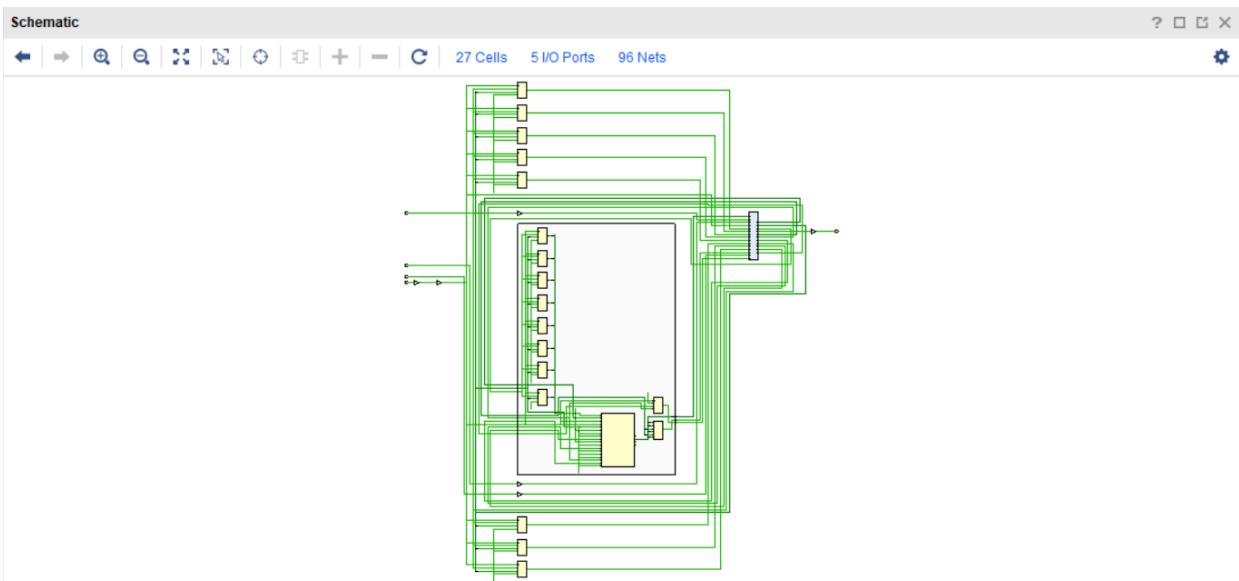
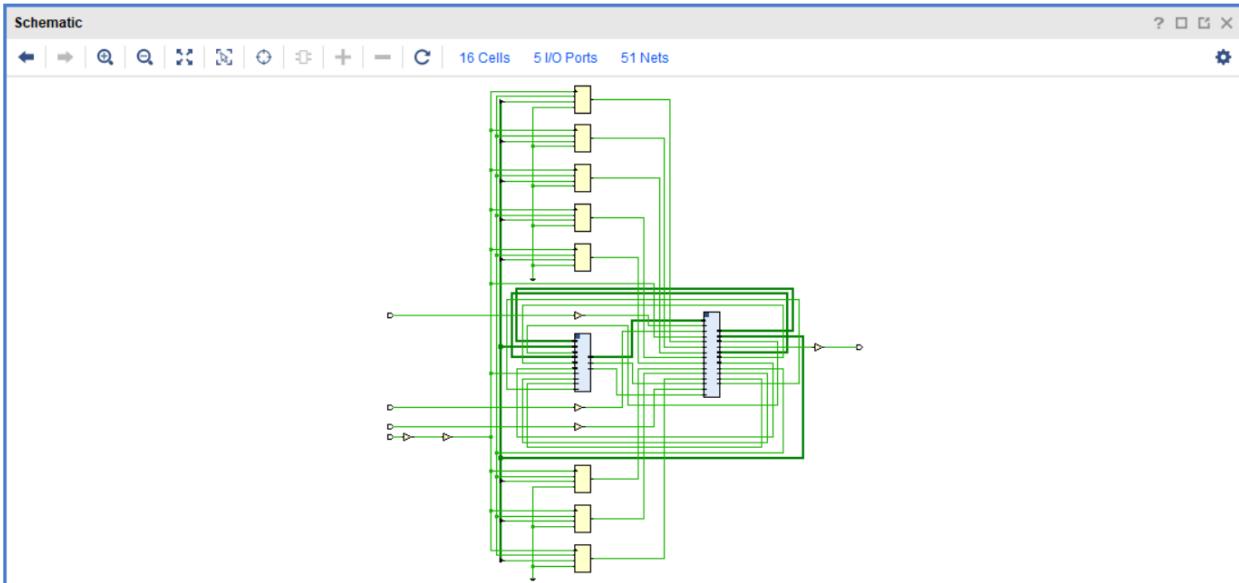
Gray Encoding:

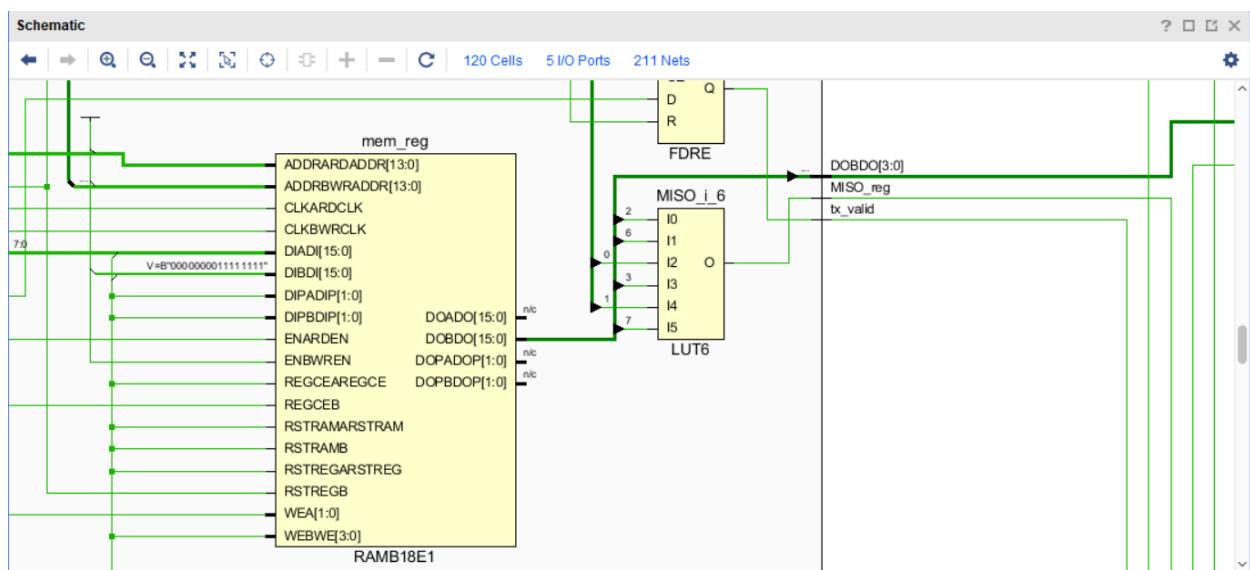
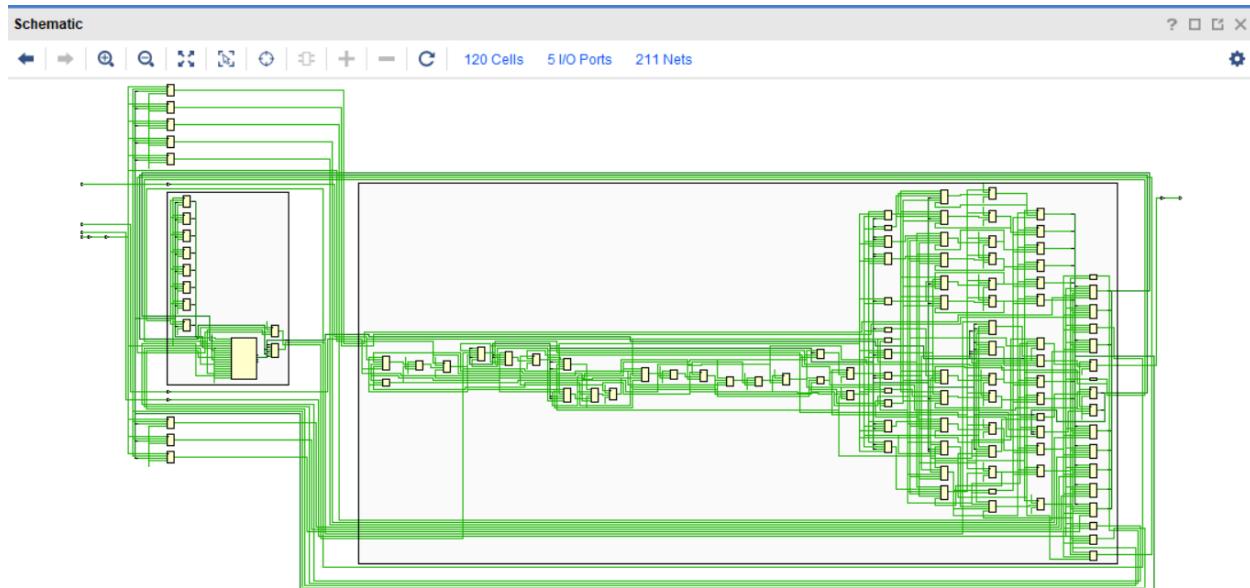
Elaborated design schematic:





## Synthesized Design:





Schematic × synth\_1\_synth\_synthesis\_report\_0 - synth\_1 × D:/2nd year/Digital design/SPI\_Sync/SPI\_Project/SPI\_Project.runs/synth\_1/SPI\_Wrapper.vds

Q | H | ← | → | X | D | I | X | // | ■ | ? | Read-only | |

```

22 INFO: [Synth 8-6157] synthesizing module 'SPI_Wrapper' [D:/2nd year/Digital design/SPI_Sync/SPI_Wrapper.V:1]
23 Parameter IDLE bound to: 3'b000
24 Parameter CHK_CMD bound to: 3'b001
25 Parameter WRITE bound to: 3'b010
26 Parameter READ_ADD bound to: 3'b011
27 Parameter READ_DATA bound to: 3'b100
28 INFO: [Synth 8-6157] synthesizing module 'SPI_Slave' [D:/2nd year/Digital design/SPI_Sync/SPI_Slave.V:1]
29 Parameter IDLE bound to: 3'b000
30 Parameter CHK_CMD bound to: 3'b001
31 Parameter WRITE bound to: 3'b010
32 Parameter READ_ADD bound to: 3'b011
33 Parameter READ_DATA bound to: 3'b100
34 INFO: [Synth 8-5534] Detected attribute (* fsm_encoding = "gray" *) [D:/2nd year/Digital design/SPI_Sync/SPI_Slave.V:21]
35 INFO: [Synth 8-155] case statement is not full and has no default [D:/2nd year/Digital design/SPI_Sync/SPI_Slave.V:32]
36 INFO: [Synth 8-155] case statement is not full and has no default [D:/2nd year/Digital design/SPI_Sync/SPI_Slave.V:62]
37 INFO: [Synth 8-6155] done synthesizing module 'SPI_Slave' (1#) [D:/2nd year/Digital design/SPI_Sync/SPI_Slave.V:1]
38 INFO: [Synth 8-6157] synthesizing module 'RAM_Sync_Single_port' [D:/2nd year/Digital design/SPI_Sync/RAM.V:1]
39 Parameter MEM_DEPTH bound to: 256 - type: integer
40 Parameter ADDR_SIZE bound to: 8 - type: integer
41 INFO: [Synth 8-6155] done synthesizing module 'RAM_Sync_Single_port' (2#) [D:/2nd year/Digital design/SPI_Sync/RAM.V:1]
42 INFO: [Synth 8-6155] done synthesizing module 'SPI_Wrapper' (3#) [D:/2nd year/Digital design/SPI_Sync/SPI_Wrapper.V:1]
43 -----
44 Finished RTL Elaboration : Time (s): cpu = 00:00:01 ; elapsed = 00:00:02 . Memory (MB): peak = 409.887 ; gain = 153.184
< ----- >

```

Schematic × synth\_1\_synth\_synthesis\_report\_0 - synth\_1 × D:/2nd year/Digital design/SPI\_Sync/SPI\_Project/SPI\_Project.runs/synth\_1/SPI\_Wrapper.vds

Q | H | ← | → | X | D | I | X | // | ■ | ? | Read-only | |

```

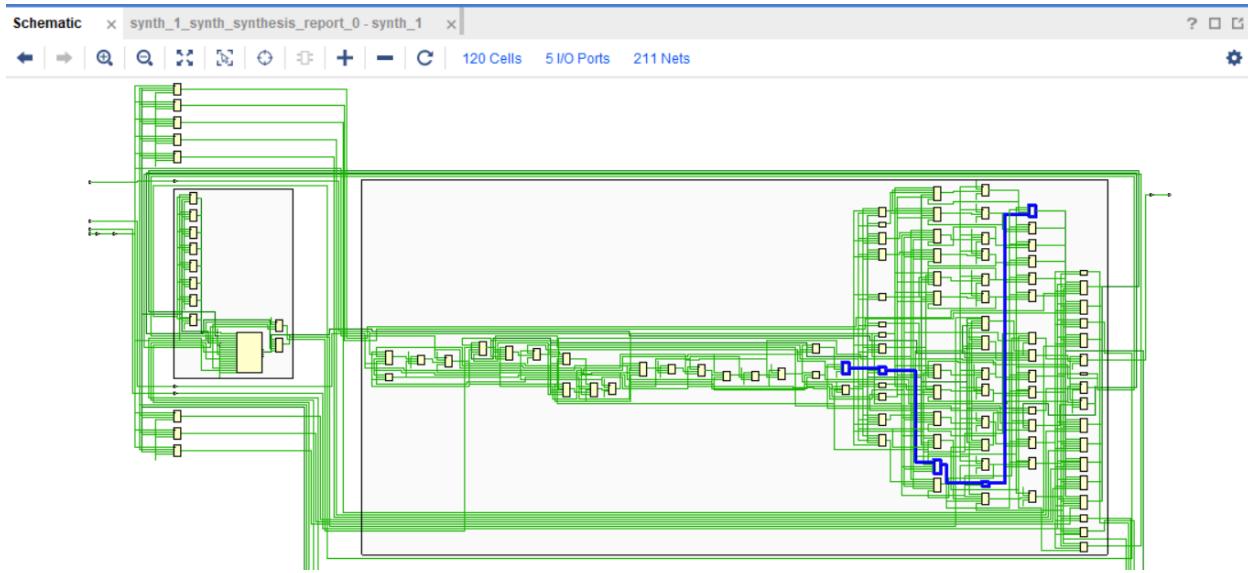
91 Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:11 ; elapsed = 00:00:24 . Memory (MB): peak = 760.379 ; gain = 503.676
92 -----
93 INFO: [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'SPI_Slave'
94 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
95 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
96 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
97 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
98 -----
99      State |          New Encoding |          Previous Encoding
100 -----
101     IDLE |           000 |           000
102   CHK_CMD |           001 |           001
103    WRITE |           011 |           010
104  READ_ADD |           010 |           011
105 READ_DATA |           111 |           100
106 -----
107 INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'SPI_Slave'
108 WARNING: [Synth 8-327] inferring latch for variable 'FSM_gray_ns_reg' [D:/2nd year/Digital design/SPI_Sync/SPI_Slave.V:34]
109 INFO: [Synth 8-6430] The Block RAM mem_reg may get memory collision error if read and write address collide. Use attribute (* rw_addr_collision= "y")
110 -----
111 Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:11 ; elapsed = 00:00:24 . Memory (MB): peak = 760.379 ; gain = 503.676
112 -----
113

```

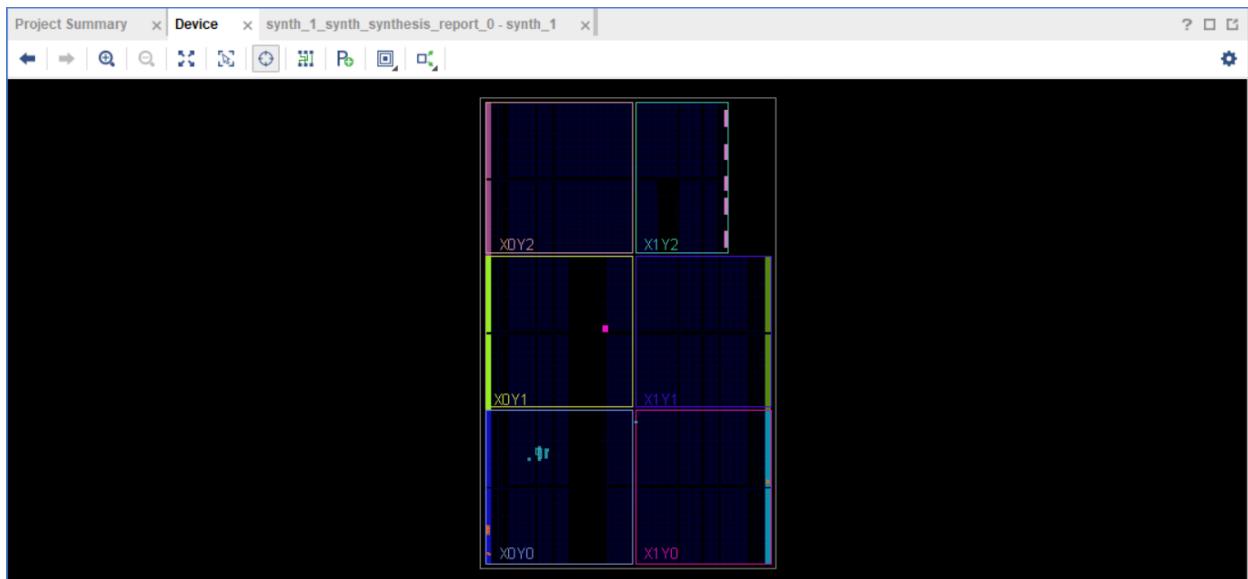
Tcl Console Messages Log Reports Design Runs Timing × Debug

Q | H | ← | → | C | D | I | Design Timing Summary

Design Timing Summary						
General Information						
Timer Settings						
Design Timing Summary						
Clock Summary (1)						
>  Check Timing (16)						
>  Intra-Clock Paths						
Inter-Clock Paths						
Other Path Groups						
User Ignored Paths						
>  Unconstrained Paths						
All user specified timing constraints are met.						
Setup						
Worst Negative Slack (WNS):	5.784 ns	Worst Hold Slack (WHS):	0.150 ns	Pulse Width	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns		Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	
Total Number of Endpoints:	113	Total Number of Endpoints:	113	Total Number of Endpoints:	50	



## Implementation:



Design Timing Summary		
General Information	Setup	Hold
	Worst Negative Slack (WNS): <b>6.253 ns</b>	Worst Hold Slack (WHS): <b>0.081 ns</b>
	Total Negative Slack (TNS): <b>0.000 ns</b>	Total Hold Slack (THS): <b>0.000 ns</b>
	Number of Failing Endpoints: <b>0</b>	Number of Failing Endpoints: <b>0</b>
	Total Number of Endpoints: <b>113</b>	Total Number of Endpoints: <b>113</b>
All user specified timing constraints are met.		

Tcl Console Messages Log Reports Design Runs Power DRC Methodology Timing Utilization ? - \_

Q X % Hierarchy ⚙

**Hierarchy**

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	
N SPI_Wrapper	54	50	17	54	21	0.5	5	1	
RAM (RAM_Sync_Singl...)	1	9	3	1	0	0.5	0	0	
SPI (SPI_Slave)	53	33	16	53	20	0	0	0	

utilization\_1

IMPLEMENTED DESIGN - xc7a35ticpg236-1L (active)

Sour Nx ? — □ ⚙

**SPI\_Wrapper**

- > Nets (51)
- > Leaf Cells (15)
- > RAM (RAM\_Sync\_Singl...)
- > SPI (SPI\_Slave)

Pr ? — □ ✖

Select an object to see properties

Project Summary Device synth\_1\_synth\_synthesis\_report\_0 - synth\_1

**Bitstream Generation Completed**

Bitstream Generation successfully completed.

View Reports  
 Open Hardware Manager  
 Generate Memory Configuration File

Don't show this dialog again

OK Cancel

Tcl Console Messages Log Reports Design Runs Power DRC Methodology Timing Utilization ? - \_

Q X % Messages ⚙

**Synthesis (2 warnings)**

- [Synth 8-327] inferring latch for variable 'FSM\_gray\_ns\_reg' [SPI\_Slave.V:34]
- [Constraints 18-5210] No constraint will be written out.

**Implementation (1 warning)**

- > Write Bitstream (1 warning)
  - > DRC (1 warning)
    - > Physical Configuration (1 warning)
      - > Chip Level (1 warning)

Tcl Console Messages Log Reports Design Runs Power DRC Methodology Timing Utilization ? - \_

Q X % Messages ⚙

**Synthesis (2 warnings)**

- [Synth 8-327] inferring latch for variable 'FSM\_gray\_ns\_reg' [SPI\_Slave.V:34]
- [Constraints 18-5210] No constraint will be written out.

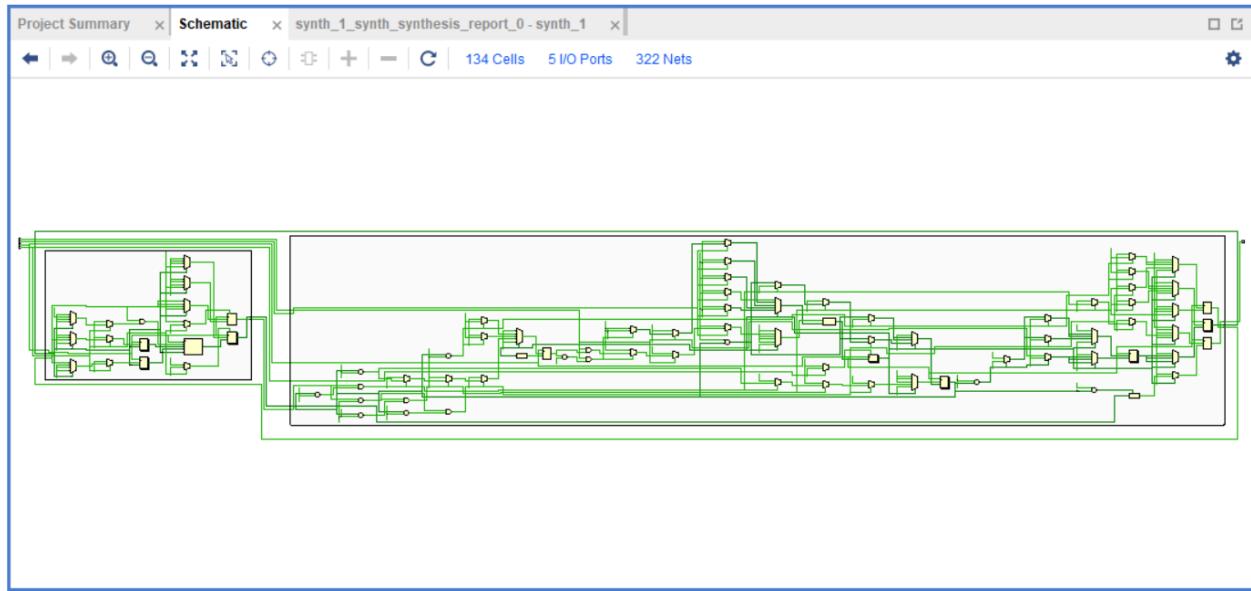
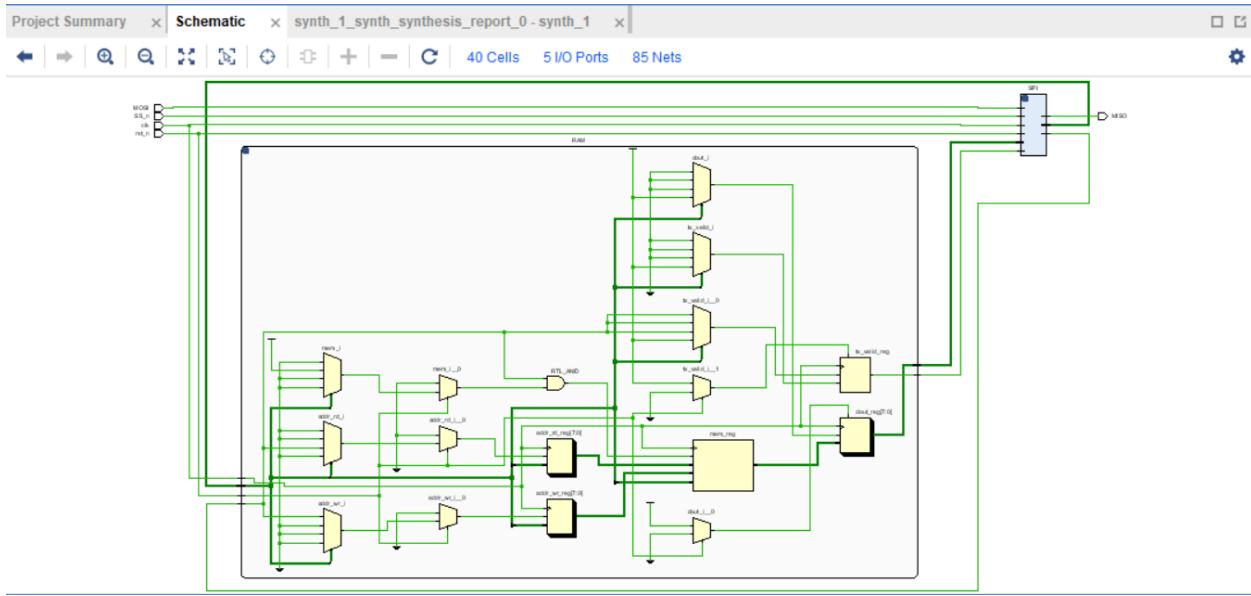
**Implementation (1 warning)**

- > Write Bitstream (1 warning)
  - > DRC (1 warning)
    - > Physical Configuration (1 warning)
      - > Chip Level (1 warning)

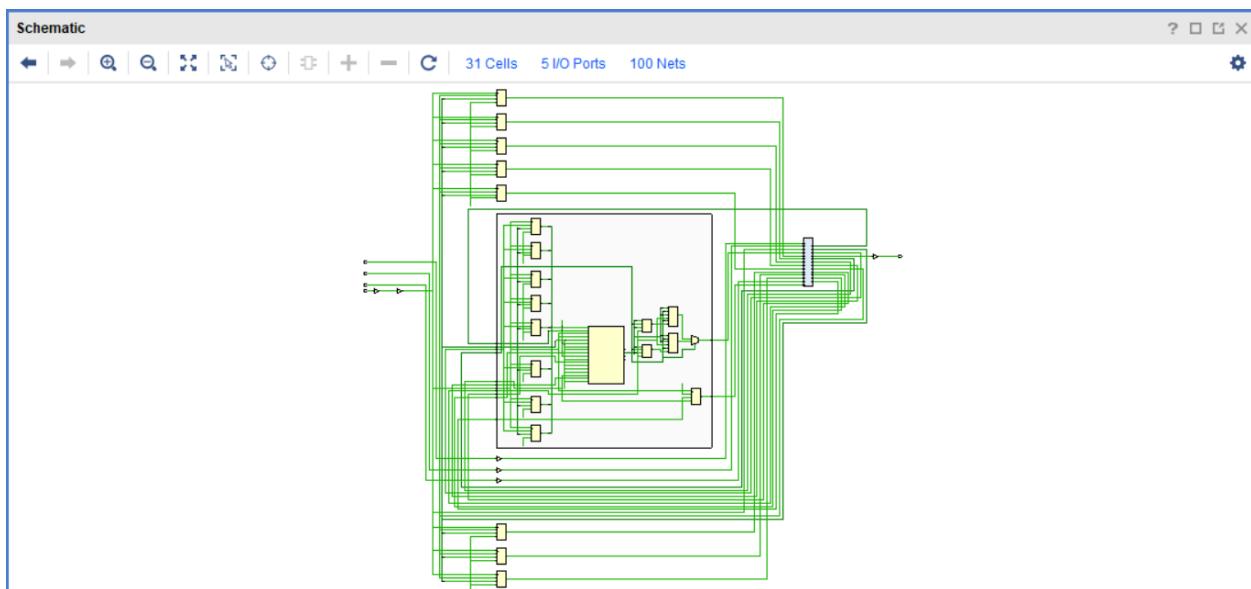
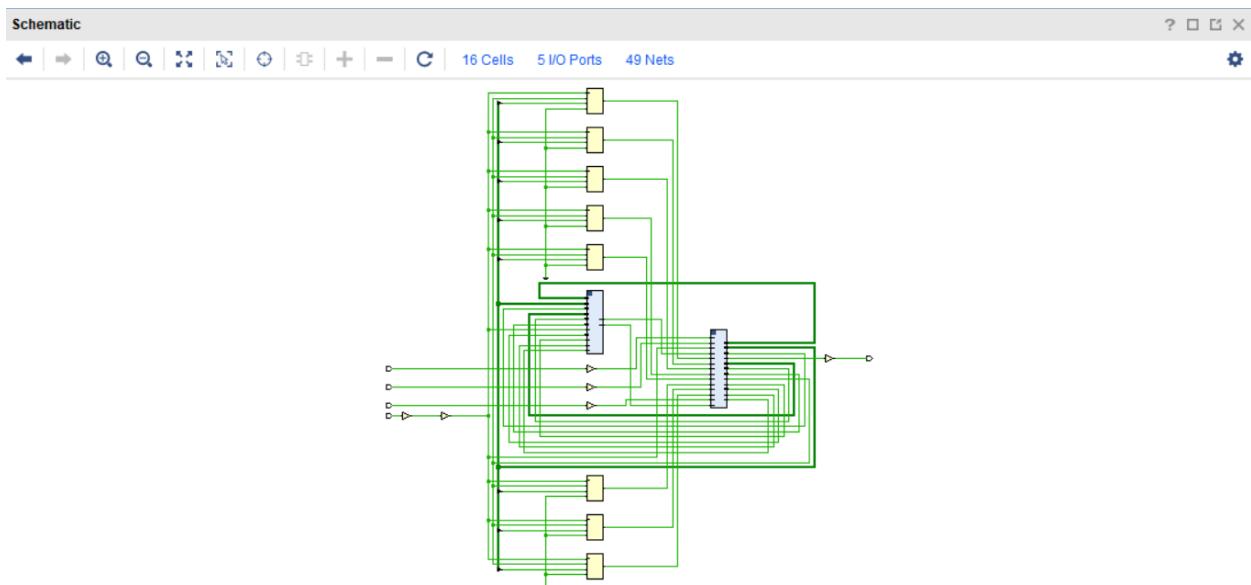
● [DRC PDRC-153] Gated clock check: Net SPI/FSM\_gray\_ns\_reg[2]\_I\_2\_n\_0 is a gated clock net sourced by a combinational pin SPI/FSM\_gray\_ns\_reg[2]\_I\_2/O, cell SPI/FSM\_gray\_ns\_reg[2]\_I\_2. This is not good design practice and will likely impact performance. For SLICE registers, for example, use the CE pin to control the loading of data.

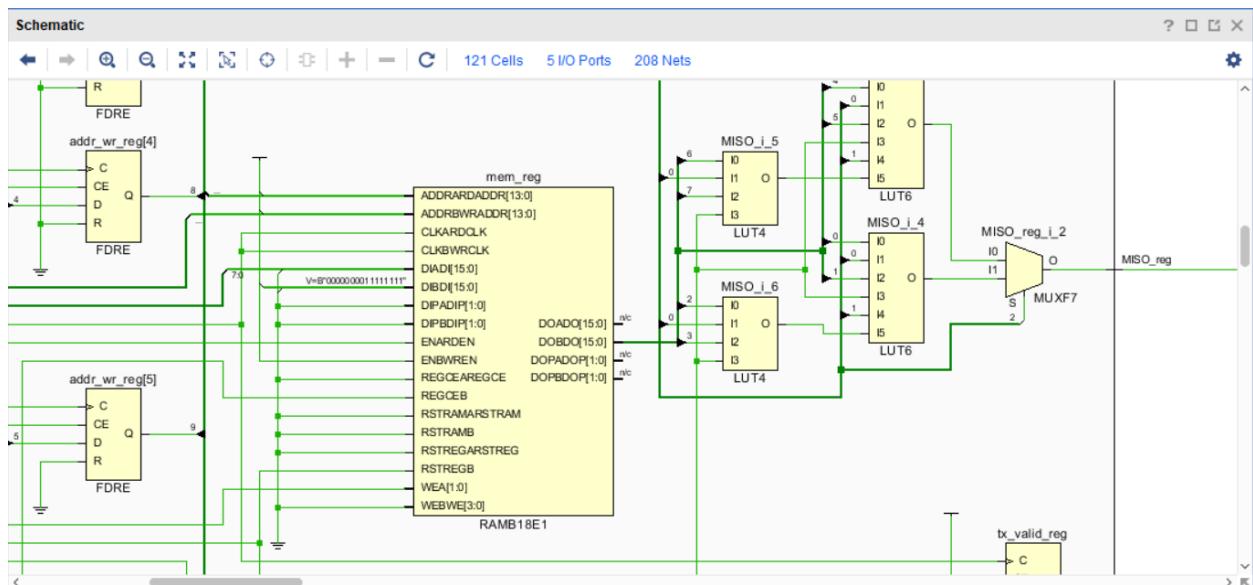
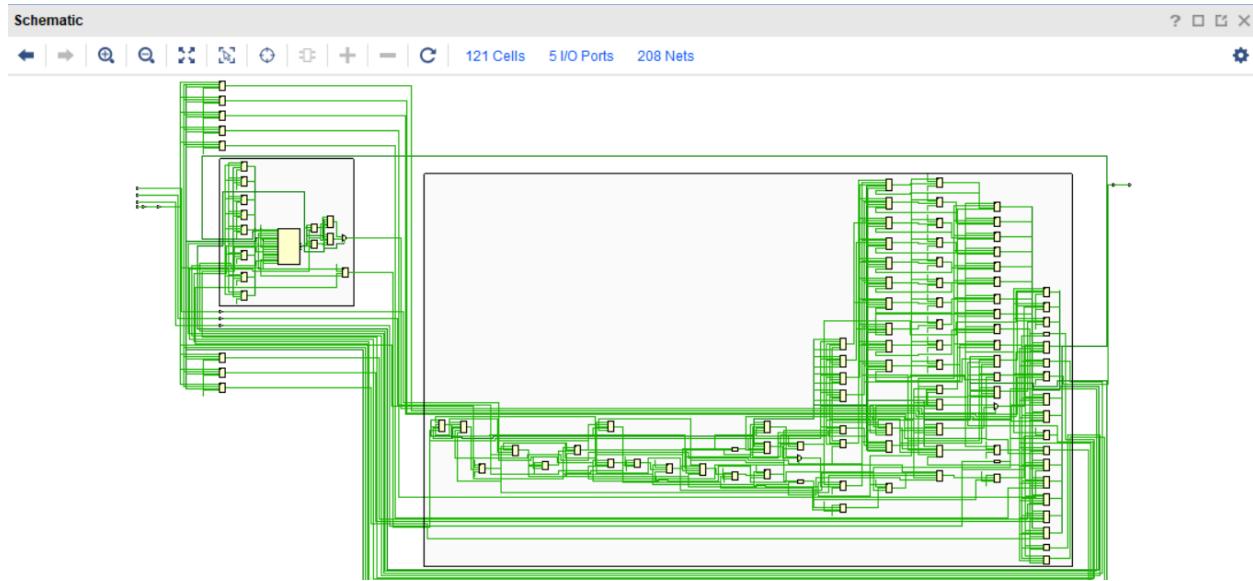
One hot Encoding:

Elaborated design schematic:



## Synthesized Design:





Schematic | synth\_1\_synth\_synthesis\_report\_0 - synth\_1 | Read-only |

D:/2nd year/Digital design/SPI\_Sync/SPI\_Project/SPI\_Project.runs/synth\_1/SPI\_Wrapper.vds

```

25 Parameter WRITE bound to: 3'b010
26 Parameter READ_ADD bound to: 3'b011
27 Parameter READ_DATA bound to: 3'b100
28 INFO: [Synth 8-6157] synthesizing module 'SPI_Slave' [D:/2nd year/Digital design/SPI_Sync/SPI_Slave.V:1]
29     Parameter IDLE bound to: 3'b000
30     Parameter CHK_CMD bound to: 3'b001
31     Parameter WRITE bound to: 3'b010
32     Parameter READ_ADD bound to: 3'b011
33     Parameter READ_DATA bound to: 3'b100
34 INFO: [Synth 8-5534] Detected attribute (* fsm_encoding = "one_hot" *) [D:/2nd year/Digital design/SPI_Sync/SPI_Slave.V:21]
35 INFO: [Synth 8-155] case statement is not full and has no default [D:/2nd year/Digital design/SPI_Sync/SPI_Slave.V:32]
36 INFO: [Synth 8-155] case statement is not full and has no default [D:/2nd year/Digital design/SPI_Sync/SPI_Slave.V:62]
37 INFO: [Synth 8-6155] done synthesizing module 'SPI_Slave' (1#1) [D:/2nd year/Digital design/SPI_Sync/SPI_Slave.V:1]
38 INFO: [Synth 8-6157] synthesizing module 'RAM_Sync_Single_port' [D:/2nd year/Digital design/SPI_Sync/RAM.V:1]
39     Parameter MEM_DEPTH bound to: 256 - type: integer
40     Parameter ADDR_SIZE bound to: 8 - type: integer
41 INFO: [Synth 8-6155] done synthesizing module 'RAM_Sync_Single_port' (2#1) [D:/2nd year/Digital design/SPI_Sync/RAM.V:1]
42 INFO: [Synth 8-6155] done synthesizing module 'SPI_Wrapper' (3#1) [D:/2nd year/Digital design/SPI_Sync/SPI_Wrapper.V:1]
43 -----
44 Finished RTL Elaboration : Time (s): cpu = 00:00:00 ; elapsed = 00:00:02 . Memory (MB): peak = 410.836 ; gain = 153.703
45 -----
46 Report Check Netlist:
47

```

Schematic | synth\_1\_synth\_synthesis\_report\_0 - synth\_1 | Read-only |

D:/2nd year/Digital design/SPI\_Sync/SPI\_Project/SPI\_Project.runs/synth\_1/SPI\_Wrapper.vds

```

91 Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:10 ; elapsed = 00:00:24 . Memory (MB): peak = 759.219 ; gain = 502.086
92 -----
93 INFO: [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'SPI_Slave'.
94 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
95 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
96 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
97 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
98 -----
99             State |           New Encoding |           Previous Encoding
100 -----
101            IDLE |           00001 |           000
102            CHK_CMD |          00010 |           001
103            WRITE |           00100 |           010
104            READ_ADD |          01000 |           011
105            READ_DATA |          10000 |           100
106 -----
107 INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'SPI_Slave'
108 WARNING: [Synth 8-327] inferring latch for variable 'FSM_onehot_ns_reg' [D:/2nd year/Digital design/SPI_Sync/SPI_Slave.V:34]
109 INFO: [Synth 8-6430] The Block RAM mem_reg may get memory collision error if read and write address collide. Use attribute (* rw_addr_collision= "y")
110 INFO: [Synth 8-6430] The Block RAM mem_reg may get memory collision error if read and write address collide. Use attribute (* rw_addr_collision= "y")
111 Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:11 ; elapsed = 00:00:25 . Memory (MB): peak = 759.219 ; gain = 502.086
112 -----
113

```

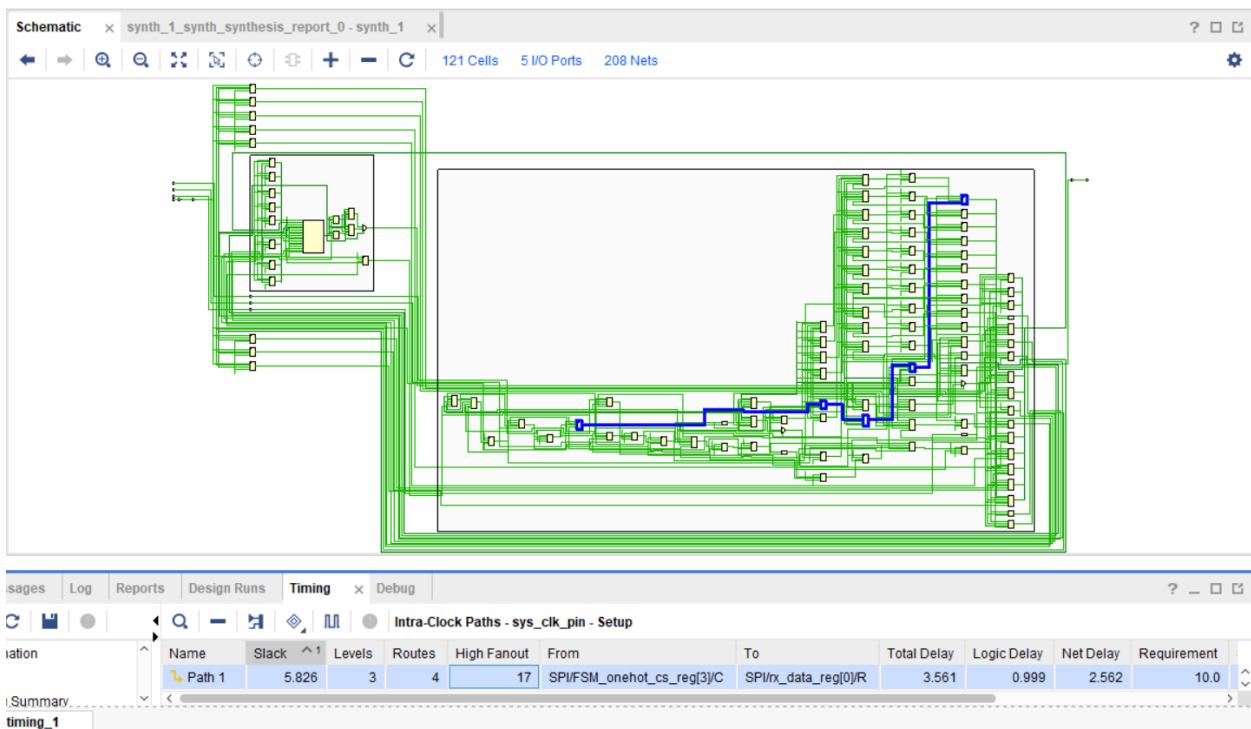
Tcl Console | Messages | Log | Reports | Design Runs | Timing | Debug |

Q | | | | | | | | | | |

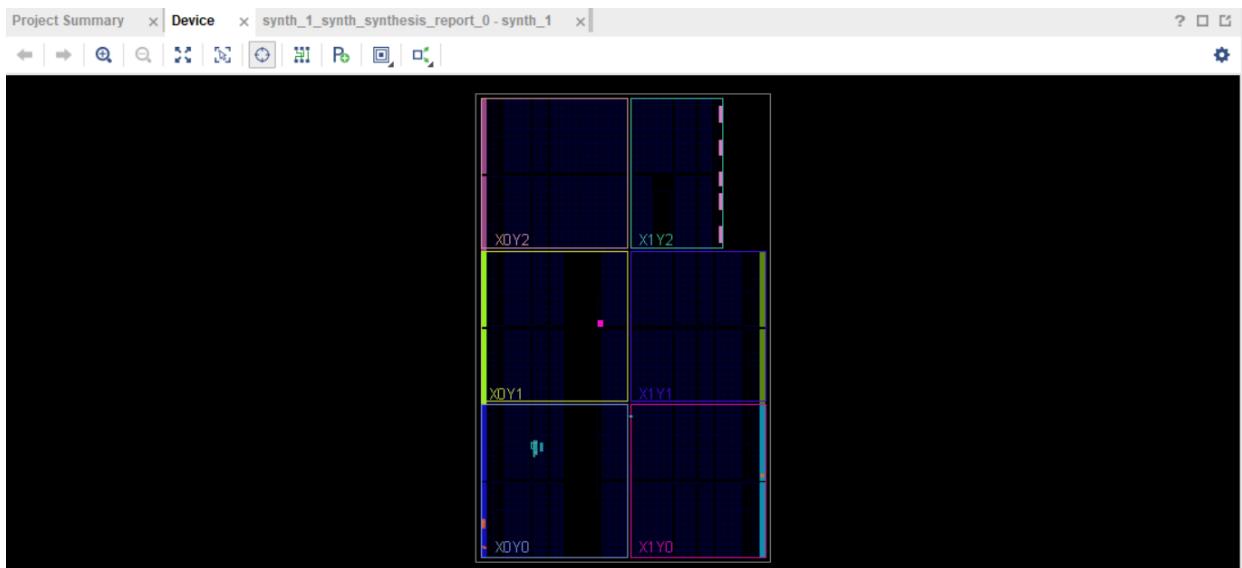
**Design Timing Summary**

General Information		
Timer Settings	Setup	Hold
Design Timing Summary	Worst Negative Slack (WNS): <b>5.826 ns</b>	Worst Hold Slack (WHS): <b>0.089 ns</b>
Clock Summary (1)	Total Negative Slack (TNS): <b>0.000 ns</b>	Total Hold Slack (THS): <b>0.000 ns</b>
Check Timing (34)	Number of Failing Endpoints: <b>0</b>	Number of Failing Endpoints: <b>0</b>
Intra-Clock Paths	Total Number of Endpoints: <b>113</b>	Total Number of Endpoints: <b>113</b>
sys_clk_pin	All user specified timing constraints are met.	Total Number of Endpoints: <b>52</b>
Setup 5.826 ns (10)		

Timing Summary - timing\_1



## Implementation:



Tcl Console | Messages | Log | Reports | Design Runs | Power | DRC | Methodology | **Timing** | X

**Design Timing Summary**

**General Information**

**Timer Settings**

**Design Timing Summary** (selected)

Clock Summary (1)

> Check Timing (34)

> Intra-Clock Paths

Inter-Clock Paths

Other Path Groups

JUserInnored Paths

Timing Summary - impl 1 (saved)

Setup			Hold			Pulse Width		
Worst Negative Slack (WNS):	6.200 ns		Worst Hold Slack (WHS):	0.054 ns		Worst Pulse Width Slack (WPWS):	4.500 ns	
Total Negative Slack (TNS):	0.000 ns		Total Hold Slack (THS):	0.000 ns		Total Pulse Width Negative Slack (TPWS):	0.000 ns	
Number of Failing Endpoints:	0		Number of Failing Endpoints:	0		Number of Failing Endpoints:	0	
Total Number of Endpoints:	113		Total Number of Endpoints:	113		Total Number of Endpoints:	52	

All user specified timing constraints are met.

Tcl Console | Messages | Log | Reports | Design Runs | Power | DRC | Methodology | **Utilization** | X

**Hierarchy**

Summary

slice Logic

- slice LUTs (<1%)
- LUT as Logic (<1%)
- F7 Muxes (<1%)
- slice Registers (<1%)
- Register as Latch (<1%)

Name	1	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N SPI_Wrapper	53	54	3	16	53	22	0.5	5	1	
RAM (RAM_Sync_Singl...)	4	9	1	4	4	0	0.5	0	0	
SPI (SPI_Slave)	49	37	2	16	49	20	0	0	0	

IMPLEMENTED DESIGN - xc7a35ticpg236-1L (active)

Sour Nx ? \_ □

Project Summary | Device | synth\_1\_synth\_synthesis\_report\_0 - synth\_1

Bitstream Generation Completed

Bitstream Generation successfully completed.

Next

View Reports

Open Hardware Manager

Generate Memory Configuration File

Don't show this dialog again

OK Cancel

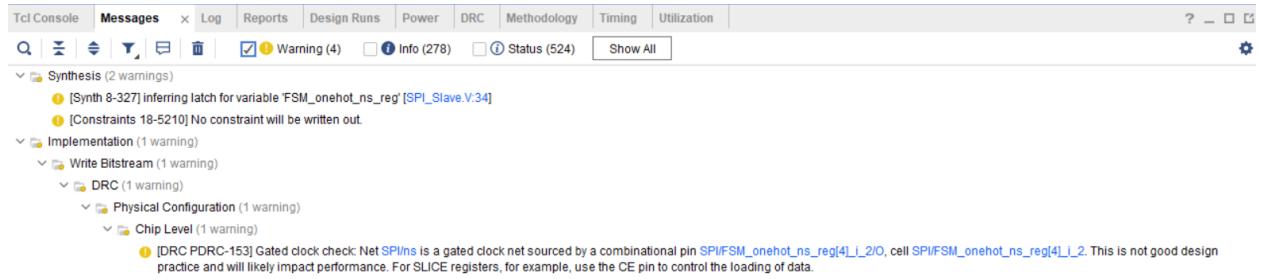
Hierarchy

Summary

slice Logic

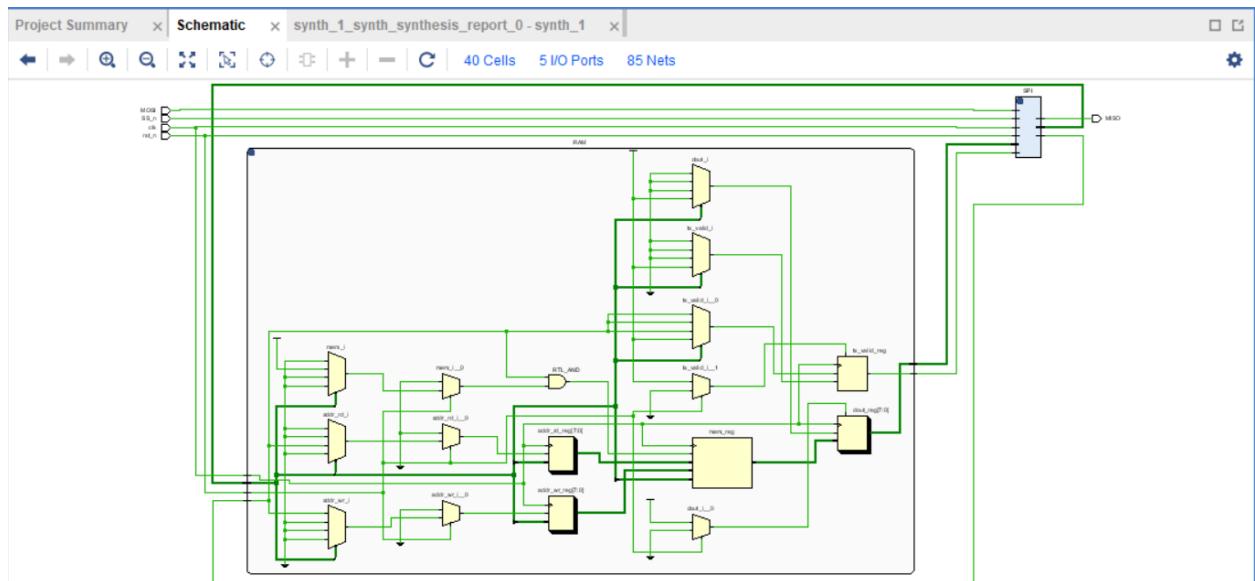
- slice LUTs (<1%)
- LUT as Logic (<1%)
- F7 Muxes (<1%)
- slice Registers (<1%)
- Register as Latch (<1%)

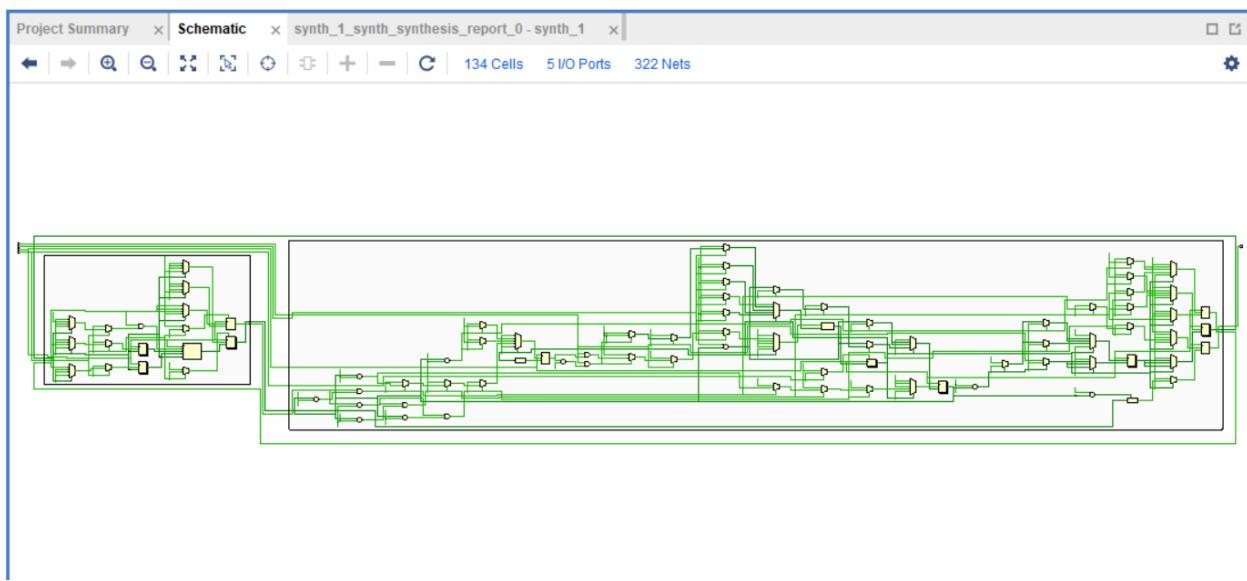
Name	1	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM (50)
N SPI_Wrapper	53	54	3	16	53	22		
RAM (RAM_Sync_Singl...)	4	9	1	4	4	0		
SPI (SPI_Slave)	49	37	2	16	49	20		



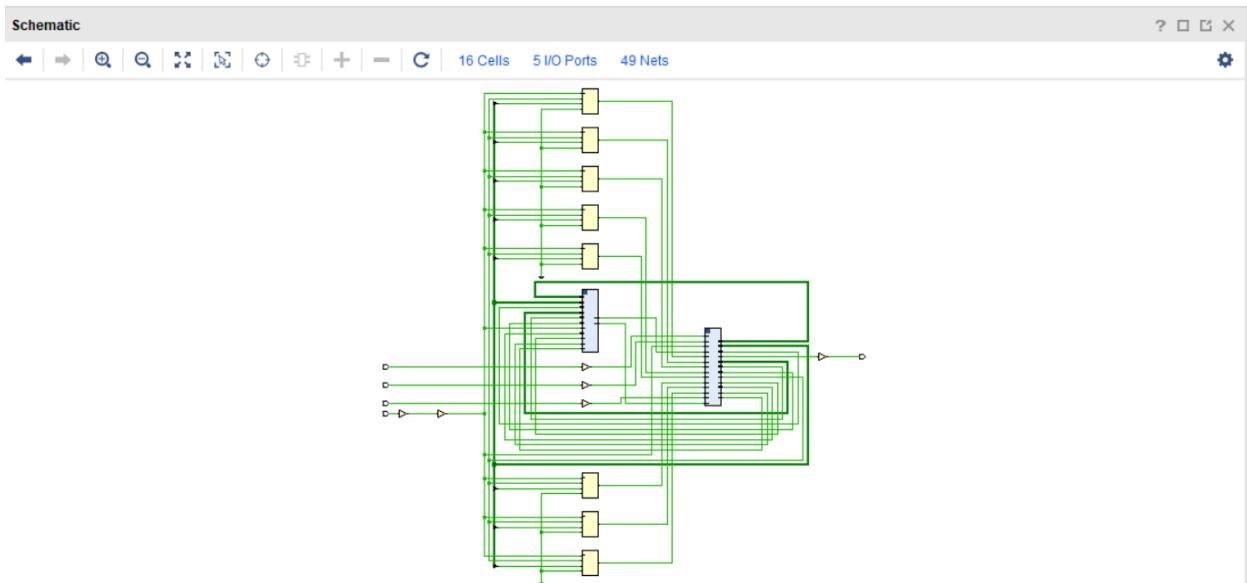
## Sequential Encoding:

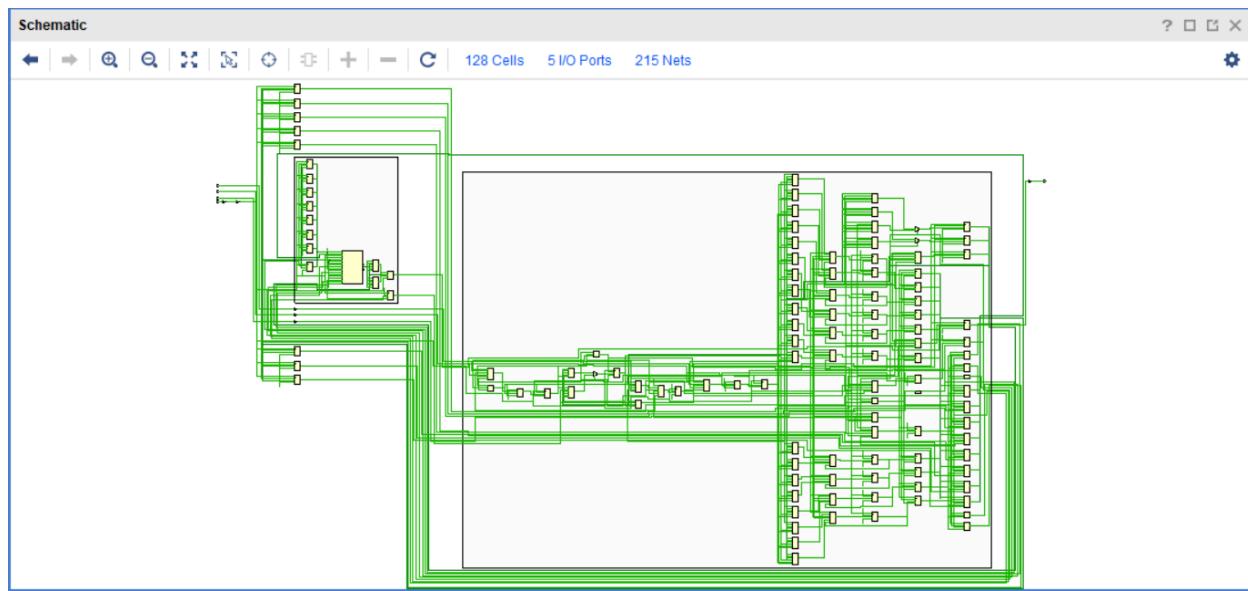
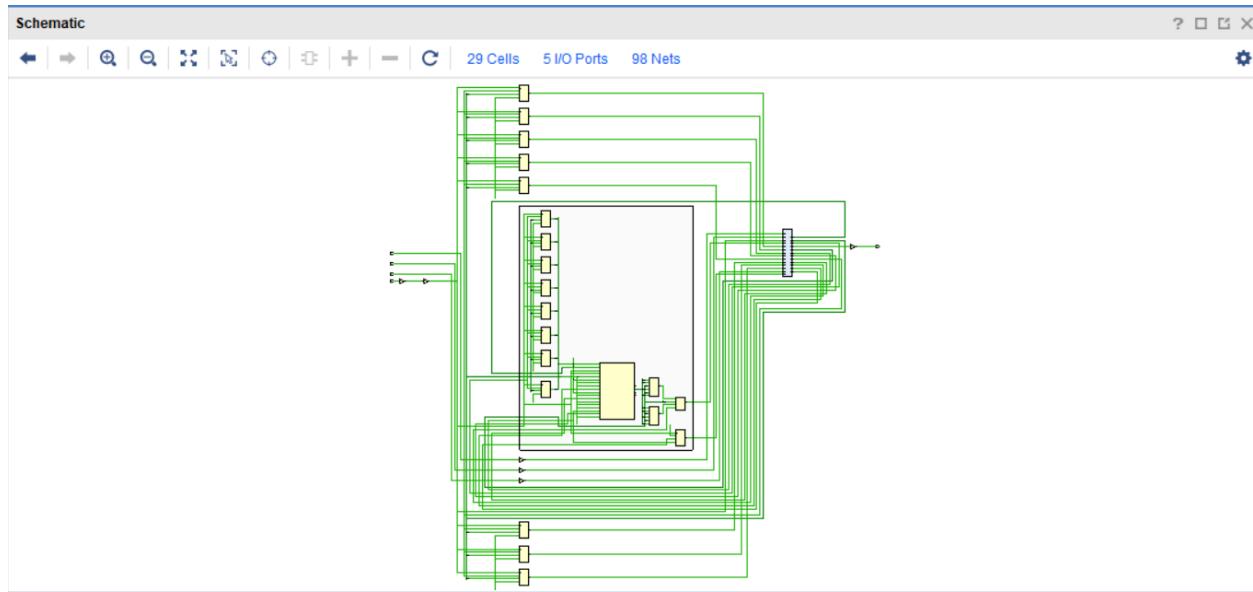
Elaborated design schematic:

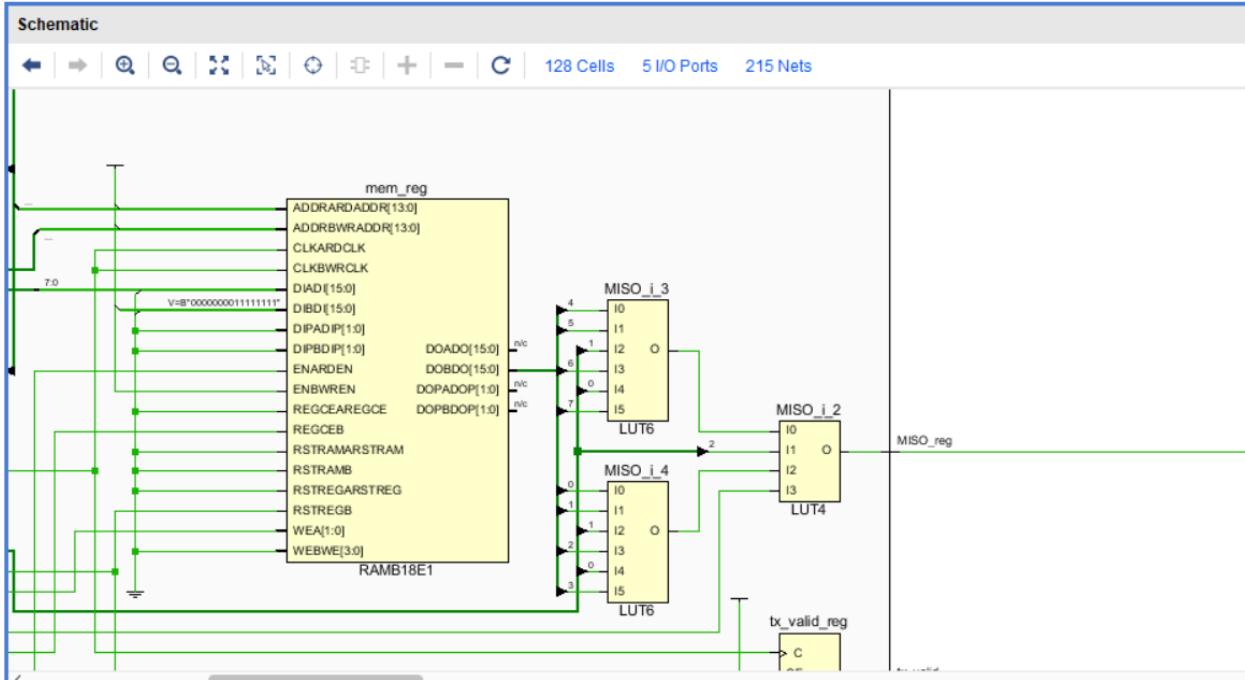




## Synthesized Design:







Schematic x synth\_1\_synth\_synthesis\_report\_0 - synth\_1 x

D:/2nd year/Digital design/SPI\_Sync/SPI\_Project/SPI\_Project.rns/synth\_1/SPI\_Wrapper.vds

Read-Only

```

22 INFO: [Synth 8-6157] synthesizing module 'SPI_Wrapper' [D:/2nd year/Digital design/SPI_Sync/SPI_Wrapper.V:1]
23   Parameter IDLE bound to: 3'b000
24   Parameter CHK_CMD bound to: 3'b001
25   Parameter WRITE bound to: 3'b010
26   Parameter READ_ADD bound to: 3'b011
27   Parameter READ_DATA bound to: 3'b100
28 INFO: [Synth 8-6157] synthesizing module 'SPI_Slave' [D:/2nd year/Digital design/SPI_Sync/SPI_Slave.V:1]
29   Parameter IDLE bound to: 3'b000
30   Parameter CHK_CMD bound to: 3'b001
31   Parameter WRITE bound to: 3'b010
32   Parameter READ_ADD bound to: 3'b011
33   Parameter READ_DATA bound to: 3'b100
34 INFO: [Synth 8-5534] Detected attribute (* fsm_encoding = "sequential" *) [D:/2nd year/Digital design/SPI_Sync/SPI_Slave.V:21]
35 INFO: [Synth 8-155] case statement is not full and has no default [D:/2nd year/Digital design/SPI_Sync/SPI_Slave.V:32]
36 INFO: [Synth 8-155] case statement is not full and has no default [D:/2nd year/Digital design/SPI_Sync/SPI_Slave.V:62]
37 INFO: [Synth 8-6155] done synthesizing module 'SPI_Slave' (1#1) [D:/2nd year/Digital design/SPI_Sync/SPI_Slave.V:1]
38 INFO: [Synth 8-6157] synthesizing module 'RAM_Sync_Single_port' [D:/2nd year/Digital design/SPI_Sync/RAM.V:1]
39   Parameter MEM_DEPTH bound to: 256 - type: integer
40   Parameter ADDR_SIZE bound to: 8 - type: integer
41 INFO: [Synth 8-6155] done synthesizing module 'RAM_Sync_Single_port' (2#1) [D:/2nd year/Digital design/SPI_Sync/RAM.V:1]
42 INFO: [Synth 8-6155] done synthesizing module 'SPI_Wrapper' (3#1) [D:/2nd year/Digital design/SPI_Sync/SPI_Wrapper.V:1]
43

```

Schematic × synth\_1\_synth\_synthesis\_report\_0 - synth\_1 ×

D:/2nd year/Digital design/SPI\_Sync/SPI\_Project/SPI\_Project.rns/synth\_1/SPI\_Wrapper.vds

Q | H | ← | → | X | // | E | ? |

```

88 Start Applying 'set_property' XDC Constraints
89 -----
90
91 Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:12 ; elapsed = 00:00:25 . Memory (MB): peak =
92 -----
93 INFO: [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'SPI_Slave'
94 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
95 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
96 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
97 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
98 -----
99         State |           New Encoding |           Previous Encoding
100 -----
101        IDLE |           000 |           000
102      CHK_CMD |           001 |           001
103        WRITE |           010 |           010
104     READ_ADD |           011 |           011
105    READ_DATA |           100 |           100
106 -----
107 INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'SPI_Slave'
108 WARNING: [Synth 8-327] inferring latch for variable 'FSM_sequential_ns_reg' [D:/2nd year/Digital design/SPI_Sync/SPI_
109 INFO: [Synth 8-61301] The Block RAM mem reg may get memory collision error if read and write address collide. Use attr
<

```

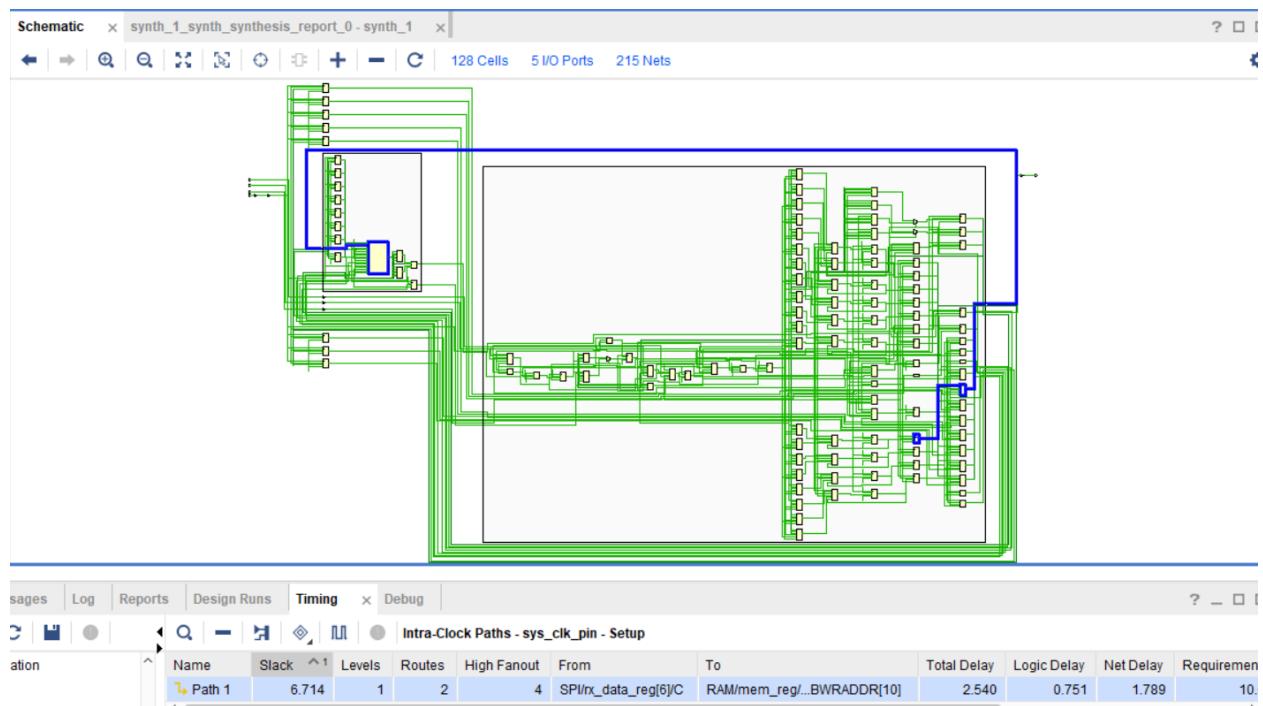
Tcl Console Messages Log Reports Design Runs **Timing** × Debug

Q | H | ← | → | C | U | ? |

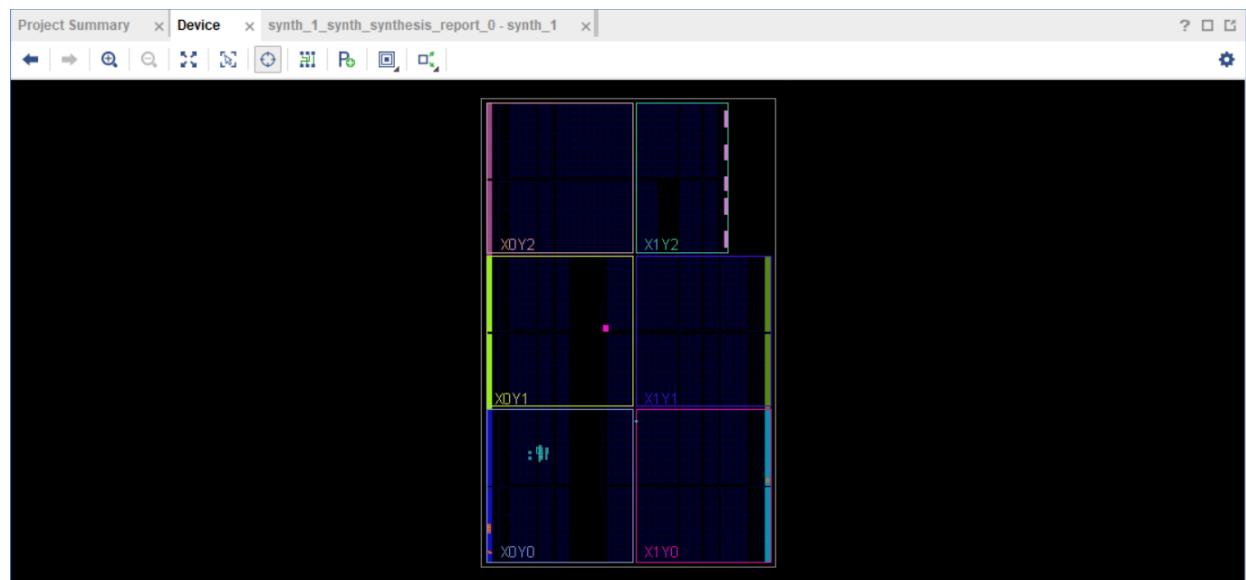
### Design Timing Summary

General Information		
Timer Settings	Setup	Hold
<b>Design Timing Summary</b>	Worst Negative Slack (WNS): <b>6.714 ns</b>	Worst Hold Slack (WHS): <b>0.158 ns</b>
Clock Summary (1)	Total Negative Slack (TNS): <b>0.000 ns</b>	Total Hold Slack (THS): <b>0.000 ns</b>
> <b>Check Timing (16)</b>	Number of Failing Endpoints: <b>0</b>	Number of Failing Endpoints: <b>0</b>
> <b>Intra-Clock Paths</b>	Total Number of Endpoints: <b>113</b>	Total Number of Endpoints: <b>113</b>
> <b>Inter-Clock Paths</b>		
> <b>Other Path Groups</b>		
> <b>User Ignored Paths</b>		
> <b>Unconstrained Paths</b>		

All user specified timing constraints are met.



Implementation:



Design Timing Summary									
General Information		Setup			Hold		Pulse Width		
Timer Settings		Worst Negative Slack (WNS): <b>6.605 ns</b>			Worst Hold Slack (WHS): <b>0.071 ns</b>		Worst Pulse Width Slack (WPWS): <b>4.500 ns</b>		
Design Timing Summary		Total Negative Slack (TNS): <b>0.000 ns</b>			Total Hold Slack (THS): <b>0.000 ns</b>		Total Pulse Width Negative Slack (TPWS): <b>0.000 ns</b>		
Clock Summary (1)		Number of Failing Endpoints: <b>0</b>			Number of Failing Endpoints: <b>0</b>		Number of Failing Endpoints: <b>0</b>		
> Check Timing (16)		Total Number of Endpoints: <b>113</b>			Total Number of Endpoints: <b>113</b>		Total Number of Endpoints: <b>50</b>		
> Intra-Clock Paths									
Inter-Clock Paths									

Utilization											
Hierarchy		Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
Summary		N SPI_Wrapper	65	50	3	20	65	20	0.5	5	1
Slice Logic		RAM (RAM_Sync_Singl...	3	9	0	4	3	0	0.5	0	0
Slice LUTs (1%)		SPI (SPI_Slave)	62	33	3	20	62	18	0	0	0
LUT as Logic (1%)											
F7 Muxes (<1%)											

IMPLEMENTED DESIGN - xc7z020clg484-1L (active)

Project Summary | Device | synth\_1\_synth\_synthesis\_report\_0 - synth\_1

Bitstream Generation Completed

Bitstream Generation successfully completed.

Next

View Reports

Open Hardware Manager

Generate Memory Configuration File

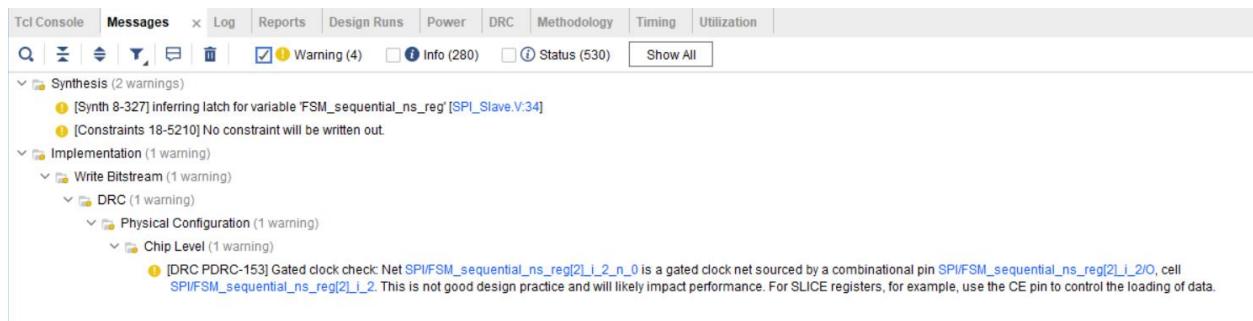
Don't show this dialog again

OK Cancel

Tcl Console | Messages | Log | Reports | Design Runs | Power | DRC | Methodology | Timing | Utilization

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)
N SPI_Wrapper	65	50	3	20	65	20	0.5	5
RAM (RAM_Sync_Singl...	3	9	0	4	3	0	0.5	0
SPI (SPI_Slave)	62	33	3	20	62	18	0	0



### Comment:

The Best Encoding is Sequential Encoding as it has the highest setup/hold slack after implementation.

### Sequential Encoding with debug core:

