DSP Mini Project:

Submitted to: ENG. Kareem Waseem

Design Code:

```
module DSP
(A,B,D,C,CLK,CARRYIN,OPMODE,BCIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOP
MODE,CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE,PCIN,BCOUT,PCOUT,P,M,CARRYOUT,C
ARRYOUTF);

  input [17:0] A,B,D,BCIN;
  input [47:0] C,PCIN;
  input [7:0] OPMODE;
  input
CLK,CARRYIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,CEA,CEB,CEM,CEP,
CEC,CED,CECARRYIN,CEOPMODE;

  output [17:0] BCOUT;
  output [47:0] PCOUT,P;
  output [35:0] M;
  output CARRYOUT,CARRYOUTF;

  parameter A0REG = 0;
  parameter A1REG = 1;
  parameter B0REG = 0;
  parameter B1REG = 1;
  parameter CREG = 1;
  parameter DREG = 1;
  parameter MREG = 1;
  parameter PREG = 1;
  parameter CARRYINREG = 1;
  parameter CARRYOUTREG = 1;
  parameter OPMODEREG = 1;
  parameter CARRYINSEL = "OPMODE5";
  parameter B_INPUT = "DIRECT";
  parameter RSTTYPE = "SYNC";

  wire [17:0] D_MUX,B0_MUX,A0_MUX,PRE_OUT,MUX_POST,B1_MUX,A1_MUX;
  wire [47:0] C_MUX,POST_OUT,D_CONCAT,P_MUX;
  wire [7:0] OPMODE_MUX;
  wire [35:0] MUL_OUT,M_MUX;
  wire CYI,CYO,CARRY_IN_MUX,CARRYOUT_POST_ADDER;
  reg [47:0] OUT_X,OUT_Z;

  //1st Stage

  FF_Mux #(.W(18),.SEL(DREG),.RSTTYPE(RSTTYPE)) m1 (D,CLK,CED,RSTD,D_MUX);
```

```
  FF_Mux #(.W(18),.SEL(A0REG),.RSTTYPE(RSTTYPE)) m2 (A,CLK,CEA,RSTA,A0_MUX);
  FF_Mux #(.W(48),.SEL(CREG),.RSTTYPE(RSTTYPE)) m3 (C,CLK,RSTC,CEC,C_MUX);
  FF_Mux #(.W(8),.SEL(OPMODEREG),.RSTTYPE(RSTTYPE)) m4
(OPMODE,CLK,CEOPMODE,RSTOPMODE,OPMODE_MUX);

  Mux #(.B_INPUT(B_INPUT),.B0REG(B0REG),.RSTTYPE(RSTTYPE)) n1
(B,BCIN,CLK,CEB,RSTB,B0_MUX);

  //2nd Stage

  assign  PRE_OUT = (OPMODE_MUX[6])? D_MUX-B0_MUX : D_MUX+B0_MUX ;
  assign  MUX_POST = (OPMODE_MUX[4])? PRE_OUT : B0_MUX;

  FF_Mux #(.W(18),.SEL(B1REG),.RSTTYPE(RSTTYPE)) m6
(MUX_POST,CLK,CEB,RSTB,B1_MUX);
  FF_Mux #(.W(18),.SEL(A1REG),.RSTTYPE(RSTTYPE)) m7
(A0_MUX,CLK,CEA,RSTA,A1_MUX);

    //4th Stage

  assign MUL_OUT = B1_MUX * A1_MUX;
  assign BCOUT = B1_MUX;

  FF_Mux #(.W(36),.SEL(MREG),.RSTTYPE(RSTTYPE)) m8
(MUL_OUT,CLK,CEM,RSTM,M_MUX);

  assign M = M_MUX;

  mux2 #(.CARRYINSEL(CARRYINSEL)) n2 (CARRYIN,OPMODE_MUX[5],CYI);

  FF_Mux #(.W(1),.SEL(CARRYINREG),.RSTTYPE(RSTTYPE)) m9
(CYI,CLK,CECARRYIN,RSTCARRYIN,CARRY_IN_MUX);

  assign D_CONCAT ={D_MUX[11:0],A1_MUX,B1_MUX};

  //5th Stage

  always @* begin
      case (OPMODE_MUX[1:0])
          2'b00: OUT_X = 48'd0;
          2'b01: OUT_X = {12'd0, M_MUX};
          2'b10: OUT_X = P_MUX;
          2'b11: OUT_X = D_CONCAT;
      endcase
  end
```

```
  always @* begin
      case (OPMODE_MUX[3:2])
          2'b00: OUT_Z = 48'd0;
          2'b01: OUT_Z = PCIN;
          2'b10: OUT_Z = P_MUX;
          2'b11: OUT_Z = C_MUX;
      endcase
  end

  assign {CARRYOUT_POST_ADDER,POST_OUT} = (OPMODE_MUX[7])? (OUT_Z-(OUT_X +
CARRY_IN_MUX)) :  (OUT_Z + OUT_X + CARRY_IN_MUX);

  FF_Mux #(.W(1),.SEL(CARRYOUTREG),.RSTTYPE(RSTTYPE)) m10
(CARRYOUT_POST_ADDER,CLK,CECARRYIN,RSTCARRYIN,CYO);

  assign CARRYOUT = CYO;
  assign CARRYOUTF = CYO;

  //Final Stage

  FF_Mux #(.W(48),.SEL(PREG),.RSTTYPE(RSTTYPE)) m11
(POST_OUT,CLK,CEP,RSTP,P_MUX);

  assign P = P_MUX;
  assign PCOUT = P_MUX;

endmodule
```

1ST Subcode:

```
module FF_Mux (D,CLK,CEN,rst,Q);

  parameter W=18;
  parameter SEL=0;
  parameter RSTTYPE="SYNC";
  input [W-1:0] D;
  input CLK,rst,CEN;
  output [W-1:0] Q;

  reg [W-1:0] D_reg;
```

```
  generate

  if (RSTTYPE=="ASYNC") begin
    always @(posedge CLK or posedge rst) begin
      if (rst)
        D_reg<=0;
      else if (CEN)
        D_reg<=D;
    end
  end
  else if (RSTTYPE=="SYNC") begin
    always @(posedge CLK) begin
      if (rst)
        D_reg<=0;
      else if (CEN)
        D_reg<=D;
    end
  end
  endgenerate

  assign Q = (SEL)? D_reg : D ;

endmodule
```

2nd Subcode:

```
module Mux (B,BCIN,CLK,CEB,RSTB,B0_MUX);

  parameter B_INPUT="DIRECT";
  parameter B0REG=0;
  parameter RSTTYPE="SYNC";

  input CLK,CEB,RSTB;
  input [17:0] B,BCIN;

  output [17:0]B0_MUX;


  generate
    if (B_INPUT == "DIRECT")
```

```
      FF_Mux #(.W(18),.SEL(B0REG),.RSTTYPE(RSTTYPE)) m5
(B,CLK,CEB,RSTB,B0_MUX);
    else if (B_INPUT == "CASCADE")
      FF_Mux #(.W(18),.SEL(B0REG),.RSTTYPE(RSTTYPE)) m5
(BCIN,CLK,CEB,RSTB,B0_MUX);
    else
      FF_Mux #(.W(18),.SEL(B0REG),.RSTTYPE(RSTTYPE)) m5
(18'b0000_0000_0000_0000_00,CLK,CEB,RSTB,B0_MUX);
  endgenerate

endmodule
```

3rd Subcode:

```
module mux2 (CARRYIN,OPMODE_MUX5,CYI);


  input OPMODE_MUX5,CARRYIN;

  output reg CYI;

  parameter CARRYINSEL="OPMODE5";

    always @(*) begin
    if (CARRYINSEL == "OPMODE5")
      CYI = OPMODE_MUX5;
    else if (CARRYINSEL == "CARRYIN")
      CYI = CARRYIN;
    else
      CYI = 0;
  end

endmodule
```

Test bench code:

```
module DSP_tb();

    reg [17:0] A, B, D, BCIN;
    reg [47:0] C, PCIN;
    reg [7:0] OPMODE;
    reg CLK, CARRYIN, RSTA, RSTB, RSTM, RSTP, RSTC, RSTD, RSTCARRYIN,
RSTOPMODE;
    reg CEA, CEB, CEM, CEP, CEC, CED, CECARRYIN, CEOPMODE;

    wire [17:0] BCOUT;
    wire [47:0] PCOUT, P;
    wire [35:0] M;
    wire CARRYOUT, CARRYOUTF;


    DSP DUT
(A,B,D,C,CLK,CARRYIN,OPMODE,BCIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOP
MODE,CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE,PCIN,BCOUT,PCOUT,P,M,CARRYOUT,C
ARRYOUTF);

    initial begin
        CLK=0;
        forever
            #1 CLK = ~CLK;
    end

    integer i;
    initial begin
        // Initialize inputs
        A = 18'd0;
        B = 18'd0;
        D = 18'd0;
        BCIN = 18'd0;
        C = 48'd0;
        PCIN = 48'd0;
        OPMODE = 8'd0;
        CLK = 0;
        CARRYIN = 0;
        RSTA = 0;
        RSTB = 0;
        RSTM = 0;
        RSTP = 0;
```

```
        RSTC = 0;
        RSTD = 0;
        RSTCARRYIN = 0;
        RSTOPMODE = 0;
        CEA = 0;
        CEB = 0;
        CEM = 0;
        CEP = 0;
        CEC = 0;
        CED = 0;
        CECARRYIN = 0;
        CEOPMODE = 0;

        @(negedge CLK);

        RSTA = 1;
        RSTB = 1;
        RSTM = 1;
        RSTP = 1;
        RSTC = 1;
        RSTD = 1;
        RSTCARRYIN = 1;
        RSTOPMODE = 1;
        CEA = 1;
        CEB = 1;
        CEM = 1;
        CEP = 1;
        CEC = 1;
        CED = 1;
        CECARRYIN = 1;
        CEOPMODE = 1;

        #10;

        A = 18'h00123; B = 18'h00456; D = 18'h00000;
        C = 48'h0000000000; PCIN = 48'h0000000000;
        OPMODE = 8'h00; BCIN = 18'h00000; CARRYIN = 0;

        repeat(4)
            @(negedge CLK);


        for(i=0; i<100; i=i+1) begin
            A = $random;
            B = $random;
```

```
            D = $random;
            C = $random;
            OPMODE = $random;
            CECARRYIN = $random;
            CEOPMODE = $random;
            @(negedge CLK);

            if (PCOUT !== 0)begin
                $display("Test Failed");
                $stop;
            end
            if (P !== 0)begin
                $display("Test Failed");
                $stop;
            end
            if (M !== 0)begin
                $display("Test Failed");
                $stop;
            end
            if (CARRYOUT !== 0)begin
                $display("Test Failed");
                $stop;
            end
            if (CARRYOUTF !== 0)begin
            $display("Test Failed");
            $stop;
            end
        end

        RSTA = 0;
        RSTB = 0;
        RSTM = 0;
        RSTP = 0;
        RSTC = 0;
        RSTD = 0;
        RSTCARRYIN = 0;
        RSTOPMODE = 0;

        for(i=0; i<1000; i=i+1) begin
            A = $random;
            B = $random;
            D = $random;
            C = $random;
            OPMODE = $random;
            CECARRYIN = $random;
```

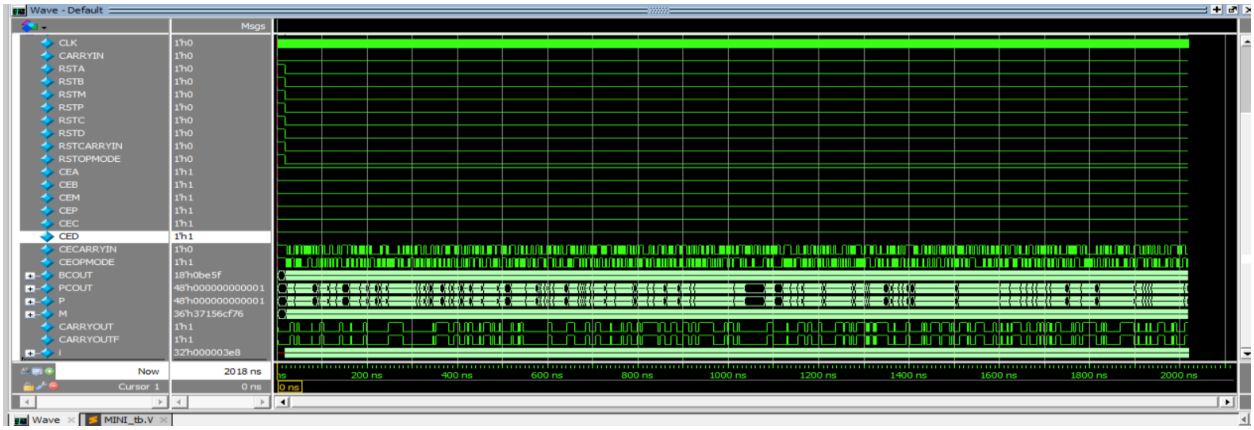
```
            CEOPMODE = $random;
            @(negedge CLK);
        end
        $stop;
    end

    initial begin
        $monitor("A= %d, B= %d, C= %d, D= %d, BCIN= %d, PCIN= %d, OPMODE= %b,
BCOUT = %d, PCOUT = %d, P = %d, M = %d, CARRYOUT = %d, CARRYOUTF =
%d",A,B,C,D,BCIN,PCIN,OPMODE,BCOUT,PCOUT,P,M,CARRYOUT,CARRYOUTF);
    end
endmodule
```

- Do_file:

```
vlib work
vlog MINI_tb.V
vsim -voptargs=+acc work.DSP_tb
add wave *
run -all
```

```
1  vlib work
2  vlog MINI_tb.V
3  vsim -voptargs=+acc work.DSP_tb
4  add wave *
5  run -all
```

- Simulations:




```
# A= 186409, B=  86460, C=       1613180352, D= 198704, BCIN=     0, PCIN=              0, OPMODE= 01010000, BCOUT =     0, PCOUT =              0, P =              0, M =              0, CARRYOUT = 0, CARRYOUTF =
0
# A= 208629, B= 241653, C= 281474075464340, D= 183389, BCIN=     0, PCIN=              0, OPMODE= 01101010, BCOUT =     0, PCOUT =              0, P =              0, M =              0, CARRYOUT = 0, CARRYOUTF =
0
# A=  40094, B=  67322, C= 281472895968263, D=   2886, BCIN=     0, PCIN=              0, OPMODE= 10010011, BCOUT =     0, PCOUT =              0, P =              0, M =              0, CARRYOUT = 0, CARRYOUTF =
0
# A= 127301, B=   2659, C= 281473155517990, D= 254041, BCIN=     0, PCIN=              0, OPMODE= 01101000, BCOUT =     0, PCOUT =              0, P =              0, M =              0, CARRYOUT = 0, CARRYOUTF =
0
# A= 107866, B= 230684, C=       1434853291, D=  92089, BCIN=     0, PCIN=              0, OPMODE= 11010000, BCOUT =     0, PCOUT =              0, P =              0, M =              0, CARRYOUT = 0, CARRYOUTF =
0
# A=  34885, B= 173965, C=       2116325884, D= 205707, BCIN=     0, PCIN=              0, OPMODE= 11011100, BCOUT =     0, PCOUT =              0, P =              0, M =              0, CARRYOUT = 0, CARRYOUTF =
0
# A=  78757, B= 101950, C= 281473575300184, D= 246003, BCIN=     0, PCIN=              0, OPMODE= 11000100, BCOUT =     0, PCOUT =              0, P =              0, M =              0, CARRYOUT = 0, CARRYOUTF =
0
# A=  86170, B= 137496, C=       1427493290, D=  26309, BCIN=     0, PCIN=              0, OPMODE= 00011010, BCOUT =     0, PCOUT =              0, P =              0, M =              0, CARRYOUT = 0, CARRYOUTF =
0
# A= 221964, B=   3817, C=       1974301675, D= 196035, BCIN=     0, PCIN=              0, OPMODE= 11111000, BCOUT =     0, PCOUT =              0, P =              0, M =              0, CARRYOUT = 0, CARRYOUTF =
0
# A=  29551, B=  84763, C=        877511016, D=  75949, BCIN=     0, PCIN=              0, OPMODE= 00100101, BCOUT =     0, PCOUT =              0, P =              0, M =              0, CARRYOUT = 0, CARRYOUTF =
0
# A=  53787, B= 212608, C=       1093533058, D= 186717, BCIN=     0, PCIN=              0, OPMODE= 00000100, BCOUT =     0, PCOUT =              0, P =              0, M =              0, CARRYOUT = 0, CARRYOUTF =
0
# A= 131890, B= 206969, C= 281473018162198, D= 241380, BCIN=     0, PCIN=              0, OPMODE= 10101010, BCOUT =     0, PCOUT =              0, P =              0, M =              0, CARRYOUT = 0, CARRYOUTF =
0
# A=  79756, B=  49777, C=       1582571964, D= 167931, BCIN=     0, PCIN=              0, OPMODE= 11011100, BCOUT =     0, PCOUT =              0, P =              0, M =              0, CARRYOUT = 0, CARRYOUTF =
0
# A= 205291, B=  80821, C= 281474032132751, D=  77449, BCIN=     0, PCIN=              0, OPMODE= 10111111, BCOUT =     0, PCOUT =              0, P =              0, M =              0, CARRYOUT = 0, CARRYOUTF =
0
# A=  66262, B=  52354, C=        954640241, D= 226586, BCIN=     0, PCIN=              0, OPMODE= 11010111, BCOUT =     0, PCOUT =              0, P =              0, M =              0, CARRYOUT = 0, CARRYOUTF =
0
# A= 138701, B=  82693, C=       1276692376, D= 191260, BCIN=     0, PCIN=              0, OPMODE= 11101100, BCOUT =     0, PCOUT =              0, P =              0, M =              0, CARRYOUT = 0, CARRYOUTF =
0
# A= 132407, B= 144899, C= 281474954550525, D= 171774, BCIN=     0, PCIN=              0, OPMODE= 00111110, BCOUT =     0, PCOUT =              0, P =              0, M =              0, CARRYOUT = 0, CARRYOUTF =
0
# A= 100784, B= 121862, C= 281473708653672, D= 150802, BCIN=     0, PCIN=              0, OPMODE= 11000101, BCOUT =     0, PCOUT =              0, P =              0, M =              0, CARRYOUT = 0, CARRYOUTF =
0
```

```
# Loading work.FF_Mux(fast__5)
# A=      0, B=      0, C=              0, D=      0, BCIN=     0, PCIN=              0, OPMODE= 00000000, BCOUT =     x, PCOUT =              x, P =              x, M =              x, CARRYOUT = x, CARRYOUTF =
x
# A=      0, B=      0, C=              0, D=      0, BCIN=     0, PCIN=              0, OPMODE= 00000000, BCOUT =     0, PCOUT =              0, P =              0, M =              0, CARRYOUT = 0, CARRYOUTF =
0
# A=    291, B=   1110, C=              0, D=      0, BCIN=     0, PCIN=              0, OPMODE= 00000000, BCOUT =     0, PCOUT =              0, P =              0, M =              0, CARRYOUT = 0, CARRYOUTF =
0
# A=  79140, B=  89729, C= 281473667061347, D=  54793, BCIN=     0, PCIN=              0, OPMODE= 00001101, BCOUT =     0, PCOUT =              0, P =              0, M =              0, CARRYOUT = 0, CARRYOUTF =
0
# A=  79140, B=  89729, C= 281473667061347, D=  54793, BCIN=     0, PCIN=              0, OPMODE= 00001101, BCOUT =  89729, PCOUT =              0, P =              0, M =              0, CARRYOUT = 0, CARRYOUTF =
0
# A= 217618, B= 254721, C=        992211318, D= 249101, BCIN=     0, PCIN=              0, OPMODE= 00111101, BCOUT =  89729, PCOUT =              0, P =              0, M =              0, CARRYOUT = 0, CARRYOUTF =
0
# A= 217618, B= 254721, C=        992211318, D= 249101, BCIN=     0, PCIN=              0, OPMODE= 00111101, BCOUT = 254721, PCOUT =              0, P =              0, M =  7101153060, CARRYOUT = 0, CARRYOUTF =
0
# A= 125433, B= 206022, C= 281474256589482, D= 230597, BCIN=     0, PCIN=              0, OPMODE= 11100101, BCOUT = 254721, PCOUT =              0, P =              0, M =  7101153060, CARRYOUT = 0, CARRYOUTF =
0
# A= 125433, B= 206022, C= 281474256589482, D= 230597, BCIN=     0, PCIN=              0, OPMODE= 11100101, BCOUT = 206022, PCOUT =     7101153060, P =     7101153060, M = 55431874578, CARRYOUT = 0, CARRYOUTF =
0
# A=  56207, B=  27122, C= 281474775415528, D= 169678, BCIN=     0, PCIN=              0, OPMODE= 11000101, BCOUT = 206022, PCOUT =     7101153060, P =     7101153060, M = 55431874578, CARRYOUT = 0, CARRYOUTF =
0
# A=  56207, B=  27122, C= 281474775415528, D= 169678, BCIN=     0, PCIN=              0, OPMODE= 11000101, BCOUT =  27122, PCOUT =    55431874578, P =    55431874578, M = 25841957526, CARRYOUT = 0, CARRYOUTF =
0
# A= 219181, B= 206437, C=        91457290, D= 221795, BCIN=     0, PCIN=              0, OPMODE= 10000000, BCOUT =  27122, PCOUT =    55431874578, P =    55431874578, M = 25841957526, CARRYOUT = 0, CARRYOUTF =
0
# A= 219181, B= 206437, C=        91457290, D= 221795, BCIN=     0, PCIN=              0, OPMODE= 10000000, BCOUT = 206437, PCOUT = 281449134753130, P = 281449134753130, M =  1524446254, CARRYOUT = 0, CARRYOUTF =
0
# A=  52381, B=  16022, C= 281472942225421, D= 243731, BCIN=     0, PCIN=              0, OPMODE= 01010011, BCOUT = 206437, PCOUT = 281449134753130, P = 281449134753130, M =  1524446254, CARRYOUT = 0, CARRYOUTF =
0
# A=  52381, B=  16022, C= 281472942225421, D= 243731, BCIN=     0, PCIN=              0, OPMODE= 01010011, BCOUT =  16022, PCOUT = 281473452264402, P = 281473452264402, M = 45247068097, CARRYOUT = 1, CARRYOUTF =
1
# A= 215554, B= 147118, C= 281474570220239, D= 256285, BCIN=     0, PCIN=              0, OPMODE= 00100011, BCOUT =  16022, PCOUT = 281473452264402, P = 281473452264402, M = 45247068097, CARRYOUT = 1, CARRYOUTF =
1
# A= 215554, B= 147118, C= 281474570220239, D= 256285, BCIN=     0, PCIN=              0, OPMODE= 00100011, BCOUT =  96613, PCOUT = 142056889794198, P = 142056889794198, M =   839248382, CARRYOUT = 1, CARRYOUTF =
1
```

Constraint file

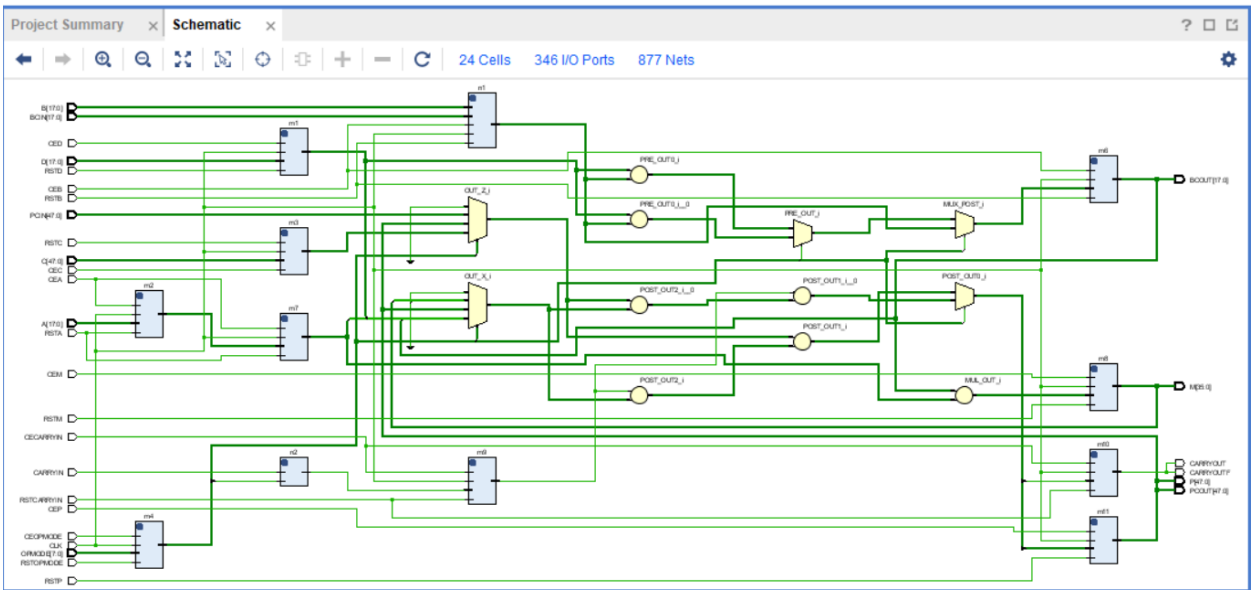
```
## Clock signal
set_property -dict {PACKAGE_PIN W5 IOSTANDARD LVCMOS33} [get_ports CLK]
create_clock -period 10.000 -name sys_clk_pin -waveform {0.000 5.000} -add
[get_ports CLK]



## Configuration options, can be used for all designs
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]

## SPI configuration mode options for QSPI boot, can be used for all designs
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 33 [current_design]
set_property CONFIG_MODE SPIx4 [current_design]


create_debug_core u_ila_0 ila
set_property ALL_PROBE_SAME_MU true [get_debug_cores u_ila_0]
set_property ALL_PROBE_SAME_MU_CNT 1 [get_debug_cores u_ila_0]
set_property C_ADV_TRIGGER false [get_debug_cores u_ila_0]
set_property C_DATA_DEPTH 1024 [get_debug_cores u_ila_0]
set_property C_EN_STRG_QUAL false [get_debug_cores u_ila_0]
set_property C_INPUT_PIPE_STAGES 0 [get_debug_cores u_ila_0]
set_property C_TRIGIN_EN false [get_debug_cores u_ila_0]
set_property C_TRIGOUT_EN false [get_debug_cores u_ila_0]
set_property port_width 1 [get_debug_ports u_ila_0/clk]
connect_debug_port u_ila_0/clk [get_nets [list CLK_IBUF_BUFG]]
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe0]
set_property port_width 18 [get_debug_ports u_ila_0/probe0]
connect_debug_port u_ila_0/probe0 [get_nets [list {B_IBUF[0]} {B_IBUF[1]}
{B_IBUF[2]} {B_IBUF[3]} {B_IBUF[4]} {B_IBUF[5]} {B_IBUF[6]} {B_IBUF[7]} {B_IBUF[8]}
{B_IBUF[9]} {B_IBUF[10]} {B_IBUF[11]} {B_IBUF[12]} {B_IBUF[13]} {B_IBUF[14]}
{B_IBUF[15]} {B_IBUF[16]} {B_IBUF[17]}]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe1]
set_property port_width 18 [get_debug_ports u_ila_0/probe1]
connect_debug_port u_ila_0/probe1 [get_nets [list {BCOUT_OBUF[0]} {BCOUT_OBUF[1]}
{BCOUT_OBUF[2]} {BCOUT_OBUF[3]} {BCOUT_OBUF[4]} {BCOUT_OBUF[5]} {BCOUT_OBUF[6]}
{BCOUT_OBUF[7]} {BCOUT_OBUF[8]} {BCOUT_OBUF[9]} {BCOUT_OBUF[10]} {BCOUT_OBUF[11]}
{BCOUT_OBUF[12]} {BCOUT_OBUF[13]} {BCOUT_OBUF[14]} {BCOUT_OBUF[15]} {BCOUT_OBUF[16]}
{BCOUT_OBUF[17]}]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe2]
set_property port_width 48 [get_debug_ports u_ila_0/probe2]
connect_debug_port u_ila_0/probe2 [get_nets [list {C_IBUF[0]} {C_IBUF[1]}
{C_IBUF[2]} {C_IBUF[3]} {C_IBUF[4]} {C_IBUF[5]} {C_IBUF[6]} {C_IBUF[7]} {C_IBUF[8]}
{C_IBUF[9]} {C_IBUF[10]} {C_IBUF[11]} {C_IBUF[12]} {C_IBUF[13]} {C_IBUF[14]}
{C_IBUF[15]} {C_IBUF[16]} {C_IBUF[17]} {C_IBUF[18]} {C_IBUF[19]} {C_IBUF[20]}
{C_IBUF[21]} {C_IBUF[22]} {C_IBUF[23]} {C_IBUF[24]} {C_IBUF[25]} {C_IBUF[26]}
{C_IBUF[27]} {C_IBUF[28]} {C_IBUF[29]} {C_IBUF[30]} {C_IBUF[31]} {C_IBUF[32]}
{C_IBUF[33]} {C_IBUF[34]} {C_IBUF[35]} {C_IBUF[36]} {C_IBUF[37]} {C_IBUF[38]}
{C_IBUF[39]} {C_IBUF[40]} {C_IBUF[41]} {C_IBUF[42]} {C_IBUF[43]} {C_IBUF[44]}
{C_IBUF[45]} {C_IBUF[46]} {C_IBUF[47]}]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe3]
set_property port_width 18 [get_debug_ports u_ila_0/probe3]
```

```
connect_debug_port u_ila_0/probe3 [get_nets [list {D_IBUF[0]} {D_IBUF[1]}
{D_IBUF[2]} {D_IBUF[3]} {D_IBUF[4]} {D_IBUF[5]} {D_IBUF[6]} {D_IBUF[7]} {D_IBUF[8]}
{D_IBUF[9]} {D_IBUF[10]} {D_IBUF[11]} {D_IBUF[12]} {D_IBUF[13]} {D_IBUF[14]}
{D_IBUF[15]} {D_IBUF[16]} {D_IBUF[17]}]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe4]
set_property port_width 18 [get_debug_ports u_ila_0/probe4]
connect_debug_port u_ila_0/probe4 [get_nets [list {A_IBUF[0]} {A_IBUF[1]}
{A_IBUF[2]} {A_IBUF[3]} {A_IBUF[4]} {A_IBUF[5]} {A_IBUF[6]} {A_IBUF[7]} {A_IBUF[8]}
{A_IBUF[9]} {A_IBUF[10]} {A_IBUF[11]} {A_IBUF[12]} {A_IBUF[13]} {A_IBUF[14]}
{A_IBUF[15]} {A_IBUF[16]} {A_IBUF[17]}]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe5]
set_property port_width 36 [get_debug_ports u_ila_0/probe5]
connect_debug_port u_ila_0/probe5 [get_nets [list {M_OBUF[0]} {M_OBUF[1]}
{M_OBUF[2]} {M_OBUF[3]} {M_OBUF[4]} {M_OBUF[5]} {M_OBUF[6]} {M_OBUF[7]} {M_OBUF[8]}
{M_OBUF[9]} {M_OBUF[10]} {M_OBUF[11]} {M_OBUF[12]} {M_OBUF[13]} {M_OBUF[14]}
{M_OBUF[15]} {M_OBUF[16]} {M_OBUF[17]} {M_OBUF[18]} {M_OBUF[19]} {M_OBUF[20]}
{M_OBUF[21]} {M_OBUF[22]} {M_OBUF[23]} {M_OBUF[24]} {M_OBUF[25]} {M_OBUF[26]}
{M_OBUF[27]} {M_OBUF[28]} {M_OBUF[29]} {M_OBUF[30]} {M_OBUF[31]} {M_OBUF[32]}
{M_OBUF[33]} {M_OBUF[34]} {M_OBUF[35]}]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe6]
set_property port_width 8 [get_debug_ports u_ila_0/probe6]
connect_debug_port u_ila_0/probe6 [get_nets [list {OPMODE_IBUF[0]} {OPMODE_IBUF[1]}
{OPMODE_IBUF[2]} {OPMODE_IBUF[3]} {OPMODE_IBUF[4]} {OPMODE_IBUF[5]} {OPMODE_IBUF[6]}
{OPMODE_IBUF[7]}]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe7]
set_property port_width 48 [get_debug_ports u_ila_0/probe7]
connect_debug_port u_ila_0/probe7 [get_nets [list {PCIN_IBUF[0]} {PCIN_IBUF[1]}
{PCIN_IBUF[2]} {PCIN_IBUF[3]} {PCIN_IBUF[4]} {PCIN_IBUF[5]} {PCIN_IBUF[6]}
{PCIN_IBUF[7]} {PCIN_IBUF[8]} {PCIN_IBUF[9]} {PCIN_IBUF[10]} {PCIN_IBUF[11]}
{PCIN_IBUF[12]} {PCIN_IBUF[13]} {PCIN_IBUF[14]} {PCIN_IBUF[15]} {PCIN_IBUF[16]}
{PCIN_IBUF[17]} {PCIN_IBUF[18]} {PCIN_IBUF[19]} {PCIN_IBUF[20]} {PCIN_IBUF[21]}
{PCIN_IBUF[22]} {PCIN_IBUF[23]} {PCIN_IBUF[24]} {PCIN_IBUF[25]} {PCIN_IBUF[26]}
{PCIN_IBUF[27]} {PCIN_IBUF[28]} {PCIN_IBUF[29]} {PCIN_IBUF[30]} {PCIN_IBUF[31]}
{PCIN_IBUF[32]} {PCIN_IBUF[33]} {PCIN_IBUF[34]} {PCIN_IBUF[35]} {PCIN_IBUF[36]}
{PCIN_IBUF[37]} {PCIN_IBUF[38]} {PCIN_IBUF[39]} {PCIN_IBUF[40]} {PCIN_IBUF[41]}
{PCIN_IBUF[42]} {PCIN_IBUF[43]} {PCIN_IBUF[44]} {PCIN_IBUF[45]} {PCIN_IBUF[46]}
{PCIN_IBUF[47]}]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe8]
set_property port_width 48 [get_debug_ports u_ila_0/probe8]
connect_debug_port u_ila_0/probe8 [get_nets [list {P_OBUF[0]} {P_OBUF[1]}
{P_OBUF[2]} {P_OBUF[3]} {P_OBUF[4]} {P_OBUF[5]} {P_OBUF[6]} {P_OBUF[7]} {P_OBUF[8]}
{P_OBUF[9]} {P_OBUF[10]} {P_OBUF[11]} {P_OBUF[12]} {P_OBUF[13]} {P_OBUF[14]}
{P_OBUF[15]} {P_OBUF[16]} {P_OBUF[17]} {P_OBUF[18]} {P_OBUF[19]} {P_OBUF[20]}
{P_OBUF[21]} {P_OBUF[22]} {P_OBUF[23]} {P_OBUF[24]} {P_OBUF[25]} {P_OBUF[26]}
{P_OBUF[27]} {P_OBUF[28]} {P_OBUF[29]} {P_OBUF[30]} {P_OBUF[31]} {P_OBUF[32]}
{P_OBUF[33]} {P_OBUF[34]} {P_OBUF[35]} {P_OBUF[36]} {P_OBUF[37]} {P_OBUF[38]}
{P_OBUF[39]} {P_OBUF[40]} {P_OBUF[41]} {P_OBUF[42]} {P_OBUF[43]} {P_OBUF[44]}
{P_OBUF[45]} {P_OBUF[46]} {P_OBUF[47]}]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe9]
set_property port_width 1 [get_debug_ports u_ila_0/probe9]
connect_debug_port u_ila_0/probe9 [get_nets [list CARRYOUTF_OBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe10]
set_property port_width 1 [get_debug_ports u_ila_0/probe10]
connect_debug_port u_ila_0/probe10 [get_nets [list CEA_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe11]
```

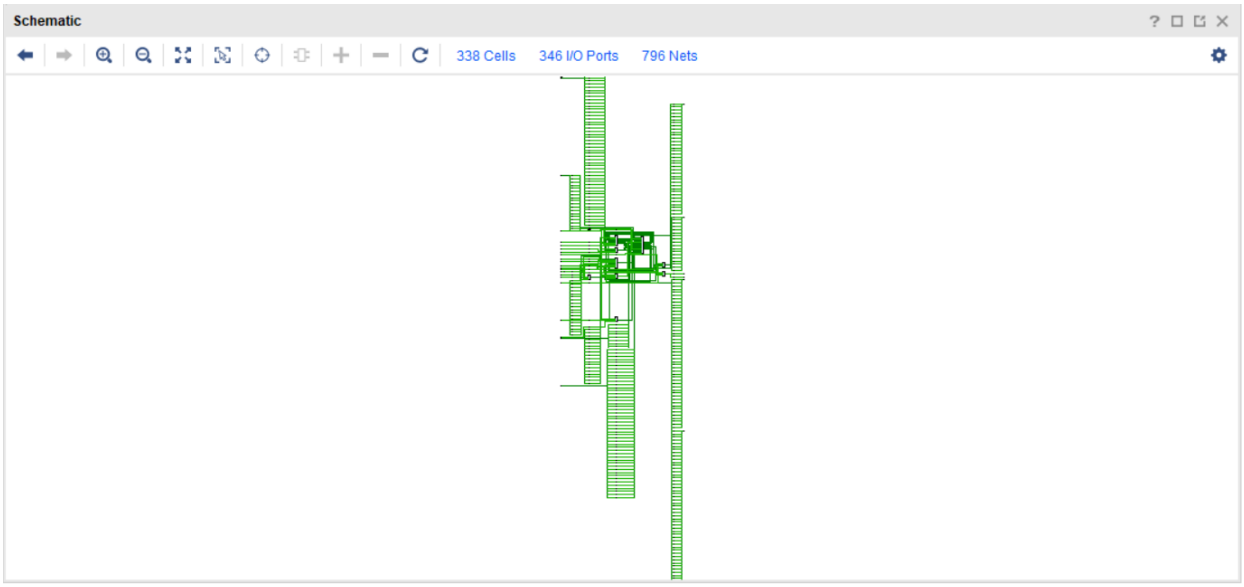
```
set_property port_width 1 [get_debug_ports u_ila_0/probe11]
connect_debug_port u_ila_0/probe11 [get_nets [list CEB_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe12]
set_property port_width 1 [get_debug_ports u_ila_0/probe12]
connect_debug_port u_ila_0/probe12 [get_nets [list CEC_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe13]
set_property port_width 1 [get_debug_ports u_ila_0/probe13]
connect_debug_port u_ila_0/probe13 [get_nets [list CECARRYIN_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe14]
set_property port_width 1 [get_debug_ports u_ila_0/probe14]
connect_debug_port u_ila_0/probe14 [get_nets [list CED_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe15]
set_property port_width 1 [get_debug_ports u_ila_0/probe15]
connect_debug_port u_ila_0/probe15 [get_nets [list CEM_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe16]
set_property port_width 1 [get_debug_ports u_ila_0/probe16]
connect_debug_port u_ila_0/probe16 [get_nets [list CEOPMODE_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe17]
set_property port_width 1 [get_debug_ports u_ila_0/probe17]
connect_debug_port u_ila_0/probe17 [get_nets [list CEP_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe18]
set_property port_width 1 [get_debug_ports u_ila_0/probe18]
connect_debug_port u_ila_0/probe18 [get_nets [list CLK_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe19]
set_property port_width 1 [get_debug_ports u_ila_0/probe19]
connect_debug_port u_ila_0/probe19 [get_nets [list RSTA_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe20]
set_property port_width 1 [get_debug_ports u_ila_0/probe20]
connect_debug_port u_ila_0/probe20 [get_nets [list RSTB_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe21]
set_property port_width 1 [get_debug_ports u_ila_0/probe21]
connect_debug_port u_ila_0/probe21 [get_nets [list RSTC_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe22]
set_property port_width 1 [get_debug_ports u_ila_0/probe22]
connect_debug_port u_ila_0/probe22 [get_nets [list RSTCARRYIN_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe23]
set_property port_width 1 [get_debug_ports u_ila_0/probe23]
connect_debug_port u_ila_0/probe23 [get_nets [list RSTD_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe24]
set_property port_width 1 [get_debug_ports u_ila_0/probe24]
connect_debug_port u_ila_0/probe24 [get_nets [list RSTM_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe25]
set_property port_width 1 [get_debug_ports u_ila_0/probe25]
connect_debug_port u_ila_0/probe25 [get_nets [list RSTOPMODE_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe26]
set_property port_width 1 [get_debug_ports u_ila_0/probe26]
connect_debug_port u_ila_0/probe26 [get_nets [list RSTP_IBUF]]
set_property C_CLK_INPUT_FREQ_HZ 300000000 [get_debug_cores dbg_hub]
```

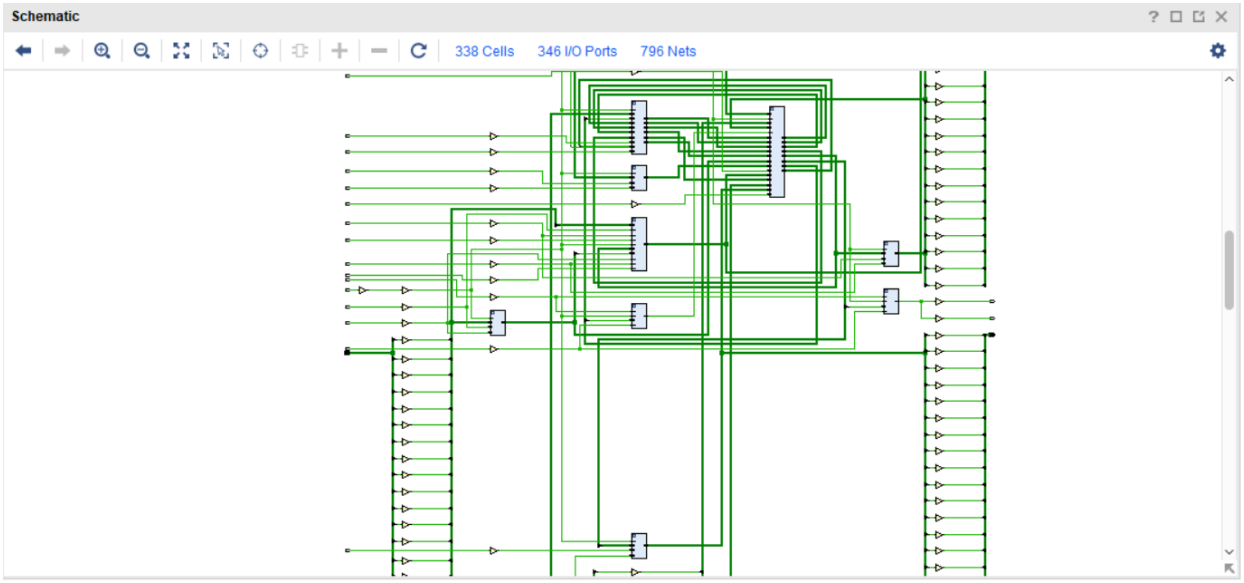
```
set_property C_ENABLE_CLK_DIVIDER false [get_debug_cores dbg_hub]
set_property C_USER_SCAN_CHAIN 1 [get_debug_cores dbg_hub]
connect_debug_port dbg_hub/clk [get_nets CLK_IBUF_BUFG]
```

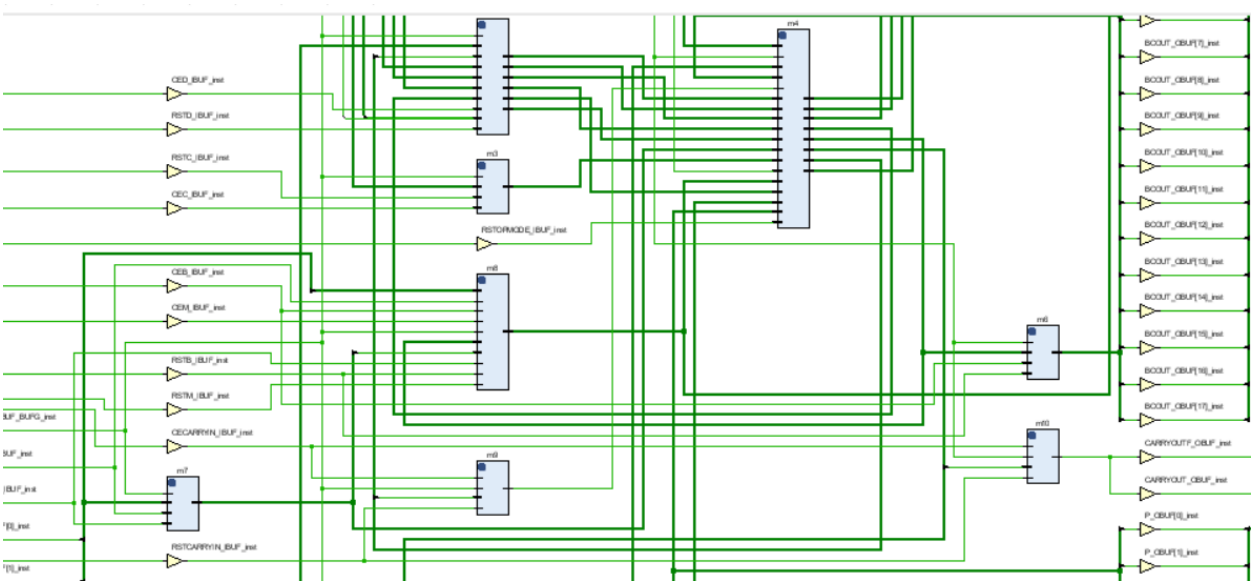
Elaboration:



- Synthesis:


Schematic
338 Cells
346 I/O Ports
796 Nets


Schematic
338 Cells
346 I/O Ports
796 Nets



Tcl Console | Messages | Log | Reports | Design Runs | Debug

Warning (42) | Info (45) | Status (19) | Show All

- Synthesis (42 warnings)
  - [Synth 8-3331] design mux2 has unconnected port CARRYIN (40 more like this)
  - [Constraints 18-5210] No constraint will be written out.

Tcl Console | Messages | Log | Reports | Design Runs | Timing | Debug

- General Information
- Timer Settings
- Design Timing Summary
- Clock Summary (1)
- Check Timing (326)
- Intra-Clock Paths
- Inter-Clock Paths
- Other Path Groups
- User Ignored Paths
- Unconstrained Paths

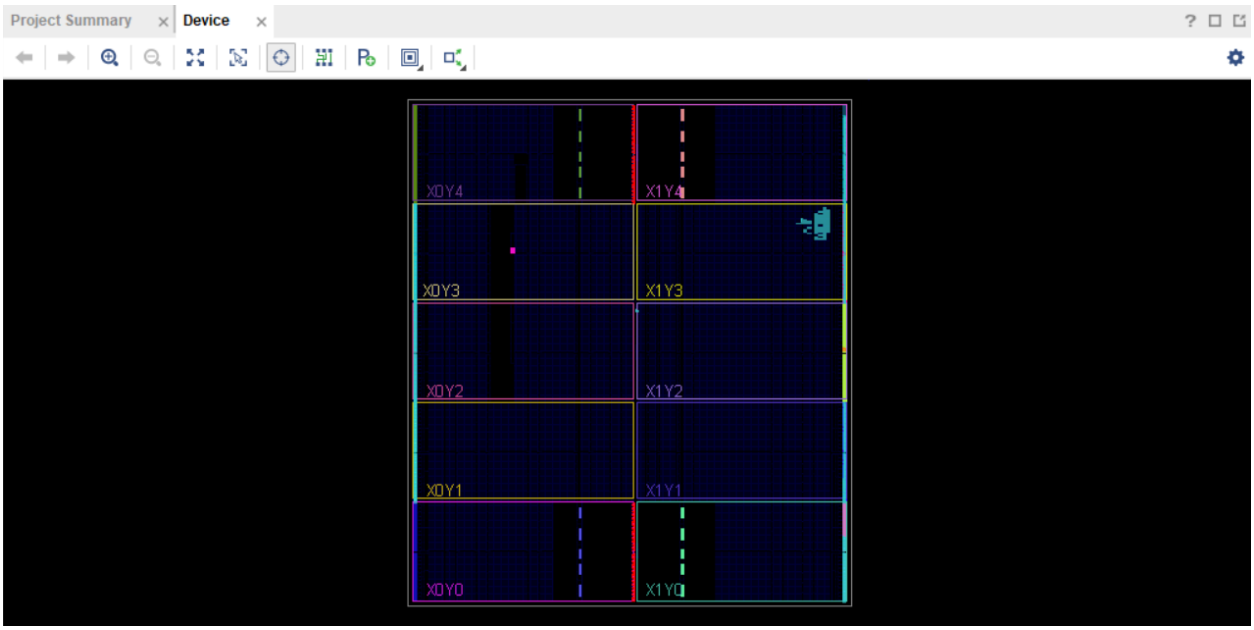
Design Timing Summary

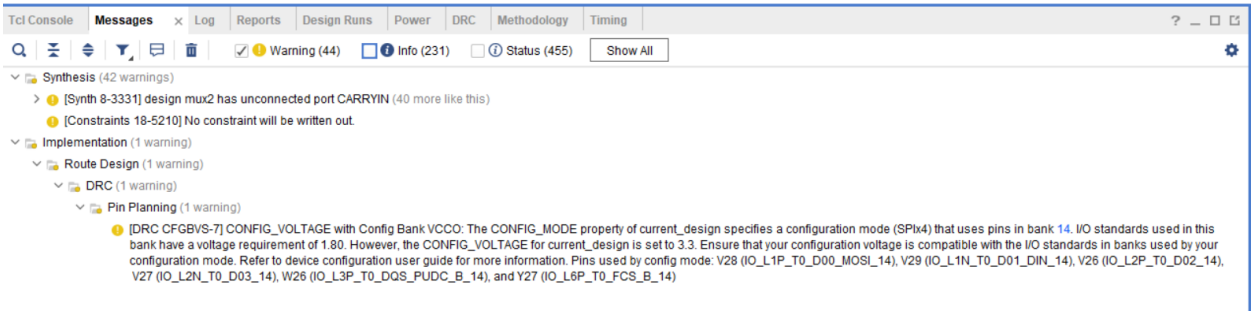
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.168 ns	Worst Hold Slack (WHS):	0.182 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	106	Total Number of Endpoints:	106	Total Number of Endpoints:	162

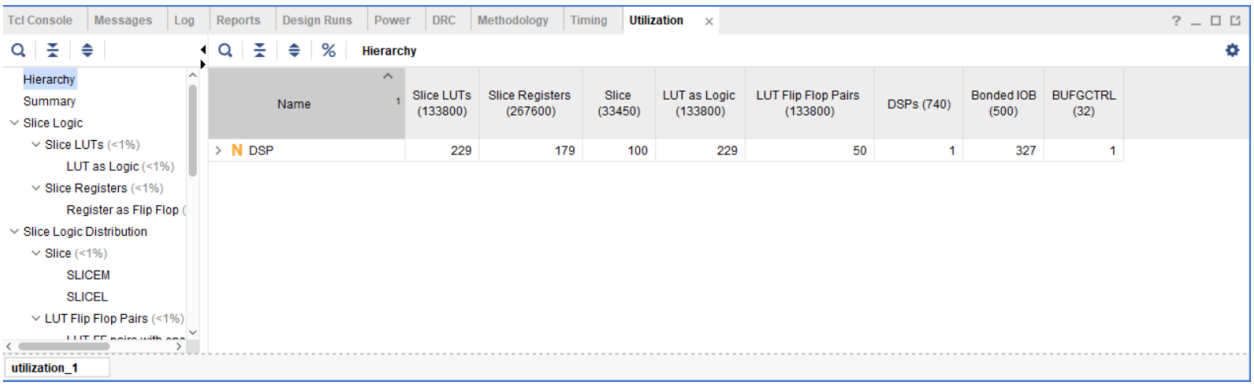
All user specified timing constraints are met.

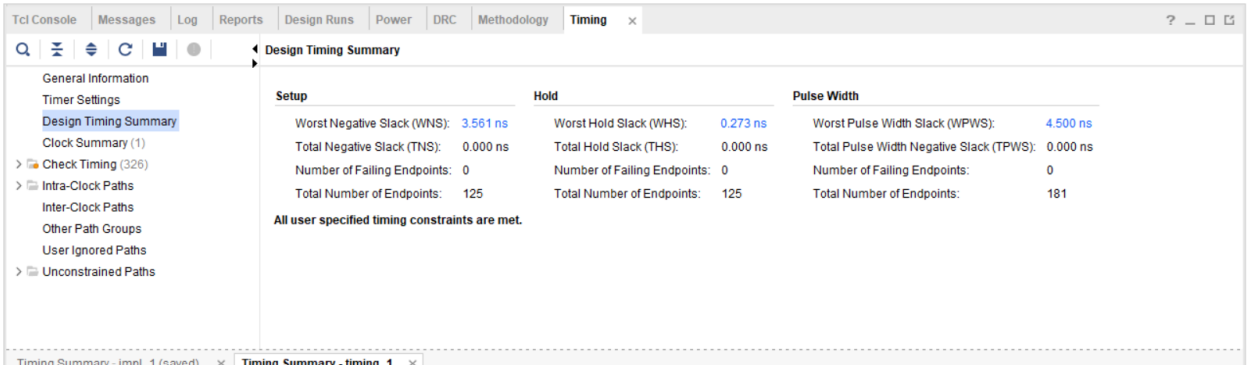
Timing Summary - timing_1

- Implementation:






Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Methodology
Timing
Utilization
Hierarchy
Summary
Slice Logic
Slice LUTs (<1%)
LUT as Logic (<1%)
Slice Registers (<1%)
Register as Flip Flop
Slice Logic Distribution
Slice (<1%)
SLICEM
SLICEL
LUT Flip Flop Pairs (<1%)
Hierarchy
Name
Slice LUTs (133800)
Slice Registers (267600)
Slice (33450)
LUT as Logic (133800)
LUT Flip Flop Pairs (133800)
DSPs (740)
Bonded IOB (500)
BUFGCTRL (32)
DSP
229
179
100
229
50
1
327
1
utilization_1


Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Methodology
Timing
Design Timing Summary
General Information
Timer Settings
Design Timing Summary
Clock Summary (1)
Check Timing (326)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
User Ignored Paths
Unconstrained Paths
Setup
Worst Negative Slack (WNS): 3.561 ns
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 125
Hold
Worst Hold Slack (WHS): 0.273 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 125
Pulse Width
Worst Pulse Width Slack (WPWS): 4.500 ns
Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 181
All user specified timing constraints are met.
Timing Summary - impl_1 (saved)
Timing Summary - timing_1