Mina Gawargious

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EDUCATION

The University of Texas at Austin | Electrical and Computer Engineering

Bachelor of Science | GPA: 3.21 | Focus: Computer Architecture & Embedded Systems **May 2021**

Master of Science | GPA: 3.24 | Focus: Architecture, Computer Systems, & Embedded Systems **May 2023**

Coursework: Computer Architecture | Microarchitecture | Digital Logic Design I & II | Operating Systems | Real-Time Operating Systems | Embedded Systems Design Lab | Software Design I & II | High Speed Computer Arithmetic | System-on-Chip Design | Embedded IoT | Cross-Layer Machine Learning Algorithm/Hardware Co-Design | Multicore Computing | VLSI | Parallel Computer Architecture | Computer Architecture Prediction Mechanisms | Algorithms

EXPERIENCE

Digital Design Engineering, *Silicon Labs* **May 2023-Present**

- Refined Energy Management Unit to improve temperature compensation for signal and RAM voltage references
- Aided in writing GPIO architecture specification, collaborating with complementary teams to determine features and evaluate tradeoffs based on performance requirements, system limitations, and deadlines
- Expanded GPIO subsystem to add new configurability, integrated changes into top-level SoC, and updated tests in C to verify new configurability
- Streamlined internal workflow Python scripts to provide up to 15x speedup and allow them to run on Jenkins CI/CD pipeline, reducing manual labor and increasing efficiency

Digital Design Engineering Intern, *MediaTek* **January 2023-May 2023**

- Drove RTL Lint cleaning process using Synopsys Spyglass Lint
- Utilized QuestaCDC to ensure Clock-Domain-Crossing is properly checked
- Leveraged Perl, Python, and Bash scripting to automate lint waiver generation and other internal scripts to speed up RTL design and verification for Dimensity 9400 SoC using TSMC's 3nm process

Digital Design Engineering Intern, *Silicon Labs* **August 2022-December 2022**

- Assisted in RTL development of Energy Management Unit (EMU) for low-power wireless SoCs, learning new industry-standard tools and methodologies such as Perforce, Questa Visualizer, and UVM
- Learned UVM verification environment and updated UVM sequences to test new features of EMU

Systems Engineering Intern, *Silicon Labs* **May 2022-August 2022**

- Created React Native app and PyQt5 GUI to significantly speed up radio testing
- Packet-Error-Rate (PER) data was presented to marketing team to aid with commercialization of EFR32FG25 Sub-GHz Wireless SOCs

Graduate Research Assistant, *Mobile and Pervasive Computing Lab at UT Austin* **September 2021-May 2022**

- Used PyTorch to develop scalable software for Federated Machine Learning on Raspberry Pis to show scalability of ML models on constrained edge devices
- Designed website using React Native to display and control training loss and progress of Raspberry Pis

PROJECTS

Microarchitecture Project - Verilog:

- Worked in a team of 3 to design a 7-stage pipeline implementing part of Intel's x86 IA-32 ISA in structural Verilog
    - Personal role: designed writeback cache, instruction-length decode logic, and part of bus architecture

Operating Systems Labs - C:

- Worked with a partner to add support for user programs, virtual memory, and an improved file system with support for subdirectories and file growth to the Pintos Operating System
    - Learned to manage, update, and debug large prewritten codebase with 30,000+ lines of code across 50+ files by using GDB and git

Real-Time Operating Systems Labs - C, ARM Assembly:

- Worked with a partner to write an operating system for the TM4C microcontroller, with round-robin and priority scheduling, a basic shell, a file system using indexed allocation, and network support using TCP/IP
    - Personal role: wrote the scheduling algorithms and majority of file system