Lab 1 Setup and Synthesis Flow

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实验步骤

按照要求修改文件common_setup.tcl如下：

```
set ADDITIONAL_SEARCH_PATH        "../ref/libs/mw_lib/sc/LM .rtl/ .scripts/"  ;#
Directories containing logical libraries,

# logical design and script files.

set TARGET_LIBRARY_FILES          sc_max.db ;#  Logical technology library file

set SYMBOL_LIBRARY_FILES          sc.sdb;#  Symbol library file
```

在Design Compiler的终端输入如下命令进行验证：

```
dc_shell> source common_setup.tcl
dc_shell> source dc_setup.tcl
dc_shell> read_verilog rtl/TOP.v
dc_shell> source scripts/TOP.con
dc_shell> compile_ultra
dc_shell> report_constraint -all_violators
dc_shell> report_timing
dc_shell> write -format verilog -hier -output mapped/TOP.gv
dc_shell> write -format ddc -hier -output mapped/TOP.ddc
```

实验结果

成功输出了设计文件TOP.gv和TOP.ddc。

思考题

1. What is the Link library?
   * sc_max.db

2. What is the Target library?
   sc_max.db

3. What is the Symbol library?
   sc.sdb

4. What user directories have been added to the Search path?
   ../ref/libs/mw lib/sc/LM ./rtl . /scripts