Lab 2 Timing Constraints

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实验步骤

按照要求修改文件./scripts/MY_DESIGN.con如下：

```
#   CLOCK DEFINITION
create_clock -period    3.0    [get_ports clk]
set_clock_latency -source  -max   0.7     [get_clocks clk]
set_clock_latency -max    0.3    [get_clocks clk]
set_clock_uncertainty -setup    0.15    [get_clocks clk]
set_clock_transition   0.12     [get_clocks clk]

#   INPUT TIMING
set_input_delay -max    0.45    -clock clk [get_ports data*]
set_input_delay -max    0.4     -clock clk [get_ports sel]

#   OUTPUT TIMING
set_output_delay -max    0.5     -clock clk [get_ports out1]
set_output_delay -max    2.04     -clock clk [get_ports out2]
set_output_delay -max    0.4     -clock clk [get_ports out3]

#   COMBINATIONAL LOGIC TIMING
set_input_delay -max    0.2    -clock clk [get_ports Cin*]
set_output_delay -max    0.2    -clock clk [get_ports Cout]
```

在Design Compiler的终端输入如下命令进行验证：

```
dc_shell> source common_setup.tcl
dc_shell> source dc_setup.tcl
dc_shell> read_verilog rtl/MY_DESIGN.v
dc_shell> source scripts/MY_DESIGN.con
dc_shell> check_timing
dc_shell> compile_ultra
dc_shell> report_clock
dc_shell> report_clock -skew
dc_shell> report_port -verbose
dc_shell> write_script -out scripts/MY_DESIGN.sdc
dc_shell> write -format ddc -hier -output unmapped/MY_DESIGN.ddc
```

实验结果

成功输出了约束文件MY_DESIGN.sdc和设计文件MY_DESIGN.ddc。其中约束文件如下：

```
################################################################################

# Created by write_script -format dctcl on Fri May 22 15:25:33 2020

################################################################################

# Set the current_design #
current_design MY_DESIGN

set_units -time ns -resistance kOhm -capacitance pF -voltage V -current uA
remove_wire_load_model
set_local_link_library {sc_max.db}
set_register_merging [current_design] 17
set_map_only [get_cells intadd_0/U4]
set_map_only [get_cells intadd_0/U3]
set_map_only [get_cells intadd_2/U3]
set_map_only [get_cells intadd_2/U2]
set_map_only [get_cells intadd_1/U4]
set_map_only [get_cells intadd_1/U3]
set_map_only [get_cells intadd_2/U4]
set_map_only [get_cells intadd_1/U2]
set_map_only [get_cells intadd_0/U2]
set_register_merging [get_cells {R3_reg[1]}] 17
set_register_merging [get_cells {R3_reg[3]}] 17
set_register_merging [get_cells {R3_reg[2]}] 17
set_register_merging [get_cells {R3_reg[4]}] 17
set_register_merging [get_cells {R1_reg[0]}] 17
set_register_merging [get_cells {R1_reg[1]}] 17
set_register_merging [get_cells {R1_reg[2]}] 17
set_register_merging [get_cells {R1_reg[3]}] 17
set_register_merging [get_cells {R1_reg[4]}] 17
set_register_merging [get_cells {R2_reg[0]}] 17
set_register_merging [get_cells {R2_reg[1]}] 17
set_register_merging [get_cells {R2_reg[2]}] 17
set_register_merging [get_cells {R2_reg[3]}] 17
set_register_merging [get_cells {R2_reg[4]}] 17
set_register_merging [get_cells {R4_reg[0]}] 17
set_register_merging [get_cells {R4_reg[1]}] 17
set_register_merging [get_cells {R4_reg[2]}] 17
set_register_merging [get_cells {R4_reg[3]}] 17
set_register_merging [get_cells {R4_reg[4]}] 17
set_switching_activity -period 1 -toggle_rate 0.0333333 -static_probability    \
0.5 [get_ports {Cin1[4]}]
create_clock [get_ports clk]  -period 3  -waveform {0 1.5}
set_clock_latency -max 0.3  [get_clocks clk]
set_clock_latency -source -max 0.7  [get_clocks clk]
set_clock_uncertainty -setup 0.15  [get_clocks clk]
set_clock_transition -max -rise 0.12 [get_clocks clk]
set_clock_transition -max -fall 0.12 [get_clocks clk]
set_clock_transition -min -rise 0.12 [get_clocks clk]
set_clock_transition -min -fall 0.12 [get_clocks clk]
```

```
set_input_delay -clock clk  -max 0.45  [get_ports {data1[4]}]
set_input_delay -clock clk  -max 0.45  [get_ports {data1[3]}]
set_input_delay -clock clk  -max 0.45  [get_ports {data1[2]}]
set_input_delay -clock clk  -max 0.45  [get_ports {data1[1]}]
set_input_delay -clock clk  -max 0.45  [get_ports {data1[0]}]
set_input_delay -clock clk  -max 0.45  [get_ports {data2[4]}]
set_input_delay -clock clk  -max 0.45  [get_ports {data2[3]}]
set_input_delay -clock clk  -max 0.45  [get_ports {data2[2]}]
set_input_delay -clock clk  -max 0.45  [get_ports {data2[1]}]
set_input_delay -clock clk  -max 0.45  [get_ports {data2[0]}]
set_input_delay -clock clk  -max 0.4  [get_ports sel]
set_input_delay -clock clk  -max 0.2  [get_ports {Cin1[4]}]
set_input_delay -clock clk  -max 0.2  [get_ports {Cin1[3]}]
set_input_delay -clock clk  -max 0.2  [get_ports {Cin1[2]}]
set_input_delay -clock clk  -max 0.2  [get_ports {Cin1[1]}]
set_input_delay -clock clk  -max 0.2  [get_ports {Cin1[0]}]
set_input_delay -clock clk  -max 0.2  [get_ports {Cin2[4]}]
set_input_delay -clock clk  -max 0.2  [get_ports {Cin2[3]}]
set_input_delay -clock clk  -max 0.2  [get_ports {Cin2[2]}]
set_input_delay -clock clk  -max 0.2  [get_ports {Cin2[1]}]
set_input_delay -clock clk  -max 0.2  [get_ports {Cin2[0]}]
set_output_delay -clock clk  -max 0.5  [get_ports {out1[4]}]
set_output_delay -clock clk  -max 0.5  [get_ports {out1[3]}]
set_output_delay -clock clk  -max 0.5  [get_ports {out1[2]}]
set_output_delay -clock clk  -max 0.5  [get_ports {out1[1]}]
set_output_delay -clock clk  -max 0.5  [get_ports {out1[0]}]
set_output_delay -clock clk  -max 2.04  [get_ports {out2[4]}]
set_output_delay -clock clk  -max 2.04  [get_ports {out2[3]}]
set_output_delay -clock clk  -max 2.04  [get_ports {out2[2]}]
set_output_delay -clock clk  -max 2.04  [get_ports {out2[1]}]
set_output_delay -clock clk  -max 2.04  [get_ports {out2[0]}]
set_output_delay -clock clk  -max 0.4  [get_ports {out3[4]}]
set_output_delay -clock clk  -max 0.4  [get_ports {out3[3]}]
set_output_delay -clock clk  -max 0.4  [get_ports {out3[2]}]
set_output_delay -clock clk  -max 0.4  [get_ports {out3[1]}]
set_output_delay -clock clk  -max 0.4  [get_ports {out3[0]}]
set_output_delay -clock clk  -max 0.2  [get_ports {Cout[4]}]
set_output_delay -clock clk  -max 0.2  [get_ports {Cout[3]}]
set_output_delay -clock clk  -max 0.2  [get_ports {Cout[2]}]
set_output_delay -clock clk  -max 0.2  [get_ports {Cout[1]}]
set_output_delay -clock clk  -max 0.2  [get_ports {Cout[0]}]
```

思考題

1. What is the target library file name?
   sc_max.db

2. What is the target library name?
   cb13fs120_tsmc_max

3. What is the “Time Unit” of the target library?
   1ns