实验五 存储器

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实验源码

```
module mem(
    inout [7:0] data,
    input [4:0] addr,
    input read,
    input write
);

reg [7:0] memory [31:0];

always @ (posedge write)
begin
    memory[addr] = data;
end

assign data = read ? memory[addr] : 8'bzzzz_zzzz;
endmodule
```

测试代码与结果

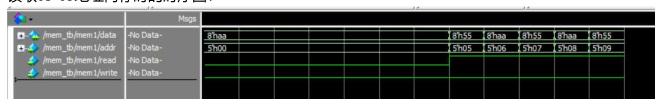
使用提供的测试代码进行测试。

```
# Setting all memory cells to zero... 0.0 ns
#
# Reading from one memory address... 64.0 ns
#
# Setting all memory cells to alternating patterns... 84.0 ns
#
# Doing block read from five memory addresses... 158.0 ns
#
# Completed Memory Tests With 0 Errors!
```

向内存中05-09地址写入的时序图:

⊒ •	Msgs											
	8'h00	8 haa	[8'h55	(8'haa	(8'h55	(8'haa	[8h55	8 haa	[8h55	8 haa	8'h55	8'haa
/mem_tb/mem1/addr 5'h0a 5'h0a 1'h0	5'h0a	[5h00	5'h01	5'h02	5'h03	5'h04	5 h05	5°h06	5h07	5'h08	5'h09	5'h0a

读取05-09地址内存时的时序图:



测试结果表明,模块设计正确,各个功能工作正常。