**lab1 Setup andSynthesis Flow**

cd DC\_lab/lab1

**Task 1. Examine and modify the setup files**

|  |  |
| --- | --- |
| **User-defined variable** | **Directory or File Names** |
| ADDITIONAL\_SEARCH\_PATH | ../ref/libs/mw lib/sc/LM ./rtl . /scripts |
| TARGE T\_LIBRARY\_FILES | sc\_max.db |
| SYMBOL\_LIBRARY\_FILES | sc.sdb |

**Task 2. Invoke Design Compiler**

design\_shell-t or design\_vision

read\_verilog

**Task 3. Constrain TOP with a Script file**

source TOP.con

**Task 4. Compile or Map to Vendor-Specific Gates**

compile\_ultra

**Task 5. Generate Reports and Analyze Timing**

report\_constraint -all\_violators

report\_timing

**Task 6. Save the Optimized Design**

write -format verilog -hier -output mapped/TOP.gv

write -format ddc -hier -output mapped/TOP.ddc

**Task 7. Remove Designs and Exit Design Vision**

remove\_design -designs

Question 1. What is the Link library?

Question 2. What is the Target library?

Question 3. What is the Symbol library?

Question 4. What user directories have been added to the Search path?