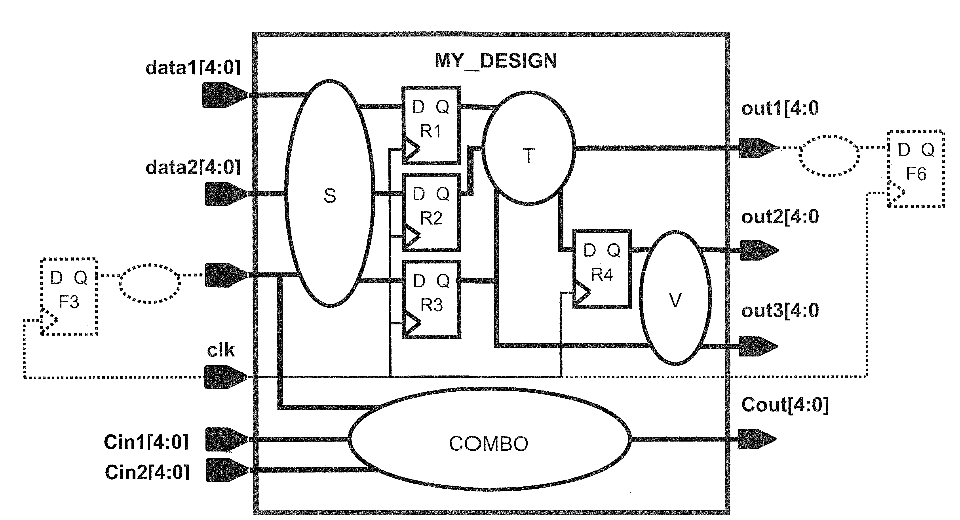
**lab2 Timing Constraints**

cd DC\_lab/lab2



**Design Specification**

|  |  |
| --- | --- |
| **Clock Definition** | **1.** Clock **clk** has a frequency of **333.3 Mhz.**  2. The maximum external clock generator delay to the clock port is **700ps.** (HINT: source latency)  3. The maximum insertion delay from the clock port to all the register clock pins is **300ps +/- 30ps.** (HINT:Treat the 300ps as network latency and the +/-30ps as clock skew)  4. The clock period can fluctuate **+/- 40ps** due to jitter.  5. Apply **50ps** of "setup margin" to the clock period.  6. The worst case rise/fall transition time of any clock pin is **120 ps.** |
| **Register Setup Time** | Assume a maximum setup time of **0.2ns** for any register in MY\_DESIGN |
| **Input Ports (sequential logic)** | 1. The maximum delay from ports **data1** and **data2** through the internal input logic **S** is **2.2ns**.  2. The latest F3 data arrival time at the **sel** port is **1.4ns** absolute time. (HINT: Input delav is specified as , relative time - relative to the launching clock edge) |
| **Output Ports (sequential logic)** | 1. The maximum delay of the external combo logic at port **out1**is **420ps**; F6 has a setup time of **80ps**.  2. The maximum internal delay to **out2** is **810ps**.  3. The **out3** port has a **400ps** setup time requirement with respect to its capturing register clock pin. |
| **Combinational Logic** | The maximum delay from **Cin1** and **Cin2** to **Cout** is **2.45ns**. (HINT: Use appropriate input and output delay constraints with respect to clock clk ) |

**Task 1. Determine the Target Library's *Time Unit***

more common\_setup. tcl

dc shell–t | tee -i lab2.log

dc shell–t> read\_db sc\_max.db

dc shell–t> list\_libs

redirect -file lib.rpt {report\_lib <library\_NAME>}

**Task 2. Create a Timing Constraints File**

create a new file called MY\_DESIGN.con.

dcprocheck scripts/MY\_DESIGN.con

# CLOCK DEFINITION

create\_clock -period [get\_ports clk]

set\_clock\_latency -source -max [get\_clocks clk]

set\_clock\_latency -max [get\_clocks clk]

set\_clock\_uncertainty -setup [get\_clocks clk]

set\_clock\_transition [get\_clocks clk]

# INPUT TIMING

set\_input\_delay -max -clock clk [get\_ports data\*]

set\_input\_delay -max -clock clk [get\_ports sel]

# OUTPUT TIMING

set\_output\_delay -max -clock clk [get\_ports out1]

set\_output\_delay -max -clock clk [get\_ports out2]

set\_output\_delay -max -clock clk [get\_ports out3]

# COMBINATIONAL LOGIC TIMING

set\_input\_delay -max -clock clk [get\_ports Cin\*]

set\_output\_delay -max -clock clk [get\_ports Cout]

**Task 3. Apply Constraints and Validate**

invoke the DC shell from the lab2 directory.

source scripts/MY\_DESIGN.con

check timing

compile\_ultra

report\_clock

report\_clock -skew

report\_port –verbose

write\_script -out scripts/MY\_DESIGN.sdc

write -format ddc -hier -out unmapped/MY\_DESIGN.ddc

Question 1. What is the target library file name?

Question 2. What is the target library name?

Question 3. What is the “Time Unit” of the target library?