VERIFICATION PLAN

AHB-LITE INTERFACE

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AHB-Lite Protocol:

AHB-Lite implements the features required for high-performance, high clock frequency systems including:

• burst transfers
• Single-clock edge operation
• Non-tristate implementation
• Wide data bus configurations, 64, 128, 256, 512, and 1024 bits.

The most common AHB-Lite slaves are internal memory devices, external memory interfaces, and high bandwidth peripherals. Although low-bandwidth peripherals can be included as AHB-Lite slaves, they typically reside on the AMBA Advanced Peripheral Bus (APB) for system performance reasons. Bridging between this higher level of bus and APB is done using an AHB-Lite slave, known as an APB bridge. Figure 1-1 shows a single master AHB-Lite system design with one AHB-Lite master and three AHB-Lite slaves. The bus interconnect logic consists of one address decoder and a slave-to-master multiplexor. The decoder monitors the address from the master so that the appropriate slave is selected and the multiplexor routes the corresponding slave output data back to the master.

Working of Protocol:

Global Signals:

Name	Destination	Description
HCLK	Clock source	Clock source for all operations on the protocol. Input signals are sampled at rising edge and changes in output signals happen after the rising edge
HRESTn	Reset Controller	Asynchronous primary reset for all bus elements

Master Signals:

Name	Destination	Description
HADDR [31:0]	Slave and Decoder	Address bus of 32 bits
HBURST [2:0]	Slave	Indicates the type of burst signal including wrapping and incrementing bursts
HSIZE [2:0]	Slave	Indicates the size of transfer from 8 bits to 1024 bits

Slave Signals:

Name	Destination	Description
HRDATA [31:0]	Multiplexor	Read data bus to transfer the data from a Slave's location to the Master via multiplexor
HREADYOUT	Multiplexor	Indicates transfer has finished on the bus and is used to extend the data phase
HRESP	Multiplexor	Provides additional information that the transfer was successful or failed

Decoder Signals:

Name	Destination	Description
HSELx Note: x is a unique identifier for AHB lite slave	Slave	Indicates current transfer is for intended for selected slave

Multiplexor Signals:

Name	Destination	Description
HRDATA [31:0]	Master	Read data bus to rout to Master
HREADY	Master and Slave	Indicates completion of previous transfer
HRESP	Master	Transfer response

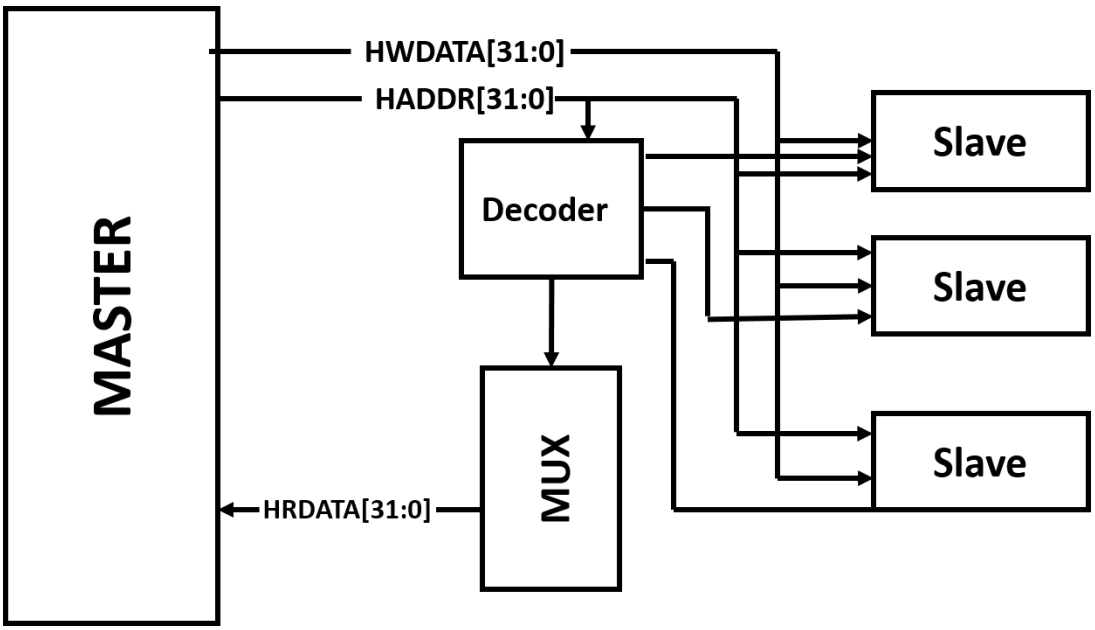

Fig 1.1

Working Protocol

The master starts a transfer by driving the address and control signals. These signals provide information about the address, direction, width of the transfer, and indicate if the transfer forms part of a burst. Transfers can be of different type's for instance single, incrementing bursts that do not wrap at address boundaries, wrapping bursts that wrap at particular address boundaries, etc. The write data bus moves data from the master to a slave, and the read data bus moves data from a slave to the master.

Every transfer consists of two phases:

1) Address phase: one address and control cycle
2) Data phase: one or more cycles for the data.

A slave cannot request that the address phase is extended and therefore all slaves must be capable of sampling the address during this time. However, a slave can request that the master extends the data phase by using HREADY. This signal when LOW, causes wait states to be inserted into the transfer and enables the slave to have extra time to provide or sample data. The slave uses a response signal to indicate the success or failure of a transfer.

VERIFICATION PLAN

No	Features	Test Description	Ref.	Type	Result	Expected outcome	Comments
1	Write Transfer from Master to Slave	An **address B** is driven onto the bus. The slave will sample the **address B** on the next rising clock edge. Afterward, the slave will drive the **HREADY** response. This response is sampled on the next rising edge of **HCLK**.	3.1	TR		Address phase should not be more than one cycle. The slave must only sample address when **HREADY** is high. The **Data (B)** must be written at the **address B** and a completed transfer is signalled i.e., **HRESP** should be low and **HREADY** should be high.	**HWRITE** is high, indicating a write transfer and the master broadcasts data on the write data bus, **HWDATA [31:0].**
2	Read Transfer from Slave to Master	An **address B** is driven onto the bus. The slave will sample the **address B** on the next rising clock edge. Afterward, the slave will drive the **HREADY** response. This response is sampled on the next rising edge of HCLK.	3.1	TR		The address phase should not be more than one cycle. The slave must only sample address on when **HREADY** is high. The **Data (B)** must be read from the **address B** and completed transfer is signalled i.e., **HRESP** should be low and	**HWRITE** is low, a read transfer is performed and the slave must generate the data on the read data bus, HRDATA [31:0].

						HREADY should be high	
3	Random transfers	Random addresses A, B, C and D with zero wait states are driven onto the bus. The slave will sample the addresses A, B, C and D on rising clock edged of their address phase.	3.1	TR		Just like in test 1 and test 2 the slave must only sample the address A, B, C and D when **HREADY** is high and completion of transfer must be signalled by the slave i.e., **HRESP** should be low and **HREADY** should be high. Based on the basic transfer type i.e., write or read **Data(B)**, Data(B), Data(C) and Data(D) will be driven on the HWDATA [31:0] bus or HRDATA [31:0] bus respectively.	Based on the type of transfer i.e., read transfer or write transfer **HWRITE** will be set low and high respectively.
4	Read or Write transfer with wait states	An **address B** is driven onto the bus. The slave will sample the address on the rising edge of the clock provided that **HREADY** is high. After sampling the address. Wait states are added in the data phase by keeping **HREADY** low for two cycles after we	3.1 5.1 5.1.2	A		During the wait state, the slave must provide transfer pending response i.e., **HREADY** and **HRESP** must be low before completion. Afterward, a successful complete transfer is signalled when **HREADY** is high	Adding wait states causes latency in the read or write transfer. The master cannot cancel the transfer.

		have sampled the address				and **HRESP** is low.	
5	Multiple transfers extended	Three addresses A, B, and C are driven onto the bus. The addresses are sampled on rising clock edges during their address phases. Wait states are added using **HREADY**. Transfer to **address B** is one wait state. Transfer to address B is two wait states.	3.1	TR		Since the data phase of address, A is extended the address phase of B is extended by one cycle. The address phase of C is extended by three cycles.	When a transfer is extended it has side effects of extending the address phase of the next transfer.
6	Write followed by Read transfer	An **address B** is driven onto the bus twice. The slave will sample the **address B** on the first and second rising clock edge for write and read transfer respectively. Firstly, **HWRITE** is high, indicating a write transfer and the master broadcasts data on the write data bus, HWDATA [31:0]. Lastly, **HWRITE** is set low, a read transfer is performed and the slave must generate the data on the read data bus, HRDATA [31:0].	3.1	TR		Based on the specifications of the memory. Read transfer should produce the updated **Data (B)**.	During the Write transfer the completed transfer is signalled i.e., **HRESP** should be low and **HREADY** should be high. During the Read transfer the completed transfer is signalled i.e., **HRESP** should be low and **HREADY** should be high.
7	Read followed by Write transfer	An **address B** is driven onto the bus twice. The slave will	3.1	TR		Based on the specifications of the memory.	During the Read transfer the

		sample the **address B** on the first and second rising clock edge for read and write transfer respectively. Firstly, **HWRITE** is set low, a read transfer is performed and the slave must generate the data on the read data bus, HRDATA [31:0]. Lastly, **HWRITE** is high, indicating a write transfer and the master broadcasts data on the write data bus, HWDATA [31:0].				Read transfer should produce the **Data(B)** which was stored before Write transfer. The Write transfer will update **Data(B)**.	completed transfer is signaled i.e., **HRESP** should be low and **HREADY** should be high. During the Write transfer the completed transfer is signaled i.e., **HRESP** should be low and **HREADY** should be high.
8	Wrapping burst types: • WRAP4 • WRAP8 • WRAP16	We have transfer size of 4-byte (32-bit) which is a word. In WRAP4, firstly **address B**+4, **address B**+8 and **address B**+12 is driven onto the bus which are sampled by the slave on the rising clock edges of their address phases. After the transfer at **address B**+12, we have reached the address boundary therefore next transfer is wrapped to **address B**.	3.5 3.5.3	A		In WRAP4 the burst is a four-beat burst of word transfers; the addresses wrap at 16-byte boundary. In WRAP8 the burst is an eight-beat burst of word transfers; the addresses wrap at 32-byte boundary. In WRAP16 the burst is a sixteen-beat burst of word transfers; the addresses wrap at 64-byte boundary.	Wrapping bursts wrap when they cross an address boundary. **Address boundary = HBURST x HSIZE** Note: Different combinations of read and write transfers can be used which were implicitly

		Similarly, we drive addresses on the bus for WRAP8 and WRAP16 to check if they wrap at the address boundaries.				For all the above scenarios the slave will provide a completed transfer signal.	checked in previous tests.
9	Incrementing burst type: • INCR4 • INCR8 • INCR16	We have transfer size of 4-byte (32-bit) which is a word. Firstly, **address B**+4, B+8 and B+12 is driven onto the bus which are sampled by the slave on the rising clock edges of their address phases. After the transfer at **address B**+12, we have reached the address boundary. Since we are using incrementing burst type. Instead of wrapping around it will transfer to the next location which is B+16. Similarly, we drive addresses on the bus for INCR8, INCR 16 to check if they increment at the address boundaries.				In INCR4, the transfers are incremented by 4. In INCR8, the transfers are incremented by 8. In INCR16, the transfers are incremented by 16. For all the above scenarios the slave will provide a completed transfer signal.	Incrementing bursts access sequential locations. The addresses of each transfer in the burst are an increment of the previous address.
10	Incrementing burst type:	First burst is driven on the bus which consists of two half				In first burst, the transfer address is	

	INCR and undefined length burst	word transfers at an **address B**. The second burst is read consisting of three word read transfers starting at address B				incremented by two. In the second burst, the transfer address is incremented by four. For all the above scenarios the slave will provide a completed transfer signal.	
11	Protection signals HPROT [3:0]: • 4'b0000 • 4'b1111	An **address B** is driven on the bus. The timing of HPROT and address bus must be same. The must remain constant throughout the burst transfer. The protection signal HPROT [3:0] = 4'b0000 corresponds to non-cacheable, non-buffer able, unprivileged opcode fetch. The protection signal HPROT [3:0] = 4'b1111 corresponds to cacheable, buffer able, privileged data access.	3.7	A		The protection signal basically gives extra information which can be used to determine an exception for instance illegal instruction, illegal access and etc. For instance, **Data (B)** can't be accessed because only a privileged level can access that information. The response is entirely dependent how the design engineer implemented it.	The test is dependent on master's ISA (Instruction Set Architecture) and design. Used by a module that wants to implement some level of protection.
12	HRESETn	It is an active low signal. When HRESETn is asserted then **HREADYOUT** must be HIGH and	7.1.2	A		All the bus elements will reset and HRESETn is disserted synchrounsly	

		HTRANS must IDLE					
13	Cancellation of transfer	After a master started a transfer, master cannot cancel a transfer.	5.1	A		The transfer should be completed once the master started	
14	Master Signal: IDLE HTRANS [1:0] =b00	An address A is driven onto the bus. An IDLE transfer is inserted to this address.	3.2	A		The transfer must be ignored by the slave. Slave provides a zero-wait OKAY response.	Master Signal: IDLE HTRANS [1:0] =b00
15	Master Signal: BUSY HTRANS [1:0] =b01	Address A and B are driven onto the bus. When a BUSY transfer is inserted on address A then the address and control signals must reflect the next burst transfer i.e., address B. A sequential transfer is signalled for address B.	3.2	A		After the complete transfer signal from the slave for address A; address B is sampled during the sequential transfer.	Master Signal: BUSY HTRANS [1:0] =b01
16	Transfer type changes from IDLE to NONSEQ during waited states	Address A, B, C, and X are driven onto the bus. One IDLE transfer is inserted to address B and address C. The transfer type is changed to NONSEQ and initiates a transfer to address x. With HREADY low, the HTRANS is kept constant.	3.6.1	A		The slave will sample address A at the rising clock edge of the address phase. After successful transfer to address A the slave will ignore the IDLE transfers i.e., transfers associated with addresses B and C will be neglected.	Transfer type changes from IDLE to NONSEQ during waited states

						Then, address B will be sampled in its address phase. Transfer to address B will complete and slave will signal a complete transfer response.	
17	Transfer type changes from BUSY to SEQ during waited states for a fixed-length burst	A sequential address A is driven onto the bus. Then a busy transfer is inserted and address B is driven on the bus. Wait states are added by keeping HREADY low. A sequential address C is driven on the bus. The transfer type changes from BUSY to SEQ. HTRANS is kept constant and slaves must keep HREADY low during this phase. Then HREADY is set high.	3.6.1	A		Transfer to address A completes when HREADY is set high. In the next cycle, the transfer to address B completes, and then in the next cycle the transfer to address C completes.	Transfer type changes from BUSY to SEQ during waited states for a fixed-length burst
18	Transfer type changes from BUSY to NONSEQ during waited states for an undefined length burst	We have an undefined length burst. A sequential address A is driven onto the bus. Then a busy transfer is inserted to address B and is driven onto the bus.	3.6.1			The undefined length burst completes with HREADY high. The burst is terminated due to the NONSEQ transfer type.	Transfer type changes from BUSY to NONSEQ during waited states for an undefined length burst

		Wait states are added by keeping HREADY low. Then a non sequential address C is driven onto the bus. The transfer type changes from BUSY to NONSEQ. HTRANS is kept constant and slaves must keep HREADY low during this phase . Then HREADY is set high.				Then the transfer of address C is signalled completed by the slave. In the next cycle, the transfer to address B completes, and then in the next cycle the transfer to address C completes.	
19	Address change during wait state with IDLE transfer	A single burst is initiated to address A and is driven onto the bus. Then another address Y is initiated onto the bus. An IDLE transfer is inserted to this address The slave inserts a wait state by keeping HREADY low. Then another address Z is initiated onto the bus. An IDLE transfer is inserted to this address.	3.6.2			During the address phases of address A and address B the slave samples the addresses at the rising edge of the clock cycle. The slave will signal a completed transfer after the transfer to address A . The IDLE transfers are ignored by the slave between addresses A and B.	Address change during wait state with IDLE transfer

		Then, a NOSEQ transfer is inserted to another address B, and is driven onto the bus. The transfer type changes to NONSEQ. Until HREADY goes HIGH, no more address changes are permitted.				Then, the slave will signal a completer transfer after the transfer to address B.	
20	Address change during awaited transfer after an ERROR	Two sequential addresses A and B are driven onto the bus. The address phase of address A is one cycle whereas the address phase of address B is extended to two cycles Then an address C is inserted with IDE transfer and driven onto the bus. As a result, the transfer type is changed to IDLE.	3.6.2			The addresses are sampled at the rising edge of the clock cycle in their address phases. During the first cycle of the data phase of address A, the slave provides an OKAY response. During the first cycle of the data phase of address B, the slave provides an OKAY response. Since the address phase was extended therefor in the next cycle slave will generate an ERROR response. During this cycle, the transfer type	Address change during awaited transfer after an ERROR

						changed successfully. In the next cycle, the slave responds with an OKAY signal.	
21	Transfer type changes from IDLE to NONSEQ during waited states	Address A, B, C, and X are driven onto the bus. One IDLE transfer is inserted to address B and address C. The transfer type is changed to NONSEQ and initiates a transfer to address x. With HREADY low, the HTRANS is kept constant.	3.6.1	A		The slave will sample address A at the rising clock edge of the address phase. After successful transfer to address A the slave will ignore the IDLE transfers i.e., transfers associated with addresses B and C will be neglected. Then, address B will be sampled in its address phase. Transfer to address B will complete and slave will signal a complete transfer response.	Transfer type changes from IDLE to NONSEQ during waited states
22	Transfer type changes from BUSY to SEQ during waited states for a fixed-length burst	A sequential address A is driven onto the bus. Then a busy transfer is inserted and address B is driven on the bus. Wait states are added by keeping HREADY low.	3.6.1	A		Transfer to address A completes when HREADY is set high. In the next cycle, the transfer to address B completes, and then in the next cycle the transfer	Transfer type changes from BUSY to SEQ during waited states for a fixed-length burst

		A sequential address C is driven on the bus. The transfer type changes from BUSY to SEQ. HTRANS is kept constant and slaves must keep HREADY low during this phase. Then HREADY is set high.				to address C completes.	
23	Transfer type changes from BUSY to NONSEQ during waited states for an undefined length burst	We have an undefined length burst. A sequential address A is driven onto the bus. Then a busy transfer is inserted to address B and is driven onto the bus. Wait states are added by keeping HREADY low. Then a non-sequential address C is driven onto the bus. The transfer type changes from BUSY to NONSEQ. HTRANS is kept constant and slaves must keep HREADY low during this phase . Then HREADY is set high.	3.6.1			The undefined length burst completes with HREADY high. The burst is terminated due to the NONSEQ transfer type. Then the transfer of address C is signalled completed by the slave. In the next cycle, the transfer to address B completes, and then in the next cycle the transfer to address C completes.	Transfer type changes from BUSY to NONSEQ during waited states for an undefined length burst

24	Address change during wait state with IDLE transfer	A single burst is initiated to address A and is driven onto the bus. Then another address Y is initiated onto the bus. An IDLE transfer is inserted to this address The slave inserts a wait state by keeping HREADY low. Then another address Z is initiated onto the bus. An IDLE transfer is inserted to this address. Then, a NOSEQ transfer is inserted to another address B, and is driven onto the bus. The transfer type changes to NONSEQ. Until HREADY goes HIGH, no more address changes are permitted.	3.6.2			During the address phases of address A and address B the slave samples the addresses at the rising edge of the clock cycle. The slave will signal a completed transfer after the transfer to address A . The IDLE transfers are ignored by the slave between addresses A and B. Then, the slave will signal a completer transfer after the transfer to address B.	Address change during wait state with IDLE transfer
25	Address change during awaited transfer after an ERROR	Two sequential addresses A and B are driven onto the bus. The address phase of address A is one cycle whereas the address phase of	3.6.2			The addresses are sampled at the rising edge of the clock cycle in their address phases. During the first cycle of the data	Address change during awaited transfer after an ERROR

		address B is extended to two cycles Then an address C is inserted with IDE transfer and driven onto the bus. As a result, the transfer type is changed to IDLE.				phase of address A, the slave provides an OKAY response. During the first cycle of the data phase of address B, the slave provides an OKAY response. Since the address phase was extended therefor in the next cycle slave will generate an ERROR response. During this cycle, the transfer type changed successfully. In the next cycle, the slave responds with an OKAY signal.	
26	Slave response: Transfer done	The transfer is completed successfully.	5.1.1	A		Slave must give **HREADY** HIGH and **HRESP** OKAY	
27	Slave response: Transfer pending	Transfer is pending	5.1.2	A		Slave must give **HREADY** LOW and **HRESP** OKAY	
28	Slave response: transfer failed	The transfer is not completed successfully	5.1.3	A		**HRESP** must be HIGH. Two cycle response is required for an error condition.	

29	**HREADY**OUT	When HIGH the transfer has finish on the bus	2.3	A			
30	**HREADY**	If the transfer is extended then the master must hold the valid data until the transfer completes	6.1.1	A			