VERIFICATION PLAN

AHB-LITE INTERFACE

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AHB-Lite Protocol:

AHB-Lite implements the features required for high-performance, high clock frequency systems including:
• burst transfers
• Single-clock edge operation
• Non-tristate implementation
• Wide data bus configurations, 64, 128, 256, 512, and 1024 bits.
The most common AHB-Lite slaves are internal memory devices, external memory interfaces, and high bandwidth peripherals. Although low-bandwidth peripherals can be included as AHB-Lite slaves, they typically reside on the AMBA Advanced Peripheral Bus (APB) for system performance reasons. Bridging between this higher level of bus and APB is done using an AHB-Lite slave, known as an APB bridge. Figure 1-1 shows a single master AHB-Lite system design with one AHB-Lite master and three AHB-Lite slaves. The bus interconnect logic consists of one address decoder and a slave-to-master multiplexor. The decoder monitors the address from the master so that the appropriate slave is selected and the multiplexor routes the corresponding slave output data back to the master.

Working of Protocol:

Global Signals:

Name	Destination	Description
HCLK	Clock source	Clock source for all operations on the protocol. Input signals are sampled at rising edge and changes in output signals happen after the rising edge
HRESTn	Reset Controller	Asynchronous primary reset for all bus elements

Master Signals:

Name	Destination	Description
HADDR [31:0]	Slave and Decoder	Address bus of 32 bits
HBURST [2:0]	Slave	Indicates the type of burst signal including wrapping and incrementing bursts
HSIZE [2:0]	Slave	Indicates the size of transfer from 8 bits to 1024 bits

Slave Signals:

Name	Destination	Description
HRDATA [31:0]	Multiplexor	Read data bus to transfer the data from a Slave's location to the Master via multiplexor
HREADYOUT	Multiplexor	Indicates transfer has finished on the bus and is used to extend the data phase
HRESP	Multiplexor	Provides additional information that the transfer was successful or failed

Decoder Signals:

Name	Destination	Description
HSELx Note: x is a unique identifier for AHB lite slave	Slave	Indicates current transfer is for intended for selected slave

Multiplexor Signals:

Name	Destination	Description
HRDATA [31:0]	Master	Read data bus to rout to Master
HREADY	Master and Slave	Indicates completion of previous transfer
HRESP	Master	Transfer response

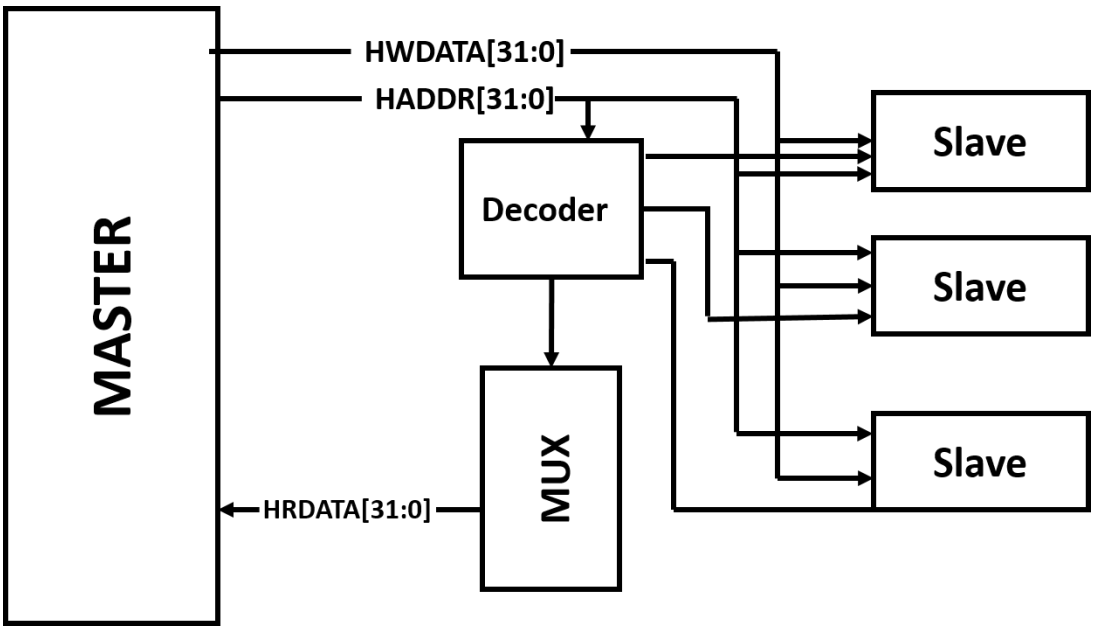

Fig 1.1

Working Protocol

The master starts a transfer by driving the address and control signals. These signals provide information about the address, direction, width of the transfer, and indicate if the transfer forms part of a burst. Transfers can be of different type's for instance single, incrementing bursts that do not wrap at address boundaries, wrapping bursts that wrap at particular address boundaries, etc. The write data bus moves data from the master to a slave, and the read data bus moves data from a slave to the master.

Every transfer consists of two phases:

1) Address phase: one address and control cycle

2) Data phase: one or more cycles for the data.

A slave cannot request that the address phase is extended and therefore all slaves must be capable of sampling the address during this time. However, a slave can request that the master extends the data phase by using HREADY. This signal when LOW, causes wait states to be inserted into the transfer and enables the slave to have extra time to provide or sample data. The slave uses a response signal to indicate the success or failure of a transfer.

VERIFICATION PLAN

No	Features	Test Description	Ref.	Type	Result	Comments
1	Write Transfer from Master to Slave	When HWRITE is high then the Master will broadcast the data on the HWDATA [31:0] bus for individual burst types i.e., HBURST [2:0] including incrementing and wrapping types.	3.1	TR		Successful write. HRESP should be low and HREADY should be high
2	Read Transfer from Slave to Master	When HWRITE is low then the slave must generate the data on the HRDATA [31:0] bus for individual burst types i.e., HBURST [2:0] including incrementing and wrapping type.	3.1	TR		Successful read. HRESP should be low and HREADY should be high
3	Continuous writing to the same slave at	When HWRITE is high, the Master will broadcast	3.1	TR		Successful write. HRESP should be low

	the same address location	the data packets on the HWDATA [31:0] bus.				and HREADY should be high for the successive data packets
4	Continuous reading from the same slave and same address location	When HWRITE is low, the slave must generate the data packets on the HRDATA [31:0] bus.	3.1	TR		Successful read. HRESP should be low and HREADY should be high for the successive data packets
5	Random Write transfers	When HWRITE is high, the Master will broadcast the data packets on the HWDATA [31:0] bus.	3.1	TR		Successful write. HRESP should be low and HREADY should be high for the successive data packets
6	Random Read Transfers	When HWRITE is low, the slave must generate the data packets on the HRDATA [31:0] bus.	3.1	TR		Successful read. HRESP should be low and HREADY should be high for the successive data packets
7	Write-Read Transfer	Write transfer followed by Read transfer at a particular address A.	3.1	TR		HRESP is low, HREADY is high and the address location must have the updated value
8	Read-Write Transfer	Read transfer followed by Write transfer at a particular address A.	3.1	TR		HRESP is low, HREADY is high and the slave must return the previous Data (A).

9	Global Signal: HCLK	A clock signal is generated in the top module	7.1.1	A		All input signals must be sampled at the rising edge of the clock and changes in the output signals must occur after the rising edge.
10	Global Signal: HRESTn	Since this is an active low signal. When asserted then it must reset all bus elements. Note: Slaves must ensure that HREADYOUT is high. HTRANS [1:0] must indicate IDLE.	7.1.2	TR		All previous binary information in the bust elements will be lost.
11	Master Signal: IDLE HTRANS [1:0] =b00	When IDLE transfer is inserted to an address.	3.2	TR		The HREADY must be low during the IDLE transfer. The transfer must be ignored by the slave. Slave must provide a OKAY response.
12	Transfer type changed during waited states: Scenario 1	Transfer type changes from IDLE to NONSEQ during waited states. The HTRANS signal must be kept constant after the transition until HREADY is high	3.6.1	A		Successfully transfer type changed. Slave must give OKAY response.
13	Transfer type changed during waited states: Scenario 2	Transfer type changes from BUSY to SEQ during waited states for fixed length bursts. The HTRANS signal must be kept constant after the transition until READY is high	3.6.1	A		Successfully transfer type changed. Slaves must give an OKAY response.
14	Transfer type changed during	Transfer type changes from BUSY to any other	3.6.1	A		Successfully transfer type

	waited states: Scenario 3	type during waited states for undefined length burst. The burst continues if an SEQ transfer is performed but terminates if an IDLE or NONSEQ transfer is performed.				changed. Slaves must give an OKAY response.
15	Transfer type changed during waited states: Scenario 4	Transfer type changed from IDLE to SEQ.	3.6.1	A		Slaves will give an ERROR.
16	Slave response: Transfer done	Transfer is successfully completed.	5.1.1	A		Slave must give **HREADY** HIGH and **HRESP** OKAY
17	Slave response: Transfer pending	Transfer is pending.	5.1.1	A		Slave must give **HREADY** LOW and **HRESP** OKAY
18	HREADY	If the transfer is extended it must saves it until it completes.	6.1.1	A		
19	HREADYOUT	When HIGH transfer must complete	2.3	A		When HREADYOUT is high, it means transfer is finished.