M T W T F S S
Page No.
Date
YOUVA

* History of computers :-

i) Zeroth Gen. of computers (1645 - 1945)

- First machine called computer, developed by Charles Babbage, named as Babbage engine.
- Was developed by using mechanical components like levers, gears and pulleys.
- 10X faster than humans computation.

ii) First Gen. (1945 - 1955)

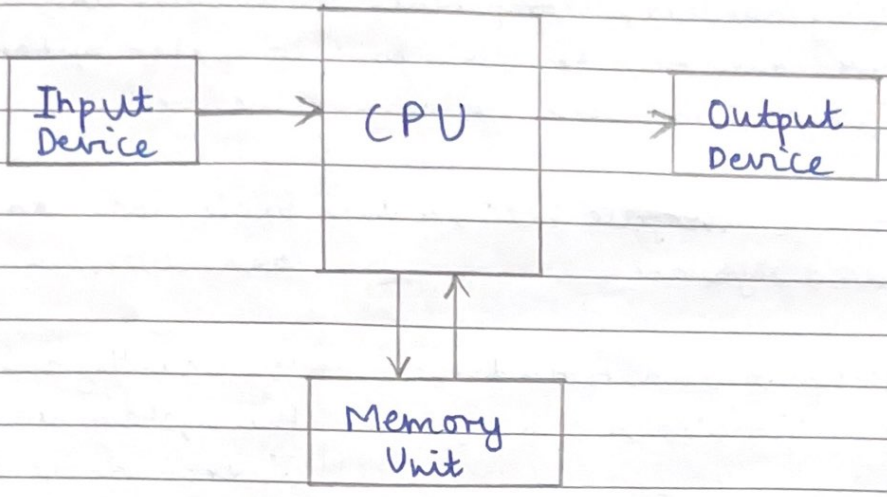
- ENIAC (Electronic Numerical Integrator & Computer), first computer developed by using vacuum tubes.
- It consists of :- 1) 15000 vacuum tubes
  2) 18000 Electromechanical Relays
- Weight - 30 tons ; Power cons. - 140 kwatts.
- It was programmable and programmed by using thumb wheel switches.

M T W T F S S
Page No.:
Date:
YOUVA

★	COMPUTER ARCHITECTURE	COMPUTER ORGANISATION
i)	Way hardware components are connected together to form a computer system.	Structure and behavior of a computer system as seen by the user.
ii)	Acts as interface bet" hardware and software.	Deals with components of a connection in a system.
iii)	Helps to understand the functionalities of a system.	How exactly all the units in the system are arranged & interconnected.
iv)	A programmer can view architecture in terms of instructions, addressing modes and registers.	Expresses the realisation of architecture.
v)	While designing a comp. system architecture is considered first.	Done on the basis of architecture.
vi)	Deals with high level design issues.	Deals with low level design issues.
vii)	Involves logic (Instruction sets, Addressing modes, Data types, cache optimization).	Involves physical components (Circuit design, Adders, Signals, Peripherals)

M T W T F S S
Page No.:
Date:
YOUVA

★ BASIC COMPUTER ORGANISATION :-



i) Input Device : Used to provide input (program/data) to computer. Ex: keyboard, mouse, etc.

ii) Output Device : Used to display or to send out output or result generated by CPU to user.
Ex: Monitor, printer, etc.

iii) CPU : 1.) Called heart of the computer.
2.) Responsible for carrying out the desired operation as per the instruction or input provided by Input Device.
3.) Result generated is either given to output device or stored in memory for future use.

iv) Memory Unit : 1.) Storage medium. Used to store programs & data, in immediate results or final results.
2.) The input provided by input device is first stored into memory by CPU.
3.) Whenever CPU needs instruction / data from memory, it will read from memory.
∴ Comm. bet^n CPU & memory → bidirectional.

- 2 types : 1.) Primary storage memory device
  2.) Secondary "

1.) Primary memory :

- Also known as Main memory or Internal memory, it stores programs and active data in semi-conductor memories.
- Volatile memory : RAM (Random Access Memory)
- Non-volatile memory : ROM (Read Only Memory), PROM (Programmable ROM).

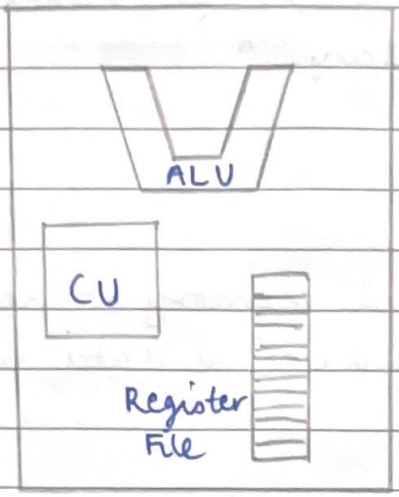
2.) Secondary memory :

- Also known as external memory / Auxillary memory.
- Non-volatile memory and is used for permanent storage of data and program.
- Ex : Hard disk, floppy disk, Magnetic tapes, etc.

★ INTERNAL STRUCTURE OF CPU :-

- It contains mainly : 1.) ALU (Arithmetic Logic Unit)
  2.) Control Unit
  3.) Register Files
  4.) CPU Interconnection.

*



1.) ALU (Arithmetic & Logic Unit) :-

- Responsible for performing all arithmetic operations like addition, subtraction, multiplication, divisions & logical operations like AND, OR, XOR, complement, rotate and shift.

- It consists of arithmetic circuits like half adder, full adder, half subtractor, full subtractor & multiplier. These circuits are developed using logic gates, & these logic gates are developed by using transistors.

2.) CU (Control Unit) :-

- Acts as the brain of the computer.

- Responsible for generating necessary control signals at appropriate time
  Ex: memory read, memory write, I/O read, I/O write, interrupt acknowledge.

- 2 approaches of CU design :- 1.) Hardwired CU
  2.) Microprogrammed CU

3.) Register File - A set of registers :-

- Set of internal registers, used for temporary storage of data.
- Act like the internal memory of the computer.
- The size, no. & use of these internal registors are different from processor to processor.
- Registers are classified acc. to : i.) Size
  ii) Use
  iii) Availability.

i) Size of the register : 8 bit, 16 bit, 32 bit, 64 bit.
They are always available in some standard size.

ii) Use of the register : ① GPR (General Purpose Register)
- Used for temporary storage of data

② SFR (Special Function Register)
- Used for a specific function.
- Ex → Program Counter (PC).

iii) Availability to user and programmer : ① Programmer Visible Register.
- If register is available to user while writing the program, it is called PVR.

② Programmer-Invisible Register.
- If register is not available to user while writing the program but is used internally by the processor itself, is called PIR.

★ COMPUTER FUNCTIONS :-

1.) Data processing : wide variety of data & processing.

2.) Data storage: Files of data are stored on the computer for subsequent retrieval and update.

3.) Data movement : computers serve as sources or destinations of data -
- When data is received from or delivered to a device that is directly connected to the computer, the process is known as input-output (I/O) and the device is referred to as a peripheral.
- When data is moved over longer dist., to or from a remote device, the process is known as data communications.

4.) Control: control unit manages the computer's resources and orchestrates the performance of its functional parts in response to instructions.

Date:

★ VON NEUMANN ARCHITECTURE :-

- Fixed Program computers – Their function is very specific and they couldn't be reprogrammed. Ex: Calculators

- Computers based on stored program concept - programs and data are stored in a seperate storage unit called memories and are treated the same - easier to reprogram.

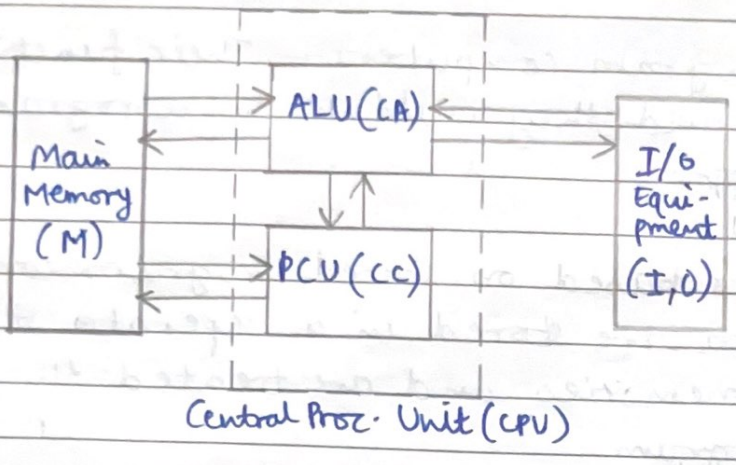
- Uses a single processor and one memory for both instructions and data.

- Executes programs following the fetch - decode - execute cycle.

- Princeton Institute for Advance Studies designed a new stored program computer, referred to as the IAS computer, in 1952.

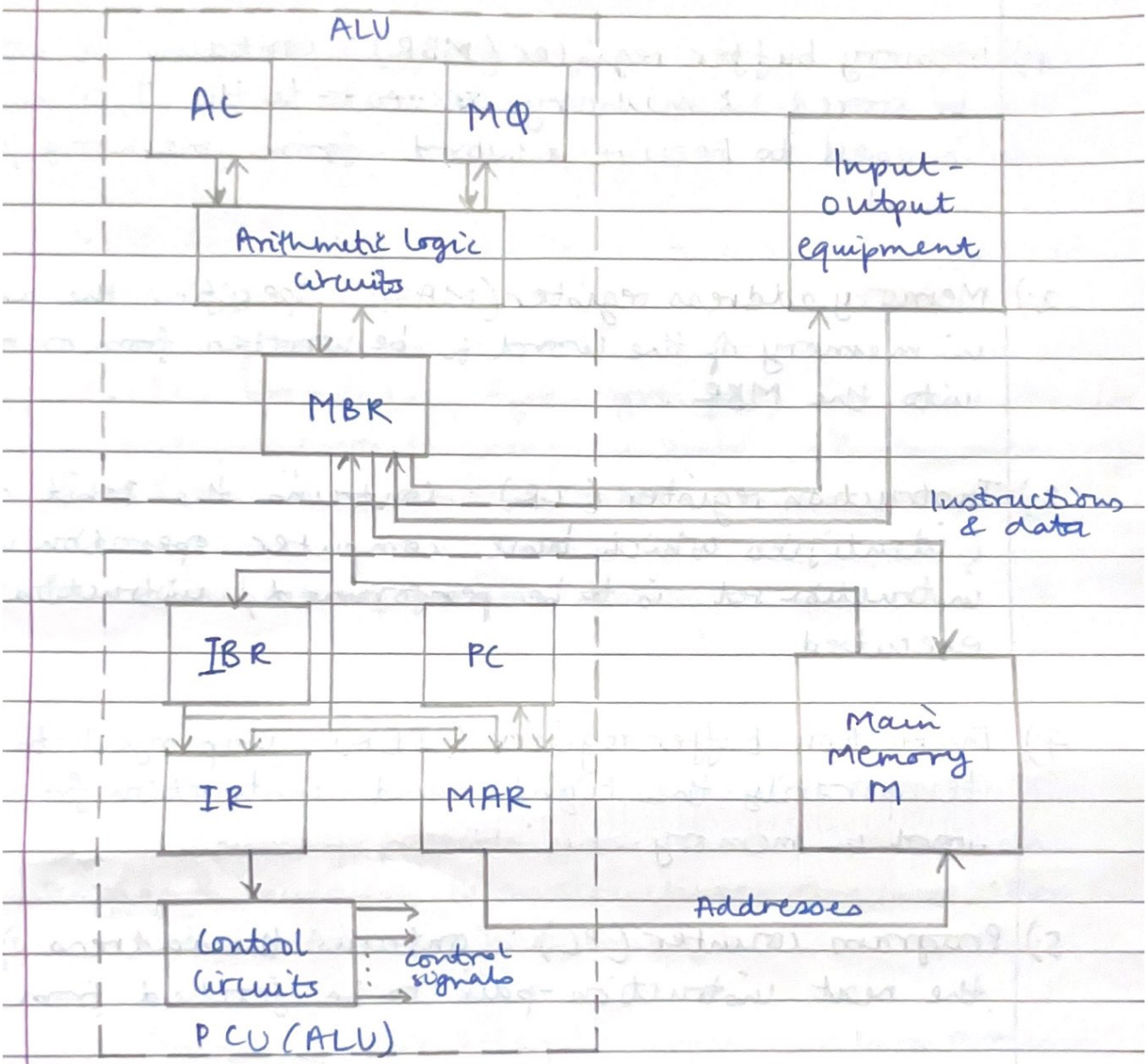
- It consists of: 1.) Main memory storing programs & data
  2.) ALU operating on binary data.
  3.) Control unit interpreting instructions from memory and executing.
  4.) Input & Output equipment operated by control unit.

★ VAN NEUMANN MACHINE STRUCTURE :-



- CA - Central arithmetic : part perform the elementary operations of arithmetic (Addition, subtraction, comparisions and logical operations, Bit shifting operations and Arithmetic operations).
- CC - Central control : proper sequencing of its operations / logical control of the device.
- M - Main memory : collection of storage cells together with associated circuits needed to transfer information in and out of the storage. The memory stores binary information in groups of bits called words.
- I,O - capable of delivering data (output) to and receiving data from a computer (input).

STRUCTURE OF IAS - DETAILED :-



M T W T F S S
Page No.:
Date:
YOUVA

✱ REGISTERS TYPES :-

1.) Memory buffer register (MBR) : contains a word to be stored in memory or sent to the I/O unit or is used to receive a word from memory / I/O unit.

2.) Memory address register (MAR) : Specifies the address in memory of the word to be written from or read into the MBR.

3.) Instruction register (IR) : Contains the 8-bit opcode (identifies which basic computer operation in the instruction set is to be performed) instruction being executed.

4) Instruction buffer register (IBR) : Employed to hold temporarily the right hand instructions from a word in memory.

5.) Program counter (PC) : Contains the address of the next instruction-pair to be fetched from memory.

6.) Accumulator (AC) & multiplier quotient (MQ) : employed to hold temporarily operands and results of ALU operations.

M T W T F S S
Page No.:
Date:
YOUVA

★ BUS :-

- Communication pathways, it is a group of wires running in parallel and carrying some useful information like address, data or control signals.
- Used to connect/interface two or more devices together in a computer.
- Usually broadcast, often grouped. Ex: A bus enables a comp. processor to communicate with the memory or video card to communicate with the memory.
- Power lines may not be shown.

★ Interconnections :-

- There are no of possible interconnection systems.
- Single & multiple BUS structures are most common
Ex: Control / Address / Data bus (PC).
Ex: Unibus (DEC-PDP)
(Digital Equipment Corp. - Programmed Data Processor)

★ Functions :-

1.) Data sharing : Series / Parallel, 8-bit, 16-bit, 32-bit or even 64-bit buses.

2.) Addressing : A bus has address lines which allow data to be sent to or from specific memory locations.

2.) Power : A bus supplies power to various peripherals connected to it.

4.) Timing : System clock - synchronize the peripherals attached to it with the rest of the system.

** TYPES OF BUS :-

1.) System bus : If the same bus is used to carry address, data and control signals, its a system bus.

- In computer, all memory chips and other peripheral devices are connected to CPU (microprocessor) by using system bus.

2.) Dedicated bus : If all lines of a bus are used to carry only one type of information, its a dedicated bus.

- Data Bus : All lines carry only data. Width is a key determinant of performance.

- Address Bus : Only address. Identifies the source or destination of data. Bus width determines maximum memory capacity of system.

  - 2 lines of addr. lines = memory capacity.

3.) Control Bus : carry only control signals, generated by CU.

- Has to control and timing of information.

- Memory read/write signal
- Interrupt signal
- Clock signals.

3.) Multiplexed Bus: Bus used to carry address as well as data, not at the same time.

- Initially if carrying address, after sometime (demultiplexing), the same lines will carry data
- Advantage - fewer lines.
- Disadvantage - more complex control
  - Ultimate performance.

☆ Single bus problems :-

- Propagation delays.
  - Long data paths means that coordination of bus use can adversely affect performance.
  - If aggregate data transfer approaches bus capacity.
- Most systems use multiple buses to overcome these problems.

★ BUS ARBITRATION :-

- In a computer system a single bus system (system bus) is used to connect CPU, CM, MM and all other devices together. Because of sharing of the bus at a time, only one device is allowed to communicate with the CPU.

- If multiple devices want to communicate with the CPU at a time then priority is to be decided so that the device with highest priority ~~with~~ will get bus service.

- Bus Arbitration is a selection mechanism that decides which device will get bus service in case simultaneous bus requests by different devices. It is of 2 types :-

1.) Centralised Arbitration : A single hardware device (bus controller / arbiter) is responsible for managing access to the bus.

2.) Distributed Arbitration : Each device may claim the bus. A 4bit identification no. is allocated to each device on the bus. The created ID will decide the device's priority.

Date:

★ PCI - Peripheral component interconnect :-

- Popular high-bandwidth, processor-independent bus that can function as a mezzanine or peripheral bus.

- Delivers better system performance for high speed I/O subsystems (ex: graphic display adapters). It is specifically designed to meet economically the I/O requirements of modern systems. It requires very few chips to implement and supports other buses attached to the PCI bus.

- Supports a variety of microprocessor-based configurations including both single and multiple-processor systems, provides a general-purpose set of functions. It makes use of synchronous timing and a centralized arbitration scheme.

- PCI bus connects the CPU and expansion boards. PCI devices like Modem, Network card, sound/video card, et

- Is a 32-bit or 64-bit bus. 49 mandatory signal lines divided into func. groups :-

1.) System lines
- Including clock & reset

2.) Address & Data pins
- 32 time mux lines for addr/data
- Interrupt & validate lines.

3.) Interface Control pins

4.) Arbitration pins
- Not shared
- Direct connection to PC bus arbiter

5.) Error lines.

• Optional signal lines :-

1.) Interrupt pins.
- Not shared.

2.) Cache support pins.
-

3.) 64-Bit Bus Extension
- Additional 32 lines
- Time multiplexed.
- 2 lines to enable devices to agree to use 64-bit transfer.

Page No.
Date: YOUVA

* SCSI - Small Computer System Interface :-

- Pronounced "scuzzy", its a fast bus that can connects various devices/peripherals to the comp. at same time like hard disks, scanners, printers, etc. unlike USB connected for small devices.

- Helps to put multiple items on one bus and works with most computer systems.

- Known for its high data transfer rates and versatility in supporting multiple devices on a sigle bus, it is essential in enterprise and high-performance computing environments.

* Disadvantages:-

1.) Limited BIOS (Basic Input/Output System) support as it has to be configured for each computer.

2.) No common SCSI software interface.

3.) All diff. types of SCSI have different speeds, bus widths, connectors which can be confusing.

* Advantages :-

1.) Set of standard electronic interfaces allow personal PCs to communicate with peri. hardware such as CDs, etc.

2.) Faster.

3.) SCSI standards are gen. backward compatible.
- A parallel interface standard used by Apple Macintosh, PCs & Unix systems for attaching peri. devices to a comp.

M T W T F S S

Page No.:

Date:

YOUVA

* Interconnection :-