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| **Course Name:** | **Digital Design Laboratory** | **Semester:** | **III** |
| **Date of Performance:** |  | **Batch No:** | **A4** |
| **Faculty Name:** |  | **Roll No:** | **16010122083** |
| **Faculty Sign & Date:** |  | **Grade/Marks:** | **\_\_\_/25** |

**Experiment No: 5**

**Title: Flip Flops**

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| **Aim and Objective of the Experiment:** |
| To Verify truth table of JK Flip flop using IC 7476 and study conversion of JK FF to D FF and T FF  **\_\_\_\_\_\_\_\_\_** |

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| **COs to be achieved:** |
| **CO3**: Design synchronous and asynchronous sequential circuits. |

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| **Tools used:** |
| Trainer kits |

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| **Theory:** |
| Flip-flop is the common name given to two-state devices which offer basic memory for sequential logic operations. Flip-flops are heavily used for digital data storage and transfer and are commonly used in banks called "registers" for the storage of binary numerical data.  **JK-flip flop:** has two inputs, traditionally labeled J and K. IC 7476 is a dual JK master slave flip flop with preset and clear inputs. If J and K are different then the output Q takes the value of J at the next clock edge. If J and K are both low then no change occurs. If J and K are both high at the clock edge, then the output will toggle from one state to the other. It can perform the functions of the set/reset flip-flop and has the advantage that there are no ambiguous states.  **D Flip Flop:** tracks the input, making transitions with match those of the input D. The D stands for "data"; this flip-flop stores the value that is on the data line. It can be thought of as a basic memory cell. D flip-flop can be made from J-K flip-flop by connecting both inputs through a not gate.  **T Flip Flop:** T or "toggle" flip-flop changes its output on each clock edge, giving an output which is half the frequency of the signal to the T input. It is useful for constructing binary counters, frequency dividers, and general binary addition devices. It can be made from a J-K flip-flop by tying both of its inputs high.  **Implementation Details:**  **Procedure**   1. Locate IC 7476 on Digital trainer kit 2. Apply various inputs to J & K pins by means of the output on logic output indicator. 3. Connect a pulsar switch to the clock input. 4. Connect the J&K as D and T flip flop as shown in diagrams and verify the respective truth tables.   **Logic Symbol:**  JK Flip-flop  Pin Diagram of IC 7476:    Truth Table of JK FF    **Conversion of FFs**   1. **JK to D FF**   **Conversion Diagram**    **Truth Table of D FF**             1. **JK to T FF**   **Conversion Diagram**    **Truth Table of T FF** |

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| **Implementation Details** |
| **Procedure:**   1. Locate the IC 7476 and place the IC on trainer kit. 2. Connect VCC and ground to respective pins of IC trainer kit. 3. Implement the circuit as shown in the circuit diagram. 4. Connect the inputs to the input switches provided in the trainer kit. 5. Connect the outputs to the switches of O/P LEDs 6. Apply various combinations of inputs according to the truth table and observe the condition of LEDs. 7. Note down the corresponding output readings for various combinations of inputs. |
| **Post Lab Subjective/Objective type Questions:** |
| 1. **How does a JK flip-flop differ from an SR flip-flop in its basic operation?**   **Input Signals:**  JK Flip-Flop: A JK flip-flop has two inputs: J (set) and K (reset). These inputs are used to control the flip-flop's behavior.  SR Flip-Flop: An SR flip-flop has two inputs: S (set) and R (reset). These inputs are used to set and reset the flip-flop.  **Clock Signal:**  Both types of flip-flops typically have a clock input (denoted as CLK or CK), which is used to synchronize their operations. The flip-flops' outputs change state in response to the clock signal.  **Operation:**  **JK Flip-Flop:**   * When J and K are both set to 0, the JK flip-flop maintains its current state. * When J is set to 1 and K is set to 0, the JK flip-flop will toggle its state (if it was in the '0' state, it will change to '1', and vice versa) on the rising edge of the clock signal. * When J is set to 0 and K is set to 1, the JK flip-flop will toggle its state on the falling edge of the clock signal. * When both J and K are set to 1, the JK flip-flop behaves like a toggle flip-flop. It switches states on each clock edge, effectively complementing its output.   **SR Flip-Flop:**   * When S is set to 1 and R is set to 0, the SR flip-flop is set (Q = 1, Q' = 0). * When S is set to 0 and R is set to 1, the SR flip-flop is reset (Q = 0, Q' = 1). * When both S and R are set to 0, the SR flip-flop maintains its current state. * When both S and R are set to 1, it enters an undefined or prohibited state, and its behavior depends on the specific implementation. In practice, it's avoided.  1. **What is the use of characteristic and excitation table?**  * Characteristic Table: Describes the relationship between inputs and outputs in combinational circuits. Useful for analyzing and optimizing combinational logic. * Excitation Table: Used in sequential circuits, especially flip-flops, to determine how to set inputs for desired state transitions in the next clock cycle. Essential for proper sequencing in sequential circuits.  1. **How many flip flops do you require storing the data 1101?**   We need 4 flip-flops to store data 1101. |

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| **Conclusion:** |
| Learnt the different kinds of flip-flops like JK, SR, D, T, and verified the truth tables for the same. |

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| **Signature of faculty in-charge with Date:** |