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| **Course Name:** | **Digital Design Laboratory** | **Semester:** | **III** |
| **Date of Performance:** | **\_\_\_ / \_\_\_ / \_\_\_\_\_\_** | **Batch No:** | **A4** |
| **Faculty Name:** | **Kiran Ajetrao** | **Roll No:** | **16010122083** |
| **Faculty Sign & Date:** |  | **Grade/Marks:** | **\_\_\_/25** |

**Experiment No: 8**

**Title: 1-bit adder on VHDL**

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| **Aim and Objective of the Experiment:** |
| To implement 1-bit adder on VHDL |

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| **COs to be achieved:** |
| **CO4**: Implement digital networks using VHDL |

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| **Tools used:** |
| Quartus, ModelSim |

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| **Theory:** |
| A 1-bit adder, a fundamental component of digital circuits, performs binary addition of two 1-bit numbers. It utilizes logic gates to generate the sum and carry-out outputs. A half-adder adds two bits without considering the carry from the previous stage, while a full-adder accounts for the carry input.  Using VHDL, a hardware description language, the 1-bit adder can be designed as a combinational circuit. VHDL facilitates the creation of a structural and behavioral description of the adder. In practice, this simple unit serves as a building block for constructing larger multi-bit adders, enabling arithmetic operations in microprocessors and digital systems. |

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| **Implementation Details** |
| **Code:**  use IEEE.std\_logic\_1164.all;  entity OneBitAdder is  port (num1, num2, carryin : in std\_logic;  sum, carryout : out std\_logic);  end OneBitAdder;  architecture behavior of OneBitAdder is  begin  sum <= num1 xor num2 xor carryin;  carryout <= (num1 and num2) or ((num1 xor num2) and carryin);  end behavior;  **Screenshots**      image |
| **Post Lab Subjective/Objective type Questions:** |
| 1. **How can 1-bit adder be used to implement a 4-bit adder?**   To create a 4-bit adder using 1-bit adders, use a cascade approach. Start with the least significant bits of two 4-bit numbers, feed them into the first 1-bit adder, and continue this process, carrying the output carry from each stage to the next. After four stages, you will obtain the 4-bit sum of the numbers. This method, known as a ripple-carry adder, is simple but relatively slow for large inputs due to the carry propagation delay. More advanced adder designs like carry-lookahead and carry-skip are used for faster results.   1. **What is VHDL used for?**   VHDL (VHSIC Hardware Description Language) is pivotal in digital and mixed-signal system design. It serves for specifying circuit behavior and structure, simulating designs, synthesizing them into physical hardware, and rigorous verification. Additionally, VHDL supports rapid prototyping, making it invaluable for educational and research purposes. Furthermore, it plays a crucial role in maintaining and upgrading legacy systems. Its adaptability and wide-ranging applications make it a cornerstone in the field of digital design and electronics, ensuring the efficient and accurate development of complex hardware systems. |

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| **Conclusion:** |
| We learned the software of the Quartas 2 and langauage of VHDL and implemented the 1-bit adder |

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| **Signature of faculty in-charge with Date:** |