Total No. of Questions—8] [Total No. of Printed Pages—3

Seat No.	

[5057]-2055

S.E. (Computer) (First Semester) EXAMINATION, 2016

COMPUTER ORGANIZATION AND ARCHITECTURE

(2015 Pattern)

Time : Two Hours **Maximum Marks : 50**

N.B. :— (*i*) Neat diagrams must be drawn wherever necessary.

(*ii*) Figures to the right indicate full marks.

(*iii*) Use of calculator is allowed.

(*iv*) Assume suitable data, if necessary.

1. (*a*) Show the general structure of IAS computer and explain in detail. [6]

(*b*) Explain following cache mapping techniques along with their merits and demerits : [6]

(*i*) Direct

(*ii*) Set associative.

Or

2. (*a*) Perform Division of following numbers using restoring Division Algorithm : [6]

Dividend = 1011

Divisor = 0011.

P.T.O.

(*b*) What is Cache coherence ? What are the solutions to cache coherence problem in single CPU system. [6]

3. (*a*) What are the evolutionary steps of I/O channel ? Explain types of I/O channel ? [6]

(*b*) Explain the following addressing modes with *one* example each :

(*i*) Immediate

(*ii*) Register Indirect

(*iii*) Direct.

Or

4. (*a*) Differentiate between programmed I/O and interrupt driven I/O. [6]

(*b*) What is displacement addressing ? Explain its types with calculation of effective address. [6]

5. (*a*) What are various hazards in instruction pipelining ? Explain with example. [7]

(*b*) What is register organization ? What are different types of registers ? Explain in detail. [6]

Or

6. (*a*) Explain the instruction cycle in detail. [6]

(*b*) List and explain various ways in which an instruction pipleine can deal with conditional branch instructions. [7]

7. (*a*) Compare horizontal and vertical microinstruction format. [6]

(*b*) Write a control sequence for the following instruction for single bus organization : SUB (R3), R1. [7]

Or

8. (*a*) Compare Hardwired control over micro-programmed control. [6]

(*b*) Explain in detail micro instruction sequencing organization. [7]

Marking Scheme

Q.1	a)	structure of IAS Computer = 2 Marks explanation of MAR, MBR,IBR, IR, PC,AC & MQ = 4 Marks	[6]
	b)	Direct Mapping = 3 Marks Set Associative = 3 Marks	[6]
		OR	
Q.2	a)	Result = 0011 Reminder = 0010 Each cycle = 1 ½ Mark 1 ½ * 4 = 6 Marks	[6]
	b)	Definition of cache Coherence = 2 Marks Solutions Write through= 2 Marks Write Block = 1 Marks Instruction cache =1 Mark	[6]
Q.3	a)	Evolutionary steps of I/ O Channel = 3 Marks Types of I/O Channel= 3 Marks • Selector channel = 1 ½ Mark • Multiplexer Channel = 1 ½ Mark	[6]
	b)	i) Immediate 2 Marks = Explanation = 1 + Example 1 (ii) Register Indirect 2 Marks = Explanation = 1 + Example 1 (iii) Direct Addressing 2 Marks = Explanation = 1 + Example 1	[6]
		OR	
Q.4	a)	Each point of Differentiation = 2 Marks 2*3=6 Marks	[6]
	b)	displacement addressing Definition =2 Marks 3 Types of displacement addressing = 4 Marks (Explanation with examples of each type) Relative Addressing = 2 Marks Base register addressing = 1 Marks Indexing =1 Marks	[6]
Q.5	a)	Data Hazards =3 Marks Resource Hazard =2 Marks Control Hazards =2 Marks	[7]
	b)	register organization = 1 Mark types of register = 5 Marks	[6]

P.T.O.

		• User visible = 3 marks • Control and status = 2 marks	
		OR	
Q.6	a)	State Diagram = 3 Marks Explanation = 3 Marks	[6]
	b)	Listing = 2 Marks Explanation of following point =1 Marks each • Multiple Streams • Prefetch branch target • Loop Buffer • Branch prediction • Delayed branch	[7]
Q.7	a)	Each point of comparison = 2 Marks 2*3=6 Marks	[6]
	b)	Instruction fetch = 2 Marks Operand Fetch= 2 Marks Execution of instruction steps= 3 Marks	[7]
		OR	
Q. 8	a)	Each point of comparison = 2 Marks 2*3=6 Marks.	[6]
	b)	micro instruction sequencing Diagram = 3 Marks Explanation = 4 Marks	[7]