

Scheme of Marking

Solution

Q1)	a)	Explain immediate and register addressing mode with an example. [02]
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Answer

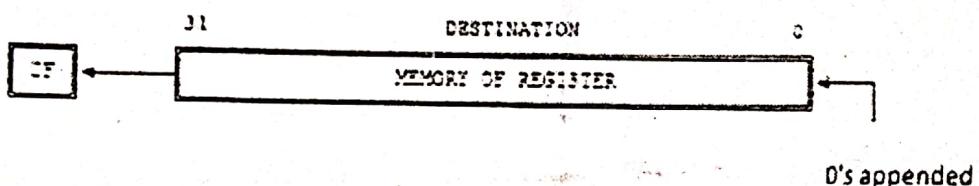
(i) **Immediate:**
Certain instructions use data from the instruction itself as one of the operands. Such an operand is called an immediate operand. The operand may be 32-, 16-, or 8-bits long.
For example: MOV EAX,00000005h

(ii) **Register:** Operands may be located in one of the 32-bit/ 16-bit/8-bit general registers.
Eg: MOV ECX,EDX

Q1)	b)	Explain with example SHL and ROL instructions. [04]
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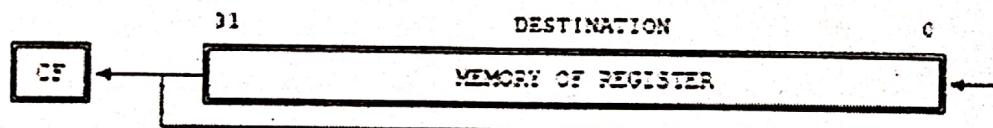
Answer

SHL:



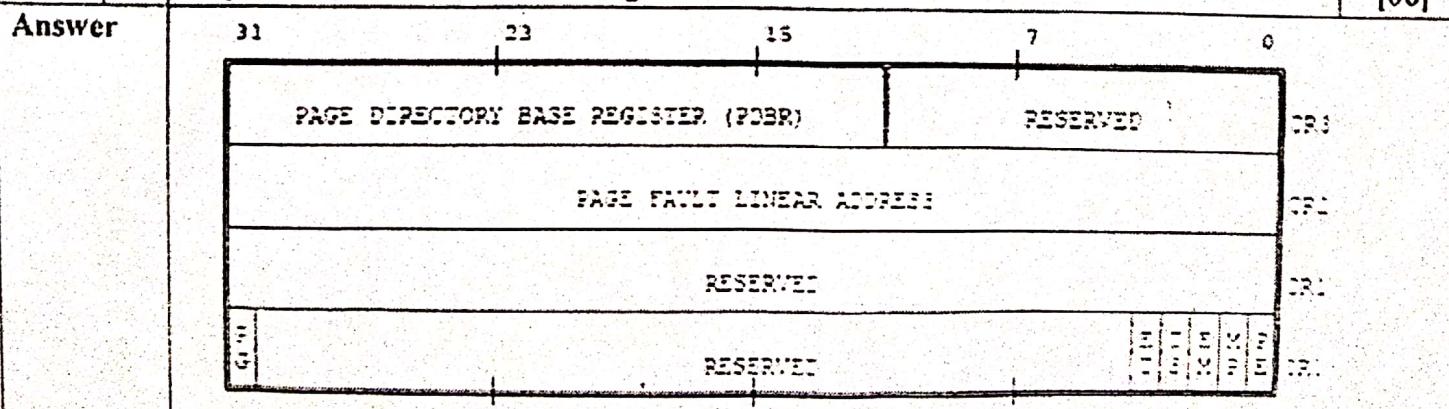
Shifts the bits of the operand upward. The high-order bit is shifted into the carry flag, and the low-order bit is set to 0.

ROL:



ROL (Rotate Left) rotates the byte, word, or doubleword destination operand left by one or by the number of bits specified in the count operand.

Q1)	c)	Explain in detail the control registers of 80386. [06]
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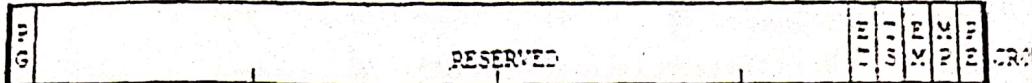


Explanation of each register 1 mark , diagram 2 marks

OR

Q2)	a)	Explain MSW.	[02]
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Answer Lower order 16-bits of CR0 register. The contents are:



PE: Protection Enable

MP: Math present

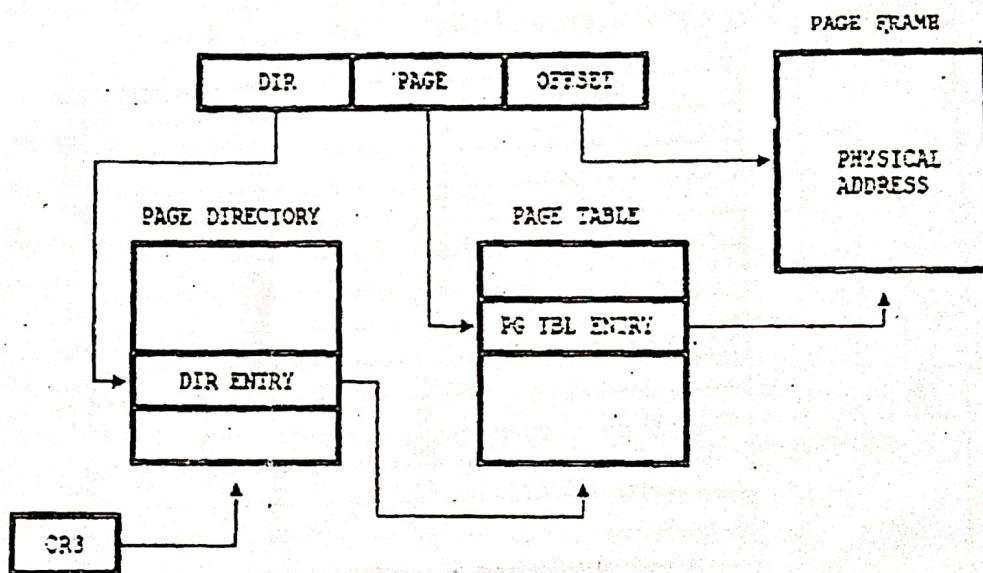
EM: Emulate co-processor

TS: Task switch

ET: Extension type

Q2)	b)	Explain paging mechanism.	[04]
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Answer



Explanation of conversion process is expected, diagram 2 marks, explanation: 2 marks

Q2)	c)	Explain the following instructions, mention flags affected: (i) LIDT (ii) CLD (iii) MOVS	[06]
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Answer

LIDT: Load IDTR, none of the flags affected

CLD: Clear direction flag, DF flag affected

MOVS: Move Data from String to String, no flags affected

Explanation of each instruction with syntax, flag and example 2 marks each

Q3)	a)	What is CPL and RPL?	[02]
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Answer

CPL: An internal processor register records the current privilege level (CPL). Normally the CPL is equal to the DPL of the segment that the processor is currently executing. CPL changes as control is transferred to segments with differing DPLs.

RPL: Selectors contain a field called the requestor's privilege level (RPL). The RPL is intended to represent the privilege level of the procedure that originates a selector.

Q3)	b)	Differentiate between memory mapped I/O and I/O mapped I/O.	[04]
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Answer	Minimum 4 points of comparison
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I/O Mapped I/O:
The I/O address space consists of 216 (64K) individually addressable 8-bit ports; any two consecutive 8-bit ports can be treated as a 16-bit port; and four consecutive 8-bit ports can be treated as a 32-bit port.

I/O Specific instructions can be used e.g. IN, OUT etc.

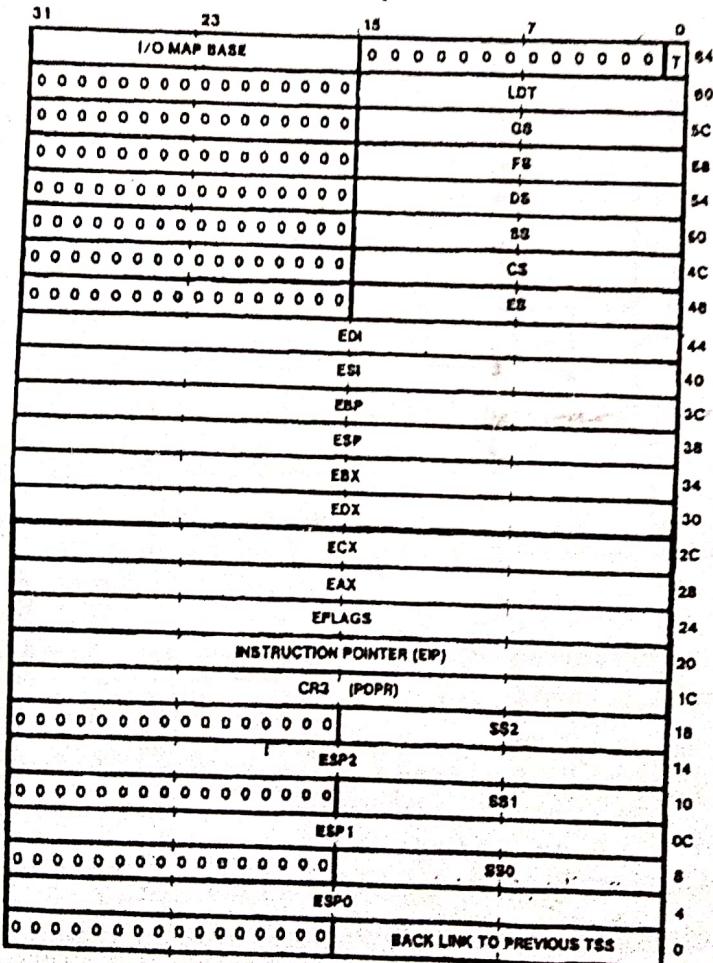
Memory Mapped I/O:

I/O devices also may be placed in the 80386 memory address space.

Any instruction that references memory may be used to access an I/O port located in the memory space. For example, the MOV instruction.

Q3)	c)	Draw and briefly explain Task State Segment.	[06]
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Answer	Diagram 4 marks and brief explanation 2marks
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OR

Q4)	a)	When does a page fault occur?	[02]
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Answer
Page fault occurs when paging is enabled ($PG=1$) and the processor detects one of the following conditions while translating a linear address to a physical address:

- The page-directory or page-table entry needed for the address translation has zero in its present bit.

- The current procedure does not have sufficient privilege to access the indicated page.

Q4)	b)	Explain any two I/O privilege instructions.	[04]
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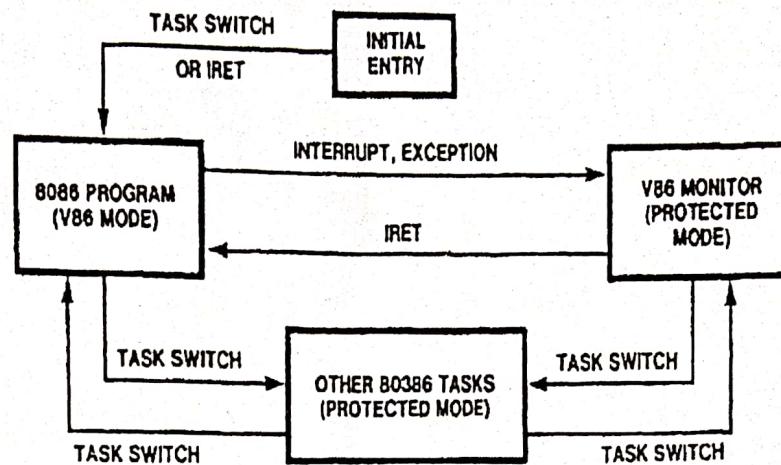
Answer		Explanation of any two I/O privilege instructions {2marks each} IN, INS, OUT, OUTS, CLI or STI																						
Q4)	c)	Explain what happens when an interrupt calls a procedure as an interrupt handler. [06]																						
Answer		Diagram 2 marks and explanation 4 marks																						
		<pre> graph LR IDT[IDT] -- "INTERRUPT ID" --> Trap[TRAP GATE OR INTERRUPT GATE] Trap --> LDT[GDT OR LDT] LDT --> SD[SEGMENT DESCRIPTOR] SD --> ES[EXECUTABLE SEGMENT] SD -- BASE --> EP[ENTRY POINT] SD -- OFFSET --> EP </pre>																						
1. Stack of interrupt procedure 2. Flags usage by interrupt procedure 3. Returning from an interrupt procedure 4. Protection in interrupt procedures																								
Q5)	a)	What are the contents of various registers of processor 80386 after reset? [03]																						
Answer The contents of EAX depend upon the result of the power-up self-test. DX holds component identifier and revision number. CR0 all bits are zero except ET (whose status depends on presence of 80387 NDP).																								
<table> <tbody> <tr> <td>EFLAGS</td> <td>= 0000002H</td> </tr> <tr> <td>IP</td> <td>= 000FFFOH</td> </tr> <tr> <td>CS selector</td> <td>= 000H</td> </tr> <tr> <td>DS selector</td> <td>= 0000H</td> </tr> <tr> <td>ES selector</td> <td>= 0000H</td> </tr> <tr> <td>SS selector</td> <td>= 0000H</td> </tr> <tr> <td>FS selector</td> <td>= 0000H</td> </tr> <tr> <td>GS selector</td> <td>= 0000H</td> </tr> <tr> <td>IDTR:</td> <td></td> </tr> <tr> <td>base</td> <td>= 0</td> </tr> <tr> <td>limit</td> <td>= 03FFH</td> </tr> </tbody> </table>		EFLAGS	= 0000002H	IP	= 000FFFOH	CS selector	= 000H	DS selector	= 0000H	ES selector	= 0000H	SS selector	= 0000H	FS selector	= 0000H	GS selector	= 0000H	IDTR:		base	= 0	limit	= 03FFH	
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Q5)	b)	How many debug registers are present in 80386? List and draw all of them. [04]																						
Answer How many? 1 mark List : 1 mark Diagram : 2 marks																								
Total 8 debug registers are present out of them 2 are reserved and six are used by 80386 to control debug feature.																								

1. Stack
2. Interrupt table
3. First instructions

Q6) c) With neat diagram explain "Entering and leaving V86 mode". [06]

Answer Diagram 2 marks explanation 4 marks

MODE TRANSITION DIAGRAM



Q7) a) Explain HOLD and HLDA signals of 80386DX. [03]

Answer 1 mark for on signal

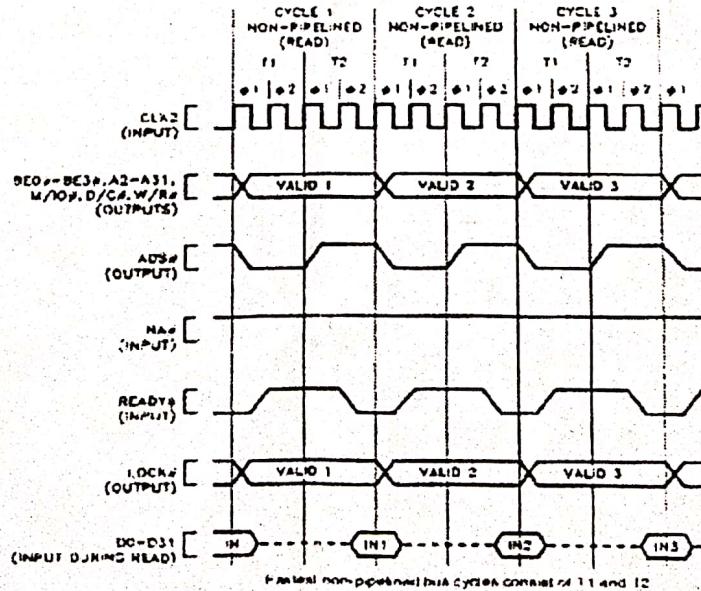
3 marks for both

Q7) b) List various bus states when address pipelining is used. [04]

Answer Ti, T1, T2, T2I, T1P, T2P, Th

Q7) c) Draw 'read cycle with non-pipelined address timing'. [06]

Answer



OR

Q8) a) Explain following signals

- i. NMI
- ii. INTR
- iii. RESET

Answer 1 mark each

Q8) b) Draw and explain 80387 register stack. [04]

Answer Diagram 3 marks, explanation 3 marks

80387 DATA REGISTERS

	79	78	64	63		0	1	0	TAG FIELD
R0	SIGN	EXPONENT	SIGNIFICAND						
R1									
R2									
R3									
R4									
R5									
R6									
R7									

Q8) c) Draw 'write cycle with pipelined address timing'. [06]

Answer Minimum Non-pipelined cycle + pipelined Write cycle (from this diagram) is expected

