Total No. of Questions—8] [Total No. of Printed Pages—2

Seat No.	

[5352]-564

S.E. (Computer) (I Sem.) EXAMINATION, 2018
COMPUTER ORGANIZATION AND ARCHITECTURE
(2015 PATTERN)

Time : Two Hours **Maximum Marks : 50**

N.B. :— (*i*) Neat diagrams must be drawn wherever necessary.
(*ii*) Figures to the right indicate full marks.
(*iii*) Use of calculator is allowed.
(*iv*) Assume suitable data, if necessary.

Q.1 a) List the elements of bus design. Explain any two elements of Bus Design [6]
b) Perform division of following 4 bit numbers using restoring Division algorithm [6]
Dividend=1010 Divisor=0011.

OR

Q.2 a) Represent 1259.125 in single precision and double precision formats. [6]
b) Explain associative mapping technique with neat diagram. [6]

Q.3 a) What are Data transfer modes of DMA? Explain any two in detail. [6]
b) Discuss following I/O mechanisms for transferring data with a neat flowchart. [6]
i. Programmed I/O
ii. Interrupt driven I/O

OR

Q.4 a) List the features of thunderbolt interface. Draw and explain thunderbolt configuration. [6]
b) Explain following addressing modes along with suitable example. [6]
I. Direct addressing
II. Indirect addressing
III. Displacement addressing mode

Q.5 a) Draw and Explain the functional block Diagram of 8086. [7]
b) Explain Instruction pipelining in detail. [6]

P.T.O.

OR

Q.6 a) Draw and Explain Instruction cycle state diagram. [7]
b) Compare Superscalar and super pipelined approaches in superscalar processor [6]

Q.7 a) Explain following instruction execution phases with suitable example [7]
i. Fetch the instruction
ii. Fetch the operand
iii. Execute the instruction
b) Draw and Explain Micro programmed Control Unit [6]

OR

Q. 8 a) Explain in detail following micro instruction sequencing techniques [6]
i. Single Address Fields
ii. Variable address Fields
b) Draw and Explain Single Bus organization of CPU [7]

Q.1	a)	Elements of Bus Design 2 Marks 1. Types of bus 2. Physical dedication 3. Method of Arbitration 4. Timing 5. Bus Width 6. Data Transfer Type Explanation of any two elements 2 * 2 = 4 Marks	[6]
	b)	Quotient= 0011 Reminder =0000 0001	[6]
		OR	
Q.2	a)	Single Precision(3Marks) = Exponent is:137 |127 Double Precision(3Marks) = Exponent is 1023	[6]
	b)	associative mapping technique Diagram =3 Marks Explanation = 3 Marks	[6]
Q.3	a)	Listing of Modes: 2 Marks Single Transfer Mode Block Transfer Mode Demand or Burst Transfer Mode Explanation of mode 2*2=4 Marks	[6]
	b)	Programmed I/O = 3 Marks Interrupt driven I/O = 3 Marks	[6]
		OR	
Q.4	a)	Any 4 Features = 2 Marks Diagram of configuration =2 Marks Explanation = 2 Marks	[6]
	b)	I. Direct addressing = 2Marks II. Indirect addressing = 2Marks III. Displacement addressing mode= 2Marks	[6]
Q.5	a)	Diagram = 3 Marks Explanation = 4 Marks	[7]
	b)	Explanation =6 Marks	[6]
		OR	
Q.6	a)	Diagram =3 Marks Explanation = 4 Marks	[7]
	b)	Each point of Differentiation = 2 Marks 2*3=6 Marks	[6]
Q.7	a)	Instruction fetch = 2 Marks Operand Fetch= 2 Marks	[7]

P.T.O.

Execution of instruction steps= 3 Marks

b) Diagram =3 Marks [6]
Explanation = 3 Marks

OR

Q. 8 a) Single Address Fields = 3 Marks [6]
Variable address Fields = 3 Marks

b) Diagram = 3 Marks [7]
Explanation = 4 Marks.