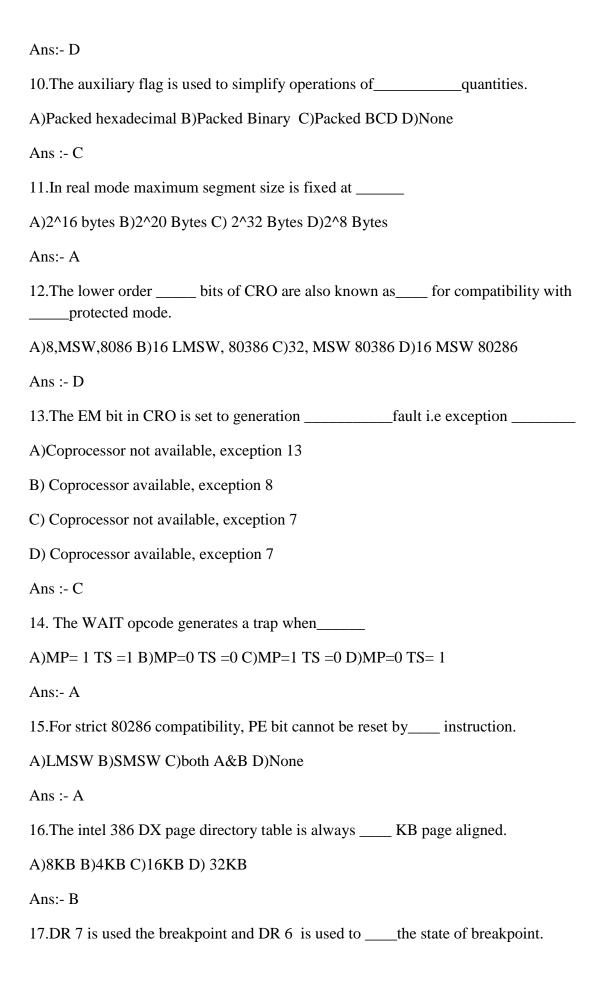
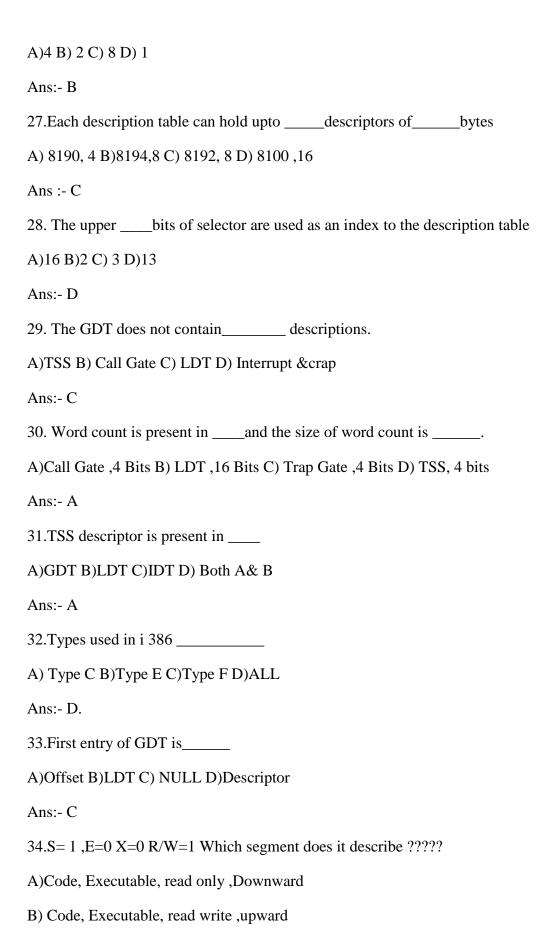
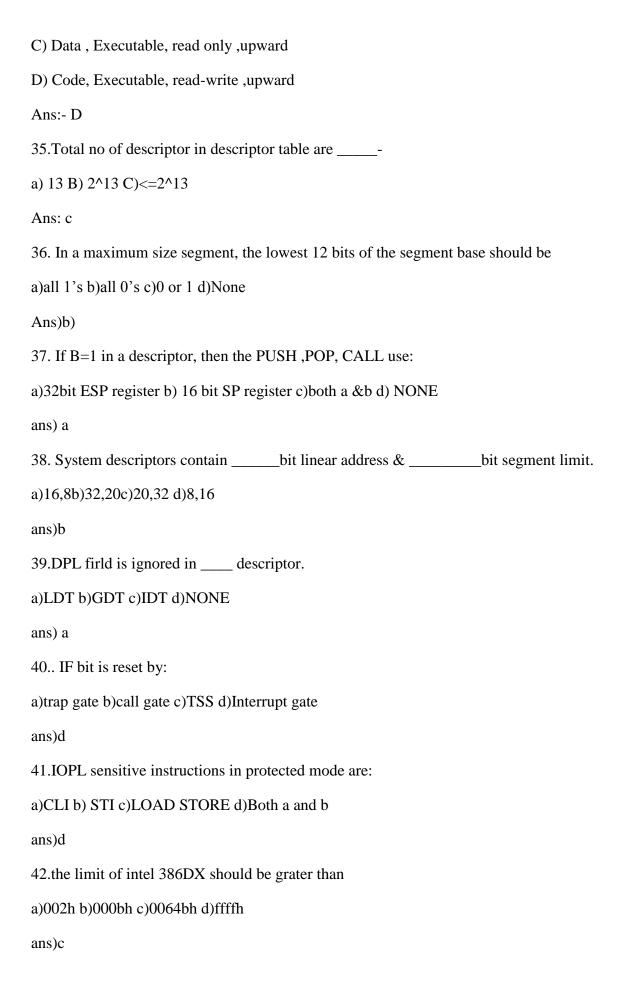
1. Barrel shifter is used to speed up which of the following operations?
A)Shift B)Rotate C)Multiply,Divide D)ALL
Ans :- D
2.Multiply and divide logic uses which algorithm?
A)1-Bit per cycle B)2 -Bit per cycle C)8 -Bit per cycle D) 32-Bit per cycle
Ans :- A
3.Each task on 80386DX can have a maximum of segments of up size.
A) 16380, 1GB B) 16381, 4GB C) 16381, 1MB D) 16830, 4KB
Ans :- B
4.8086 has bit address lines.
A) 32 B)20 C)16 D)8
Ans :- B
5.The VM bit can be set in mode byinstruction.
A)Real, INTO B) Protected, IRET C) Protected ,JMP D) None
Ans:- B
6.VM bit is unaffected byinstruction.
A)PUSHF B)POPA C)POPF D)IRET
Ans:- C
7. Which instruction can alter IOPL field when executed at CPL=0
A)IRET,POPF B)PUSHF,POPE C)IRET, PUSHF D)CALL,POPF
Ans:- A
8.Theflag when reset doesn't allow recognition of external interrupts signalled on pin
A)IF,INTR B)DF,INTR C)IF,NMI D)None
Ans:- A
9. When TF is exception 1 traps occur only as a functions of breakpoint address loaded into debug register.
A)Set, DRO B)Set DRO-DR 3 C)Reset DRO D)Reset DRO-DR3



A)Display, Set B)Display, Display C)Set, Display D)Both A&B							
Ans:- C							
18.TR 7 is the data register which contains the data of							
A) Translation look aside buffer list B)GDT C)IDT D)None							
Ans:- A							
19.80386 DV hascache.							
A)Level 1 B)Level 2 C) Level 3 D) Level 4							
Ans :- B							
20. TR 6 is							
A)Instruction test register B) Command test Register C) A&B D) None							
Ans:-							
21.Page fault line as address is present in							
A) CRO B) CRI C) CR2 D) CR 3							
Ans:- C							
22.Frequency range is							
A)5-10 MHZ B)6-10 MHZ C)1-2 MHZ D)None							
Ans:-B							
23.In 80386prefeched instruction are these							
A)4 B)8 C)6 D)2							
Ans :- C							
24.Prefeching depends on							
A)Barrel Shiftes B) Instruction C)Memory D)Buffer							
Ans :- D							
25.Fetching is done in							
A)EU B)CPU C)BIU D)ALL							
Ans :- C							
26.RPL is detected by : least bits of selector							





43. After enabling protected mode, theinstruction id used to load theCS register.
a)jmp b)call c)wait d)iret
ans) a
44. The page directory isbytes long and has max entries.
a)8k,512 b)8k,1024 c)4k,1024 d)4k,1024
Ans)c
45.U/S=1,R/W=1 which P.L. are permitted to access?
a)0,1 b)1,2 c)3 d)0,1,2,3
ans)d
46. The paging hardware allows _ bit linear address produced by virtual mode program to be divided uptopages.
a)32,256 b)16,512 c)32,512 d)20,256
ans) d)
47. Instructions applying to multitasking if attempted to use in real or virtual mode generates
a)exception 6 B)interrupt 13 c)interrupt 8 d)exception 4
ans) a
48. Virtual 8086 mode is entered by executing aninstruction at CPL=
a)IRET,2 B) INT,0 C)IRET,0 D)BOTH A & C
ans) c
49. TLB cache holds recententries of page tables.
a)16 b)8 c)20 d)32
ans) d
50. A confirming code segment takes the P.L of theinstruction due to which the segment was executed.
A)jmp,call b)call,wait c)je, call d)NONE
ANS)a
51provides the fundamental timing for 386DX
a)clk b)clk2 c)both a and b d)none

```
ans) b
52.BE0# applies to
a)D0-D7 b)D8 -D15 c) D16-D23 d_D24-D31
ans)a
53.BE1# applies to
a)D0-D7 b)D8 -D15 c) D16-D23 d_D24-D31
ans)b
54.BE0# applies to
a)D0-D7 b)D8 -D15 c) D16-D23 d_D24-D31
ans)c
55.BE0# applies to
a)D0-D7 b)D8 -D15 c) D16-D23 d_D24-D31
ans)d
56. When a I/O cycle is in progress, operand being transferred occupies only ____bits of data
bus.
a)2 b)8 c)16 d)32
ans)c
57.HALT has address ____
a)0 b)1 c)2 d)3
ans)c
58. SHUTDOWN has address ____
a)0 b)1 c)2 d)3
ans) a
59. the _____bus signals affect HALT and SHUTDOWN operations.
a)BE0#,BE1# b) BE0#,BE3# c) BE0#,BE2# d)ALL
ans)c
60. ____is ignored on the first bus state of all bus cycles.
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a)wait b)lock#c)ads#d)ready#
ans)d
61. Ready# must always meet setup and hold times ____&___for correct operation.
a)t19,t20 b)t17,18 c)t20,t21 d)t30,t31
ans)a
62.BS16# must always meet setup and hold times ____&___for correct operation.
a)t19,t20 b)t17,18 c)t20,t21 d)t30,t31
ans)b
63. HOLD must remain ___as long as any other device is a local bus muster.
a)asserted b)negated c)don't care d)NONE
ans)a
64. If both reset and hold are asserted then ___has higher priority
a)hold b)ready c) Equal priority to both d)none
ans)b
65.in hold acknowledge state, _____is the only signal being driven by 386DX while other
signals are in high impedance state.
a)hold b)ready c)wait d)hlda
ans)d
66. At the end of the second interrupt acknowledge bus cycle, INTR latches __bit interrupt
vector on ____to identify the source of interrupt.
a)8,D0-D7 b)16,D0 -D15 c) 32,D0 -D31 d) ALL
ans)a
67. During reset,, __has high impedance.
a)ads# b)be0# c)w/r# d)D0-D31
ans) d
68. The shortest time of bus activity is:
a)bus cycle b)bus state c)data cycle d)None
ans)b
```

69.T2 states are repeated indefinitely ifis not asserted.							
a)hlda b)ready# c)bs16# d)none							
ans)b							
70. When ready# is asserted, data bus pins should be atlogic state at end of each read cycle.							
a)0 b)0 or 1 c)1 d)don't care							
ans)b							
71. BS16# is asserted implies operation isbit							
a)16 b)32 c)20 d)both a and c							
ans)a							
72must be negated to allow recognition of assertedin final T2 state.							
a) na# ,bs16# b)bs16#,NA# c) NA# ,ready # d) ready#,NA#							
ans)a							
73. Once a pipelined addresss cycle is in progress, them pipelined timing is maintained in by signal							
a) asserting NA#							
b)negating NA#							
c) asserting READY#							
d)negating READY#							
ans)a							
74. The processor can go in T1P state only fromstate.							
a) T2P b)T1 c) T2 d) Ti							
ans) a							
75. Which of the following transisiton always takes place							
a)T1-> T2I b)T1P->T2 c) Ti->T1 d)T1->T2							
ans)d							
76.) Which instruction does not require LOCK prefix to lock it?							
a) call b)wait c)XCHG d) jmp							

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ans)c
77. Which instruction after execution transfers the control back to the program from where it
was called?
a)je b)jmp c) Call d) wait
ans)c)
78. Addressing mode used by wait instruction?
a)implied b) direct c) register d)all of the above
ans)a
79. INT 4 is implicitly also known as
a)iret b) into c) int d) int 13
ans)b
80. Which instruction is associated with the busy pin:
a)call b)jmp c) int d) wait
ans)d
81. DIV instruction takes how many operands.
a)1 b)2 c)3 d)all
ans) a
82. Sign flag sets. Which instruction from the following will cause a program control jump.?
a)js b)jns c)jz d)none
ans)a
83. AAA converts the result of the addition to
a)hexadecimal b) Decimal c) BCD d) Octal
ans) c
84. Test instruction
a)is same as cmp
b)does logical anding
c)tests the operands
```

d)does logical anding and does not not store the result.						
Ans)d						
85. Execution of an ALP takes place in the following way:						
a)linking, assembling,output						
b)linking,output						
c)assembling, linking,output						
d)none of the above						
ans)c						
86.To access control registersinstructions are defined.						
a)load b)store c)both a and b d)none						
ans)c						
87.All intel 386DX instructions operate onoperands						
a) 0 b)0,1 b)0,1,2 d)0,1,2,3						
ans)d						
88. A packed BCD stores each didgit in						
a)one bit b)a nibble c) one byte d)none						
ans)b						
89. Which of the following is protected mode specific instruction?						
a)mov b)add c)lmsw d)none						
ans)c						
90. HLT instruction usesaddressing mode.						
a)implied b)register c)direct d) ALL						
ans) a						
91. When STI is used						
a)IF=1 b)IF=0 c)IF=don't care d)None						
ans)a						
92is always undefined following shift operation.						

```
a)IF b)VM c)DF d)AF
ans)d
93.__flags will always be cleared by logical instructions.
a)OF, CF b) AF, CF c) VM, DF d) NT, CF
ans)a
94. The source cannot be a _____when usind LDS instruction
a)register b) operand c) memory location d) None
ans) a
95. ____ instruction is basically related to communication with I/O devices
a)add b) mov c)IN c)sub
ans)c
96.in POPA the first register to popped is:
a)ebp b)esi c)eax d)edx
ans)d
97.in PUSHA the first register to popped is:
a)ebp b)esi c)eax d)edx
ans)c
98. To load/store test register, _____addressing mode is used.
a) Register b) Memory c) direct d)implied
ans) a
99. The value in eax register for exit system call(32 bit) is:
a)0 b)1 c) 2 d)4
ans)b
100. The value in eax register for write system call(32 bit) is:
a)0 b)1 c) 2 d)4
ans)d
```