MP Unit-4 Input-Output, Exceptions and Interrupts MCQ's PART-B (1 Marks Questions)

Question- This type of interrupts cannot be avoided by processor.
A) Non Maskable
B) Maskable
C) Exceptions
D) All the above

Answer- A

Question- Interrupts are the _____events
A) External
B) Internal
C) Both A and B
D) None of the above

Answer- C

Question- In 80386, we can give interrupt to the machine by giving signals on
A) INTR
B) NMI
C) INTA
D) Both A and B

Answer- D

Question- Which interrupts used in critical condition?
A) INTR
B) Single step
C) NMI
D) All the above

Answer- C

Question- The interrupt can be disabled by using instruction_____
A) CLD

B) STI
C) CLI
D) STI

Answer- C

Question- Interrupts can be of____
A) Hardware
B) Software
C) Both A and B
D) None of the above

Answer- C

Question- Which is the following interrupt having lowest priority?
A) NMI
B) INTR
C) Faults
D) Single step

Answer- D

Question- Which is the interrupt having highest priority?
A) INTO
B) NMI
C) Single Step
D) INTA

Answer- A

Question- This _____masks NMI interrupt
A) IF
B) INTR
C) NMI
D) None of the above

Answer- C

Question- If IF=0, then it will masks
A) INTR interrupt
B) NMI interrupt
C) RF interrupt
D) None of the above

Answer- A

Question- STI and CLI instructions will be executed only when
A) CPL = IOPL
B) CPL >= IOPL
C) CPL <IOPL
D) Both A and C

Answer- D

Question- This____will masks debug faults in 80386
A) INTA
B) TF
C) RF
D) NMI

Answer- C

Question- 80386 support ___¬¬___number of interrupts.
A) 0
B) 1
C) 256
D) 255

Answer- C

Question- Exceptions are generated by
A) Internal events
B) External events
C) Both A and B
D) Hardware failures

Answer- A

Question- These exceptions are detected and serviced before the executions of Instructions
A) Traps
B) Faults
C) Aborts
D) All the above

Answer- B

Question- INT 2 interrupts belong to the_____
A) Faults
B) Traps

C) Non maskable interrupts
D) None of the above

Answer- B

Question- INT 8 belongs to the___
A) Traps
B) Aborts
C) Faults
D) None of the above

Answer- B

Question- The event such as illegal values comes under the category of _____
A) Interrupt
B) Trap
C) Debug faults
D) aborts

Answer- D

Question- This event related to exception of type fault.
A) Hardware error
B) Segment overruns
C) Both A and B
D) None of the above

Answer- B

Question- Which exception generates page fault exception?
A) Exception 9
B) Exception 11
C) Exception 14
D) Exception 15

Answer- C

Question- Non maskable interrupts assigned at vector number
A) 1
B) 2
C) 3
D) 5

Answer- B

Question- This instruction needs to be executed to find old state of machine
A) RET
B) IRET
C) INT
D) All the above

Answer- B

Question- IDT contain ____number of gate descriptors.
A) 1024
B) 512
C) 256
D) 255

Answer- C

Question- For storing the information about segments how many bytes are needed in Descriptor table?
A) 6
B) 7
C) 8
D) None of the above

Answer- C

Question- The size of GDT table is____
A) 1 GB
B) 1024 KB
C) 64 KB
D) None of the above

Answer- C

Question- One GDT can contain many
A) GDT
B) IDT
C) GATE
D) None of the above

Answer- D

Question- The descriptor which is not used in IDT is
A) Trap gate descriptor
B) Interrupt gate descriptor
C) Task gate descriptor
D) None of the above

Answer- D

Question- Trap gate descriptor defined in_____
A) LDT
B) IDT
C) TASK
D) GDT

Answer- B

Question- The first 16 bits from LSB in trap gate defines
A) Base address
B) Limit
C) Segment selector
D) None of the above

Answer- D

Question- Exception 11 or 14 generated, when
A) P bit marked present
B) P bit not marked present
C) P bit marked reserved
D) None of the above

Answer- B

Question- ____gate contain a selector to a TSS of new task and access right byte
A) Trap
B) Task
C) IDT
D) None of the above

Answer- B

Question- LIDT loads IDT register with the
A) Physical address of memory operand and offset
B) Logical address of an operand
C) Linear address and limit
D) None of the above

Answer- C

Question- The processor sets the ____if the index portion of the error code refers to a gate descriptor in the lOT.

A) P bit
B) I-bit
C) X bit
D) None of the above

Answer- B

Question- Interrupt 1 not refers to
A) General detect fault.
B) Single-step trap
C) Task-switch breakpoint trap.
D) None of the above

Answer- D

Question- Bounds Check fault when occurs generates_____
A) Exception 4
B) Exception 5
C) Exception 21
D) Exception 6

Answer- B

Question- Interrupt 7 generated means error is
A) Invalid Opcode
B) Double Fault
C) Coprocessor Not Available
D) None of these

Answer- C

Question- Coprocessor Not Available exception generates when
A) The processor encounters an ESC (escape) instruction, and the EM (emulate) bit of CRO (control register zero) is set.
B) The processor encounters either the WAIT instruction or an ESC instruction and both the MP (monitor coprocessor) and TS (task switched) bits of CRO are set.
C) Both A and B
D) None of these

Answer- C

Question- The error code is always___, when processor pushes error code onto stack Of double fault handler.
A) 0
B) 1
C) Undefined

D) None of these

Answer- A

Question- If any other exception occurs while attempting to invoke the double-fault handler___
A) The processor restarted
B) The processor shuts down.
C) Processor restarts execution of instruction
D) None of these

Answer- B

Question- Which is not in the category of benign double fault exception?
A) 0
B) 1
C) 2
D) 6

Answer- A

Question- Contributory double fault exception when occurs generates exception
A) 1
B) 14
C) 6
D) None of these

Answer- D

Question- When Contributory double fault exception 12 generates means the error is,
A) Invalid TSS
B) Stack exception
C) Page fault
D) None of these

Answer- B

Question- When Contributory double fault exception 14 generates means the error is,
A) Invalid TSS
B) Stack exception
C) Page fault
D) None of these

Answer- C

Question- Interrupt ___occurs if during a task switch the new TSS is invalid
A) 7
B) 8
C) 10
D) 14

Answer- C

Question- This error code SS id + EXT indicates condition_____
A) The limit in the TSS descriptor is less than 103
B) Stack segment selector is outside table limit
C) Invalid LDT selector or LDT not present
D) All the above

Answer- B

Question- Exception ____occurs when the processor detects that the present bit of a descriptor is
zero.
A) 10
B) 11
C) 12
D) 13

Answer- B

Question- Interrupt 11, generated when
A) Segment not present
B) Invalid segment
C) Both A and B
D) None of these

Answer- A

Question- The processor generates exception 11, because processor
A) Attempting to load the CS
B) Attempting to load the DS
C) Attempting to load the ES
D) All of these

Answer- D

Question- Attempting to load the LDT register with an LLDT instruction; causes exception_____

A) Segment not present
B) Invalid TSS
C) Invalid LDT
D) None of these

Answer- B

Question- I-bit is set if
A) if the error code refers to an IDT entry
B) if the error code refers to an IDTR
C) if the error code refers to an GDT entry
D) None of these

Answer- A

Question- Which exception generated by the processor to implement virtual memory at the segment level
A) Segment invalid
B) Segment not defined
C) Segment not present
D) Both B or C

Answer- D

Question- A stack fault occurs; by using the instructions
A) ADD
B) LEAVE
C) INC
D) None of the above

Answer- B

Question- A stack fault occurs due to the instruction
A) PUSH
B) POP
C) Enter
D) All of the above

Answer- D

Question- MOV AX, [BP+6]). ENTER causes this stack fault due to
A) Stack is empty
B) Stack in small
C) Memory is not initialized
D) None of these

Answer- B

Question- This instruction is not going to cause stack fault
A) LSS
B) MOV
C) POP
D) None of the above

Answer- D

Question- Which is not the cause of exception 13?
A) Exceeding segment limit when using CS, DS, ES, FS, or GS
B) Exceeding segment limit when referencing a descriptor table
C) Transferring control to a segment that is not executable
D) None of these

Answer- D

Question- Switching to a busy task, generates
A) General Protection Exception
B) Stack Exception
C) Segment Not Present
D) None of these

Answer- A

Question- Loading eRO with PG= 1 and PE=O, generates exception__
A) 10
B) 11
C) 12
D) 13

Answer- D

Question- Writing into a read-only data segment or into a code segment; generates exception
A) General Protection Exception
B) Stack Exception
C) Segment Not Present
D) None of these

Answer- A

Question- Page fault refers to exception

A) 12
B) 13
C) 14
D) 15

Answer- C

Question- Page fault exception occurs when
A) PG=1
B) PG=0
C) Both A and B
D) None of these

Answer- A

Question- The U/S=0 field in Page-Fault Error Code Format indicates
A) The access causing the fault originated when the processor is in user mode
B) The access causing the fault originated when the processor is in supervisor mode
C) Reserved bit
D) All of the above

Answer- B

Question- The first bit from LSB in Page-Fault Error Code Format indicates
A) U/S
B) W/R
C) P
D) R

Answer- C

Question- A page fault can result from accessing any of these segments_____
A) TSS
B) GDT
C) LDT
D) All of these

Answer- D

Question- The processor stores in____ the linear address used in the access that caused page fault exception
A) CR0
B) CR1
C) CR2
D) CR3

Answer- C

Question- Interrupt 16 is
A) Device not available
B) Device is missing
C) Coprocessor Error
D) All of these

Answer- D

Question- The processor generates coprocessor error by receiving signal on____
A) ERROR
B) ERROR#
C) NMI
D) INTR

Answer- B

Question- Interrupt type 15 is_____
A) Page fault
B) Reserved
C) Floating point check
D) None of these

Answer- B

Question- The ERROR# pin on 80387 causes which fault___
A) Data point error
B) Floating point error
C) Device not available
D) None of these

Answer- B

Question- The ___bit must be set in order to enable alignment checking
A) EM
B) AM
C) AC
D) None of the above

Answer- B

Question- If ____flag set at CPL___, then alignment check exception generated
A) AC and 3

B) AM and 0
C) AF and 3
D) None of the above

Answer- A

Question- The instruction_____used to indicate status of machine check.
A) CPUID
B) GPUID
C) CPUI
D) None of these

Answer- A

Question- The interrupt for which the processor has highest priority among all the external interrupts is
A) Mouse interrupt
B) keyboard interrupt
C) NMI
D) INT

Answer- C

Question- In case of string instructions, the NMI interrupt will be served only after
A) initialisation of string
B) the occurrence of the interrupt
C) complete string is manipulated
D) execution of some part of the string

Answer- C

Question- The NMI pin should remain high for atleast
A) 4 clock cycles
B) 2 clock cycles
C) 1 clock cycles
D) None of these

Answer- B

Question- The INTR signal can be masked by resetting the
A) TRAP flag
B) INTERRUPT flag
C) MASK flag
D) DIRECTION flag

Answer- B

Question- For the INTR signal, to be responded to in the next instruction cycle, it must go …….. in the last clock cycle of the current instruction
A) high
B) Low
C) High or low
D) Unchanged

Answer- A

Question- Once the processor responds to an INTR signal, the IF is automatically
A) set
B) reset
C) High
D) None of above

Answer- B

Question- Once the CPL is selected, it can be changed by
A) HOLD
B) transferring control using system descriptors
C) transferring control using gate descriptors
D) transferring control using interrupt descriptors

Answer- C

Question- The data segments defined in GDT (global descriptor table) and the LDT (local descriptor table) can be accessed by a task with
A) privilege level 0
B) privilege level 1
C) privilege level 2
D) privilege level 3

Answer- A

Question- The task requesting an access to a descriptor is allowed to access after checking the
A) type of descriptor
B) privilege level
C) type of descriptor and privilege level

Answer- C

Question- A CALL instruction can reference only a code segment descriptor with
A) DPL less privilege than CPL
B) DPL equal privilege to CPL

C) DPL greater privilege than CPL
D) all of the mentioned

Answer- B

Question- The RPL of a selector that referred to the code descriptor must have
A) less privilege than CPL
B) greater privilege than CPL
C) equal privilege than CPL
D) any privilege regarding CPL

Answer- C

Question- The instruction that refers to only code segment descriptors with DPL equal to or less than the task CPL is
A) CALL
B) RET
C) ESC
D) RET & IRET

Answer- D

Question- An exception is generated when
A) privilege test is negative
B) an improper segment is referenced
C) referenced segment is not present in physical memory
D) All the above

Answer- D

Question- Which of the following is a system segment register?
A) GDTR
B) LDTR
C) IDTR
D) None of above

Answer- B

Question- The registers that are together, known as system address registers are
A) GDTR and IDTR
B) IDTR and LDTR
C) TR and GDTR
D) LDTR and TSR

Answer- A

Question- The descriptor table that the 80386 supports is
A) GDT (Global descriptor table)
B) IDT (Interrupt descriptor table)
C) LDT (Local descriptor table)
D) All the above
Answer- D

Question- The RF is not automatically reset after the execution of
A) IRET
B) POPA
C) IRET and POPF
D) IRET and PUSHF

Answer- C

Question- During the instruction cycle of 80386, any debug fault can be ignored is
A) VM flag is set
B) VM flag is cleared
C) RF is cleared
D) RF is set

Question- In protected mode of 80386, the VM flag is set by using
A) IRET instruction
B) task switch operation
C) IRET instruction or task switch operation
D) none of the mentioned

Answer- D

Question- The gate descriptor contains the information of
A) destination of control transfer
B) stack manipulations
C) privilege level
D) All the mentioned

Answer- D

Question- The gate that is used to specify corresponding service routine is
A) call gate and trap gate
B) task gate and interrupt gate
C) interrupt gate and trap gate
D) task gate and trap gate

Answer- C

Question- Which pin is used to differentiate between memory and I/O operations

A) M/IO#
B) IN
C) OUT
D) None of the above

Answer- A

Question- I/O instructions do not go through the segmentation and paging unit

A) Yes
B) No
C) Both A & B
D) None of these

Answer- A

Question- IN and OUT instruction drives the 80386 M/IO# pin --------

A) high
B) low
C) Both A & B
D) None of the above

Answer- B

Question- From I/O port address which pins are used to select a byte, word, double word of I/O data

A) BL3# - BL0#
B) A2 and A1
C) A1 and A0
D) None of the above

Answer- A

Question- If memory mapped I/O is udes then number of I/O locations can be upto ----------

A) 4GB
B) 2GB
C) 1GB
D) 8GB

Answer- A

Question- The I/O system is divided into how many banks?

A) 1

B) 2
C) 3
D) 4

Answer- D

Question- Which instruction is used to copy data from port
A) IN
B) INS
C) OUTS
D) OUT

Answer- A

Question- Which instruction is used to input string from port
A) IN
B) INS
C) OUTS
D) OUT

Answer- B

Question- Which instruction is used to output string to port
A) IN
B) INS
C) OUTS
D) OUT

Answer- C

Question- Which instruction is used to output to port
A) IN
B) INS
C) OUTS
D) OUT

Answer- D

Question- Which instruction is used to take input string from port as Byte?
A) INSB
B) INSW
C) INSD
D) None of these

Answer- A

Question- Which instruction is used to take input string from port as Word?
A) INSB
B) INSW
C) INSD
D) None of these

Answer- B

Question- Which instruction is used to take input string from port as Double Word?
A) INSB
B) INSW
C) INSD
D) None of these

Answer- C

Question- Which instruction is used to output string to port as Byte?
A) OUTSB
B) OUTSW
C) OUTSD
D) None of these

Answer- A

Question- Which instruction is used to output string to port as Word?
A) OUTSB
B) OUTSW
C) OUTSD
D) None of these

Answer- B

Question- Which instruction is used to output string to port as Double word?
A) OUTSB
B) OUTSW
C) OUTSD
D) None of these

Answer- C

Question- Which instruction is used to output string to port as Double word?
A) OUTSB
B) OUTSW
C) OUTSD
D) None of these

Answer- C

Question- I/O protection can be achieved using ----------
A) I/O privilege level
B) I/O permission bitmap
C) Both of these
D) None of these

Answer- C

Question- Which is not I/O sensitive instruction?
A) IN
B) INS
C) IOPL
D) None of the above

Answer- C

Question- Which is not I/O sensitive instruction?
A) OUT
B) OUTS
C) IOPL
D) None of the above

Answer- C

Question- Which is/are I/O sensitive instruction?
A) CLI
B) STI
C) All of the above
D) None of the above

Answer- C

Question- What is the condition for I/O instruction?
A) CPL <= IOPL
B) CPL < IOPL

C) CPL > IOPL
D) CPL = IOPL

Answer- A

Question- If CPL > IOPL, then what will happen?
A) instruction will be executed
B) General protection violation exception
C) None of these
D) Both A and B

Answer- B

Question- Which exception is generated if Code is not at PL0
A) Exception 13
B) Exception 11
C) Exception 12
D) Exception 14

Answer- A

Question- Where I/O persmission bitmap is Present?
A) TSS top portion
B) TSS bottom portion
C) IOPL
D) None of these

Answer- A

Question- The size of I/O permission bitmap is
A) Fixed
B) Variable
C) Both
D) None of the above

Answer- B

Question- What is the address for bank 0 in I/O organization?
A) 0000 to FFFC
B) 0000 to F000
C) 0000 to 9999
D) None of the above

Answer- A

Question- Which of the instruction is not used for input?
A) IN
B) INS
C) INS
D) OUT

Answer- D

Question- Which of the instruction is not used for input?
A) IN
B) INS
C) INS
D) OUTS

Answer- D

Question- Which of the instruction is not used for input?
A) IN
B) INS
C) INS
D) OUTSB

Answer- D

Question- Which of the instruction is not used for input?
A) IN
B) INS
C) INS
D) OUTSW

Answer- D

Question- Which of the instruction is not used for input?
A) IN
B) INS
C) INS
D) OUTSD

Answer- D

Question- Which of the instruction is not used for output?
A) OUT
B) OUTSB
C) OUTS
D) IN

Answer- D

Question- Which of the instruction is not used for output?
A) OUT
B) OUTSB
C) OUTS
D) INS

Answer- D

Question- Which of the instruction is not used for output?
A) OUT
B) OUTSB
C) OUTS
D) INSB

Answer- D

Question- Which of the instruction is not used for output?
A) OUT
B) OUTSB
C) OUTS
D) INSW

Answer- D

Question- Which of the instruction is not used for output?
A) OUT
B) OUTSB
C) OUTS
D) INSD

Answer- D

Question- Which fields are considered during I/O instructions?
A) CPL
B) IOPL
C) Both A and B
D) None of these

Answer- C

Question- Which condition is required for IN instruction?
A) CPL = IOPL
B) CPL <= IOPL
C) CPL > IOPL
D) None of these

Answer- B

Question- Which condition is required for INS instruction?
A) CPL = IOPL
B) CPL <= IOPL
C) CPL > IOPL
D) None of these

Answer- B

Question- Which condition is required for INSB instruction?
A) CPL = IOPL
B) CPL <= IOPL
C) CPL > IOPL
D) None of these

Answer- B

Question- Which condition is required for INSW instruction?
A) CPL = IOPL
B) CPL <= IOPL
C) CPL > IOPL
D) None of these

Answer- B

Question- Which condition is required for INSD instruction?
A) CPL = IOPL
B) CPL <= IOPL
C) CPL > IOPL
D) None of these

Answer- B

Question- 1
A) Which condition is required for OUT instruction?

B) CPL = IOPL
C) CPL <= IOPL
D) CPL > IOPL
Answer- None of these

Question- Which condition is required for OUTS instruction?
A) CPL = IOPL
B) CPL <= IOPL
C) CPL > IOPL
D) None of these

Answer- B

Question- Which condition is required for OUTSB instruction?
A) CPL = IOPL
B) CPL <= IOPL
C) CPL > IOPL
D) None of these

Answer- B

Question- Which condition is required for OUTSW instruction?
A) CPL = IOPL
B) CPL <= IOPL
C) CPL > IOPL
D) None of these

Answer- B

Question- Which condition is required for OUTSD instruction?
A) CPL = IOPL
B) CPL <= IOPL
C) CPL > IOPL
D) None of these

Answer- B

Question- Which condition is generating exception for IN instruction?
A) CPL = IOPL
B) CPL < = IOPL
C) CPL > IOPL
D) None of these

Answer- C

Question- Which condition is generating exception for INS instruction?
A) CPL = IOPL

B) CPL <= IOPL
C) CPL > IOPL
D) None of these

Answer- C

Question- Which condition is generating exception for INSB instruction?
A) CPL = IOPL
B) CPL <= IOPL
C) CPL > IOPL
D) None of these

Answer- C

Question- Which condition is generating exception for INSW instruction?
A) CPL = IOPL
B) CPL <= IOPL
C) CPL > IOPL
D) None of these
Answer- C

Answer- C

Question- Which condition is generating exception for OUT instruction?
A) CPL = IOPL
B) CPL <= IOPL
C) CPL > IOPL
D) None of these

Answer- D

Question- Which condition is generating exception for INSD instruction?
A) CPL = IOPL
B) CPL <= IOPL
C) CPL > IOPL
D) None of these

Answer . C

Question- Which condition is generating exception for OUTS instruction?
A) CPL = IOPL
B) CPL <= IOPL
C) CPL > IOPL
D) None of these

Answer- C

Question- Which condition is generating exception for OUTSB instruction?
A) CPL = IOPL
B) CPL <= IOPL
C) CPL > IOPL
D) None of these

Answer- C

Question- Which condition is generating exception for OUTSW instruction?
A) CPL = IOPL
B) CPL <= IOPL
C) CPL > IOPL
D) None of these

Answer- C

Question- Which condition is generating exception for OUTSD instruction?
A) CPL = IOPL
B) CPL <= IOPL
C) CPL > IOPL
D) None of these

Answer- C

Question- IN and OUT instruction drives the 80386 M/IO# pin low
A) True
B) false
C) Both A & B
D) None of the above

Answer- A

Question- IN and OUT instruction drives the 80386 M/IO# pin high
A) True
B) false
C) Both A & B
D) None of the above

Answer- B

Question- M/IO# pin is used to differentiate between memory and I/O

operations
A) True
B) False
C) Both A & B
D) None of the above

Answer- A

Question- I/O instructions do not go through the segmentation and paging unit
A) True
B) False
C) Both A & B
D) None of these

Answer- A

Question- CPL <= IOPL condition is required for IN instruction?
A) No
B) Yes
C) Both A & B
D) None of these

Answer- B

Question- CPL <= IOPL condition is required for INS instruction?
A) No
B) Yes
C) Both A & B
D) None of these

Answer- B

Question- CPL <= IOPL condition is required for INSB instruction?
A) No
B) Yes
C) Both A & B
D) None of these

Answer- B

Question- CPL <= IOPL condition is required for INSW instruction?
A) No
B) Yes
C) Both A & B
D) None of these

Answer- B

Question- CPL <= IOPL condition is required for INSD instruction?
A) No
B) Yes
C) Both A & B
D) None of these

Answer- B

Question- 1
A) CPL <= IOPL condition is required for OUT instruction?
B) No
C) Yes
D) Both A & B
Answer- None of these
Question- CPL <= IOPL condition is required for OUTS instruction?
A) No
B) Yes
C) Both A & B
D) None of these

Answer- B

Question- CPL <= IOPL condition is required for OUTSB instruction?
A) No
B) Yes
C) Both A & B
D) None of these

Answer- B

Question- CPL <= IOPL condition is required for OUTSW instruction?
A) No
B) Yes
C) Both A & B
D) None of these

Answer- B

Question- CPL <= IOPL condition is required for OUTSD instruction?
A) No

B) Yes
C) Both A & B
D) None of these

Answer- B

Question- What is the size of IVT?
A) 1K
B) 2K
C) 3K
D) 4K

Answer- A

Question- What is the byte size of single IVT entry?
A) 1 byte
B) 2 byte
C) 3 byte
D) 4 byte

Answer- D

Question- What is pair is used to point IVT entry?
A) CS:IP
B) DS:IP
C) ES:IP
D) FS:IP

Answer- A

Question- 8 bit vector is shifted by how many bits?
A) 1 bit
B) 2 bit
C) 3 bit
D) 4 bit

Answer- B

Question- Which table is used in protected mode for interrupts and exception?
A) IDT
B) LDT
C) GDT
D) None of the above

Answer- A

Question- The IDT comprises of 8 byte gate descriptor for task, trap or interrupt gates
A) True
B) False
C) Both A & B
D) None of the above

Answer- A

Question- The IDT comprises of ---------- gate descriptor for task, trap or interrupt gates
A) 8 byte
B) 4 byte
C) 2 byte
D) 1 byte

Answer- A

Question- The IDT comprises of 8 byte gate descriptor for ----------
A) Task
B) trap
C) interrupt gates
D) all of the above

Answer- D

Question- The IDT has maximum size of ------ descriptors
A) 255
B) 256
C) 257
D) None of the above

Answer- B

Question- IDTR stands for ----------
A) Interrupt Descriptor Table register
B) Interrupt definition table register
C) Interrupt default table register
D) None of the above

Answer- A

Question- IDT stands for ----------
A) Interrupt Descriptor Table
B) Interrupt definition table
C) Interrupt default table

D) None of the above

Answer- A

Question- IDT contains -------
A) Vectors
B) Gate descriptors
C) Gates
D) Tasks

Answer- B

Question- IDTR register is how many bits?
A) 32 bits
B) 64 bits
C) 48 bits
D) None of the above

Answer- C

Question- Where IDT will reside?
A) Anywhere in physical memory
B) Anywhere in virtual memory
C) Both A & B
D) None of the above

Answer- A

Question- IDTR consist of base address of ----
A) 8 bits
B) 16 bits
C) 24 bits
D) 32 bits

Answer- D

Question- IDTR consists of Limit size of ----
A) 8 bits
B) 16 bits
C) 24 bits
D) 32 bits

Answer- B

Question- Which instruction is used to load interrupts?

A) LLDT
B) LGDT
C) LIDT
D) None of the above

Answer- C

Question- Which instruction is used to store interrupts?
A) SLDT
B) SGDT
C) SIDT
D) None of the above

Answer- C

MP Unit-4 Input-Output, Exceptions and Interrupts MCQ's PART-B (2 Marks Questions)

Question- The size of segment selector in interrupt gates is
A) 20 bits
B) 16 bits
C) 32 bits
D) None of the above

Answer- B

Question- Upon execution of IRET instruction,
A) EFLAGs will be reset
B) EFLAGs will be set
C) EFLAGs will be popped from stack
D) A or B

Answer- C

Question- When IF flag cleared in interrupt gate descriptor, then
A) 80386 POP status of EFLAG
B) 80386 returns to the main program
C) 80386 masks further hardware initiated interrupts
D) None of the above

Answer- C

Question- Which is not the type of IDT descriptors?
A) Trap gates
B) System gates
C) Task gates
D) Interrupt gate

Answer- B

Question- Which gate gives information regarding privilege level violation exception
A) Trap
B) Task
C) IDT
D) None of the above

Answer- B

Question- The task can be invoked indirectly by jumping or calling gate, only when
A) CPL is higher than DPL
B) RPL is higher than CPL
C) RPL is lower than DPL
D) None of the above

Answer- B

Question- If all 256 descriptor are not required the limit can be set to -----
A) 7FF H
B) FFF H
C) 6FF H
D) None of the above

Answer- A

Question- The address range for memory bank is from ------- to ----------
A) 0000 to FFFF
B) 000A to FFFF
C) 0001 to FFFE
D) 0001 to 000F

Answer- A

Question- The address range for 80386 to 80387 is from ------- to -------
A) 0000 to FFFF
B) 800000F8 to 800000FF
C) 8000 to 8FFF
D) 8000 to 800F

Answer- B

Question- The address range for memory bank is from ------- to -----------
A) 0000 to FFFF
B) 000 to FFF
C) 00 to FF
D) 0 to F

Answer- A

Question- A task with privilege level 0, does not refer to all the lower level privilege descriptors in
A) GDT (global descriptor table)
B) LDT (local descriptor table)
C) IDT (interrupt descriptor table)
D) None of the given

Answer- B

Question- processor detects following condition while translating a linear address to a physical address
A) The page-directory or page-table entry needed for the address translation has zero in its present bit
B) The current procedure does not have sufficient privilege to access the indicated page.
C) Both A and B
D) B only

Answer- C

Question- In page fault error code tells the exception handler
A) Whether the exception was due to a not present page or to an access rights violation.
B) Whether the processor was executing at user or supervisor level at the time of the exception
C) Whether the memory access that caused the exception was a read or write.
D) All of these

Answer- D

Question- To insure a proper TSS to process it, the handler for exception 10 must be a task

invoked
Via_____.
A) Trap gate
B) System gate
C) Task gate
D) None of these

Answer- C

Question- This error code CS id + EXT not indicates condition_____
A) Stack segment selector RPL < > CPL
B) Stack segment selector is outside table limit
C) Code segment selector is not outside table limit
D) None of these

Answer- D

Question- To determine when two faults are to be signaled as a double fault, the 80386 divides the exceptions into ____types
A) 1
B) 2
C) 3
D) 4

Answer- C

Question- Which is not the class of double fault exception?
A) benign exceptions
B) contributory exceptions
C) page faults
D) None of these

Answer- D

Question- Interrupt 4- occurs after execution of _____instruction
A) INTO
B) OF
C) IF
D) Both A and B

Answer- D

Question- The processor sets the ____ bit if an event external to the program caused the exception.
A) RST
B) EXT

C) ERR
D) None of the above

Answer- B

Question- Which instruction used to access interrupt descriptor table?
A) LGDT
B) IIDT
C) SIDT
D) All the above

Answer- C