Segmentation unit allows segments of _____ size at maximum.

A. 4Gbytes

B. 6Mbytes

C. 4Mbytes

D. 6Gbytes

ANSWER: A

If _____input pin of 80386 if activated, allows address pipelining during 80386 bus cycles.

A. BS16

B. NA

C. PEREQ

D. ADS

ANSWER: B

Virtual Mode Flag bit can be set using ____ instruction or any task switch operation only in the _____ mode

A. IRET, Virtual

B. POPF, Real

C. IRET, protected

D. POPF, protected

ANSWER: C

The interrupt vector table of 80386 has been allocated _____ space starting from _____ to _____.

A. 1Kbyte, 00000H, 003FFH

B. 2Kbyte, 10000H, 004FFH

C. 3Kbyte, 01000H, 007FFH

D. 4Kbyte, 01000H, 009FFH

ANSWER: A

The ___ bit decides whether it is a system descriptor or code/data segment descriptor

A. P

B. S

C. D

D. G

ANSWER: B

A new signal group on the 80486 is the _____.

A. PARITY

B. DP0-DP3

C. PCHK

D. all

ANSWER: D

_____is used to control the cache with two new control bits not present in the 80386 microprocessor. What are the bits used to control the 8K byte cache?

A. CR0, CD, NW

B. CR0, NW, PWT

C. Control Register Zero, PWT, PCD

D. none

ANSWER: A

To prevent another master from taking over the bus during a critical operation, the 486 can assert its _____signal.

A. LOCK# or PLOCK#

B. HOLD or BOFF

C. HLDA

D. HOLD

ANSWER: A

80386 support which type of descriptor table from the following?

A. TDS

B. ADS

C. GDS

D. MDS

ANSWER: C

80386 support overall ___ addressing modes to facilitate efficient execution of higher level language programs.

A. 9

B. 10

C. 11

D. 12

ANSWER: C

Direction flag is used with

A. String instructions.

B. Stack instructions.

C. Arithmetic instructions.

D. Branch instructions.

ANSWER: A

Ready pin of a microprocessor is used

A. to indicate that the microprocessor is ready to receive inputs.

B. to indicate that the microprocessor is ready to receive outputs.

C. to introduce wait states.

D. to provide direct memory access.

ANSWER: C

These are two ways in which a microprocessor can come out of Halt state.

A. When hold line is a logical 1.

B. When interrupt occurs and the interrupt system has been enableD.

C. When both (A) and (B) are true.

D. When either (A) or (B) are true.

ANSWER: A

The Pentium microprocessor has_____execution units.

A. 1

B. 2

C. 3

D. 4

ANSWER: C

8088 microprocessor has

A. 16 bit data bus

B. 4 byte pre-fetch queue

C. 6 byte pre-fetch queue

D. 16 bit address bus

ANSWER: D

Question No.	*Question*				*Answer Key*
1.	*Q.The 80386 does not wrap the addresses at ---------- in real address mode*				*Ans:* *B*
	A:2 megabyte	*B: 1 megabyte*	*C:2 KB*	*D:1 KB*	
2.	*Q.Paging mechanism in 80386X is ---------- in real mode*				*Ans:* *B*
	A:Active	*B:Not Active*	*C:Neutal*	*D:None of these*	
3.	*Q.All segments in ------- mode are maximum 64KB long*				*Ans:* *B*
	A:Proctected mode	*B:Real mode*	*C:Both modes*	*D:All of these*	
4.	*Q.The 80386 always uses ----- for any coprocessor error exception*				*Ans:* *C*
	A:Interrupt vector 12	*B: Interrupt vector 14*	*C: Interrupt vector 16*	*D: All of these*	
5.	*Q.In 80386DX a logical address is also known as------ consist of selector and an offset*				*Ans:* *C*
	A:Physical address	*B: Logical address*	*C: Virtual address*	*D: None of these*	

6.	*Q.The 80386 concatenates the two fragments of the limit field to form a ---------- value*				*Ans: A*
	A: 20 bit	*B: 20 byte*	*C: 18 bit*	*D: 18 byte*	
7.	*Q.Global descriptor table register(GDTR) is a ------- register located inside the 80386DX*				*Ans: D*
	A: 50 bit	*B: 48 byte*	*C: 50 byte*	*D: 48 bit*	
8.	*Q.Paging is the ---------- phase of address translation*				*Ans: B*
	A: First	*B: Second*	*C: Third*	*D: Fourth*	
9.	*Q.The paging mechanism receives a ------- linear address from the segmentation unit*				*Ans: C*
	A:8 bit	*B: 16 bit*	*C: 32 bit*	*D: 48 bit*	
10.	*Q.Page level protection involves --------- kind of protection*				*Ans: C*
	A:Restication of addressable domain	*B:Type checking*	*C: Both A & B*	*D:None of these*	
11.	*Q.Nested tasks are analogous to ----- subroutines*				*Ans: C*
	A:Multiple	*B: Single*	*C: Nested*	*D: Hierachial*	
12.	*Q.Paging mechanism allows the sharing of the 8086 operating system code between ----- 8086 applications*				*Ans: C*
	A: Single	*B: Double*	*C: Multiple*	*D: None of these*	
13.	*Q.The 80386 single-step exception has ----- priority then any external interrupt*				*Ans: B*
	A: low	*B: Higher*	*C: Medium*	*D: None of these*	
14.	*Q.The task state segment descriptor for the designated task is checked for its ----- and --------*				*Ans: C*
	A:Limit and Base	*B:base and address*	*C:limit and presence*	*D:base and presence*	
15.	*Q.The Task Register(TR) specify the ----- executing task by pointing to the task State Segment(TSS)*				*Ans: B*
	A:Normal	*B: Currently*	*C: Multiple*	*D: Single*	

1.A 32-bit address bus allows access to a memory of capacity

a. 64 Mb b. 16 Mb c. 1Gb d. 4 Gb

2 .The necessary steps carried out to perform the operation of accessing either memory or I/O Device, constitute a _____

a fetch operation b. execute operation c. machine cycle d. instruction cycle

3. The input pin of 30386Dx is activated allows address pipelining during 80386.

a.BS16 b. NA c. PEREQ d. ADS

4. During physical address calculations segments register contents are shifted by -------

a 2 bits left b. 4 bits left c. 2 bits right d. 4 bits right .

5. The BIU of 8086 consists of ----------

a. segment registers b. Instruction queue c. Instruction pointer d. all of these.

6. During instruction fetch----------and----------register are used.

a. IP,DS b. CS, IP c. SS,BP d. SS,IP

7. The 80386DX can address up to----------physical memory.

a.1Mbytes b. 16Mbytes c. 1Gbytes d. 4 Gbytes

8. Which of the following is not an interrupt signal?

a. INTR b. NMI c.NA# d. RESET .

9. The coprocessor uses ----------signal when it needs to read or write data from memory.

a. BUSY# b. BUSY# and ERROR# c. ERROR# d. PEREQ

10. After reset 80386 starts execution in ----------mode.

a. Real b. Protected c. Virtual 8086 d. none of these.

11. Logical address space of 80386DX is ----------

a.1Mbytes b. 64 Mbytes c. 4Gbytes d .64 Tbytes

12. The least significant 5 bits of the CR0 are called as ----------.

a. Program Status word b. machine Status Word c. Both (a) and (b) d. None of these.

13. If PE=0 the mode selected by the processor is----------

a. Real Mode b. Protected Mode c. Virtual Mode d. All of these

14. The 80386 uses an---------- to locate the base of the vector table and to determine its length.

a. IDTR b. GDTR c. LDTR d .All of these

15 . Exactly ----------segments descriptor has to be defined for each segment memory

a. One b. Two c. Three d. Four

16. The Selector is of ----------bits .

a.10 b. 16 c.32 d.64

17. TI indicates ----------.

a. Task indicator b. Table indicator c. Task identifier d. Table identifier.

18. If the conforming code bit is set then the code segment is executed if

a. CPL>=DPL b. CPL<DPL c. Both (a) and (b) d. none of these

19. When the ----------bit in segment descriptor is zero operands contained within the segments

are of 16 bits.

a. G b. P c .D d. All of these

20. ----------bit determines the type of the segment.

a. D b. G c. S d .P.

21. The extra segment registers in 80386 are- ----------

a. DS,FS b. ES,SS c. FS,GS D.GS,CS

22. 80386DX memory can be organized as…….

a. Pages, Segments b. Segments, Registers c. Pages, Register d. none of these.

23. The 80386DX has a -------bit address bus and -------bit data bus.

a. 16,32 b) 16,16 c)32,32 d)32,16

24. The width of the GDTR and LDTR are----------bits.

a.16,24 b.16,48 c.48,16 d.24,32

25. No of segments in 8086 and 80386DX are --------

a. 4,4 b.4,6 c.6,4 d. 6,6

MULTIPLE CHOICE QUESTIONS (MCQ's)unit-2

1. After reset, the 80386 operates in ……
   (a) real mode (b) protected mode
   (c) virtual 86 mode (d) none of these
2. In real mode, the 80386 ……
   (a) operates like faster 8086 microprocessor
   (b) performs multiple tasking
   (c) provides protection to program and data
   (d) all of above
3. Which register is not supported by 80386 in real mode?
   (a) AX (b) BX
   (c) SI (d) CR1
4. Which register is not supported by 80386 in real mode?
   (a) IP (b) FLAG
   (c) DR6 (d) CR0
5. In real mode, the 80386 contains ……
   (a) 4 segments: CS, SS, DS, ES (b) 4 segments: CS, SS, FS, GS
   (c) 6 segments: CS, SS, DS, ES, FS, GS (d) 2 segments: CS and SS
6. The maximum address size of 80386 in real mode is ……
   (a) 20 bit (b) 21 bits
   (c) 24 bit (d) 32 bit
7. In real mode of 80386, the physical address is also called as ……
   (a) offset address (b) logical address
   (c) effective address (d) linear address
8. What is the size of segment in real mode operation of 80386?

(a) 64 KB (b) 4 GB
(c) changeable from 1 byte to 4 GB (d) 64 TB

9. IDT stands for ……
   (a) Interrupt Description Table (b) Interrupt Descriptor Table
   (c) Identify Description Table (d) Identify Descriptor Table
10. In real mode of 80386, what is the starting address of IDT?
   (a) determined by IDTR (b) 0
   (c) changeable (d) both (a) and (b)
11. In real mode of 80386, what is the limit of IDT?
   (a) determined by IDTR (b) 3FFFH
   (c) changeable (d) both (a) and (b)
12. In real mode of 80386, what is the value of PE bit of CR0 register?
   (a) 1 (b) 0
   (c) X (d) tri-state
13. After self-test of 80386 microprocessor,
   (a) EAX = 03 (b) DH = 03
   (c) SP = 0000H (d) all of above
14. After reset, the 80386 fetches first instruction from address.
   (a) FFF0H (b) 0000H
   (c) FFFF FFF0H (d) cannot be defined
15. What is the use of real mode?
   (a) To initialize peripherals (b) To enable interrupts
   (c) To enter protected mode (d) All of above
16. How to set PE bit of CR0 register?
   (a) Set b PE (b) MOV CR0, doubleword
   (c) LSMW word_data (d) (b) or (c)
17. For entering into protected mode from real mode, the programmer should maintain ……
   (a) Interrupt Descriptor Table (IDT) (b) Global Descriptor Table (GDT)
   (c) Local Descriptor Table (LDT) (d) (a) or (b) or (c)
   (e) (a) and (b) and (c)
18. Which is not supported in real mode of 80386?
   (a) Base only value (b) Present bit (P) = 1
   (c) Granular bit (G) = 0 (d) Limit any value
19. In 80386, which is simple and less complex mode of operation?
   (a) real mode (b) protected mode
   (c) virtual 86 mode (d) both (a) and (c)
20. In real mode, what is the size of registers?
   (a) 16 bit (b) 24 bit
   (c) 32 bit (d) 64 bit
21. In real mode of 80386, how much memory can be accessed by 80386?
   (a) 64 KB (b) 1 MB
   (c) 4 GB (d) 64 TB
22. In real mode of 80386, what is the size of address bus?
   (a) 20 bits (b) 21 bits
   (c) 32 bits (d) 64 bits
23. In real mode of 80386, what is the size of interrupt vector table?
   (a) 64 KB (b) 1 KB

(c) depends on generated interrupts (d) changeable

Answers

1.	*(a)*	*2.*	*(a)*	*3.*	*(d)*	*4.*	*(c)*	*5.*	*(c)*	*6.*	*(b)*	*7.*	*(d)*	*8.*	*(a)*	*9.*	*(b)*		
11.	*(b)*	*12.*	*(b)*	*13.*	*(b)*	*14.*	*(c)*	*15.*	*(d)*	*16.*	*(d)*	*17.*	*(d)*	*18.*	*(d)*	*19.*	*(a)*		
21.	*(b)*	*22.*	*(b)*	*23.*	*(b)*														

MULTIPLE CHOICE QUESTIONS (MCQ's)

1. What is the segment size in 80386 microprocessor?
   (a) 64 KB (b) 1 MB
   (c) 4 GB (d) Any size from 1 byte to 4 GB
2. Which value of RPL in segment selector gives highest privilege level?
   (a) 0 (b) 1
   (c) 2 (d) 3
3. Which value of RPL in segment selector gives lowest privilege level?
   (a) 0 (b) 1
   (c) 2 (d) 3
4. What DPL field of segment descriptor indicates?
   (a) privilege level of segment
   (b) privilege level of segment descriptor
   (c) privilege level of descriptor table
   (d) all of above
5. What segment descriptor contains?
   (a) Base address of segment
   (b) Limit of size of segment
   (c) Access right byte
   (d) All of above
6. What is the size of segment descriptor?
   (a) 16 bits (b) 32 bits
   (c) 48 bits (d) 64 bits
7. What is the size of limit field in segment descriptor of 80386 microprocessor?
   (a) 8 bits (b) 16 bits

(c) 20 bits (d) 32 bits

8. For conforming code segment, code executes when ……
   (a) CPL = DPL (b) CPL > DPL
   (c) CPL < DPL (d) (a) or (b)
9. One GDT contains how many descriptors?
   (a) 256 (b) 2k
   (c) 4k (d) 8k
10. One IDT contains how many descriptors?
   (a) 256 (b) 2k
   (c) 4k (d) 8k
11. What is maximum size of GDT?
   (a) 4 kB (b) 8 kB
   (c) 32 kB (d) 64 kB
12. How many GDT is/are present in 80386 microprocessor?
   (a) 1 (b) 256
   (c) 8K (d) Many, one for each task
13. How many IDT is/are present in 80386 microprocessor?
   (a) 1 (b) 256
   (c) 8k (d) Many, one for each interrupt
14. How many LDTs can be present in 80386 microprocessor?
   (a) 1 (b) 256
   (c) 8k (d) Many, one for each task
15. What is the size of IDT?
   (a) 1K (b) 2K
   (c) 8K (d) 64K
16. How many segment descriptors are present in GDT or LDT?
   (a) 1024 (b) 4096
   (c) 8192 (d) 256
17. What is the size of segment selector?
   (a) 16 bit (b) 32 bit
   (c) 48 bits (d) 64 bits
18. What is used in segment selector to select GDT or LDT?
   (a) Index field (b) TI field
   (c) RPL field (d) All of these
19. What is the use of index field present in segment selector?
   (a) To select GDT (b) To select LDT
   (c) (a) or (b) (d) To select segment descriptor
20. What is the size of index field in segment selector?
   (a) 13 bit (b) 14 bit
   (c) 15 bit (d) 16 bit

21. How many segment selectors are present in 80386?
    (a) 1 (b) 4
    (c) 6 (d) 8
22. If T1 = 0 in segment selector then …… is selected.
    (a) GDT (b) LDT
    (c) IDT (d) TSS
23. If TI = 1 in segment selector then …… is selected.
    (a) GDT (b) LDT
    (c) IDT (d) TSS
24. The first entry in GDT is called as ……
    (a) special descriptor (b) zero descriptor
    (c) null descriptor (d) segment descriptor
25. In 80386, …… is/are null selector value(s).
    (a) 0000H (b) 0001H
    (c) 0002H (d) All of these
26. The segment descriptor ……
    (a) describes a segment (b) must be created for every segment
    (c) is created by the programmer (d) all of above
27. What is the size of base address in segment descriptor of 80386?
    (a) 20 bit (b) 24 bit
    (c) 32 bit (d) 16 bit
28. What is the size of limit field in segment descriptor of 80386?
    (a) 20 bit (b) 24 bit
    (c) 16 bit (d) 32 bit
29. Which is non-system segment descriptor?
    (a) code (b) stack
    (c) data (d) all of these
30. Which is not non-system segment descriptor?
    (a) Code (b) Data
    (c) Call gate (d) Stack
32. Which is not system segment descriptor?
    (a) Code (b) LDT descriptor
    (c) Call gate (d) TSS descriptor
33. In segment descriptor of 80386, if D = 0 then the operand size is ……
    (a) 16 bit (b) 20 bit
    (c) 24 bit (d) 32 bit
34. In segment descriptor of 80386, if D = 1 then the operand size is ……
    (a) 16 bit (b) 20 bit
    (c) 24 bit (d) 32 bit
35. What is the use of Granularity (G) bit which is present in segment descriptor?
    (a) To determine size of segment
    (b) To determine multiplying factor of limit

(c) To decide size of operand
(d) All of above

36. If limit field is 1FFFH, then for data segment ……
    (a) First addressable byte is at offset 000H
    (b) First addressable byte at offset 2000H
    (c) First addressable byte at offset 1FFFH
    (d) Cannot determine
37. If limit field is 1FFFH, then for data segment ……
    (a) Last addressable byte at offset 1FFFH
    (b) Last addressable byte at offset FFFFH
    (c) Last addressable byte at offset 2000H
    (d) Cannot determine
38. If limit field is 1FFFH, then for stack segment ……
    (a) Last addressable byte at offset 0000H
    (b) Last addressable byte at offset 2000H
    (c) Last addressable byte at offset 1FFFH
    (d) Last addressable byte at offset 2000H
39. If limit field is 1FFFH then for stack segment last addressable byte is at offset ……
    (a) 2000H (b) 1FFFH
    (c) FFFFH (d) cannot determine
40. In non-system segment descriptor, if E = 0, then it defines ……
    (a) data segment (b) code segment
    (c) stack segment (d) both (a) and (c)
41. In non-system segment descriptor, if E = 1, then it defines ……
    (a) data segment (b) code segment
    (c) code segment (d) both (a) and (c)
42. What is the type number of LDT descriptor?
    (a) 2 (b) B
    (c) 9 (d) 5
43. How many bits are used for type field in system segment descriptor?
    (a) 3 (b) 4
    (c) 5 (d) all of these
44. What is the type number of gate descriptors?
    (a) 4 (b) 5
    (c) 6 (d) all of these
45. What is the type number of gate descriptors?
    (a) 7 (b) c
    (c) E (d) all of these
46. What is the use of call gate?
    (a) It acts as interface layer between code segment at different privilege levels

(b) To handle interrupts
(c) It acts as interface point between user code and a task state segment
(d) To handle exceptions

47. What is the use of trap gate?
(a) It acts as interface layer between code segments at different privilege levels
(b) To handle interrupts
(c) To handle exceptions
(d) Both (b) and (c)

48. What is the use of task gate descriptor?
(a) To handle interrupts
(b) To handle exceptions
(c) To define, a memory segment for task
(d) It acts as an interface point between user code and a TSS

49. The selector field of system segment descriptor contains ……
(a) CS selector (b) DS selector
(c) SS selector (d) both (a) and (b)

50. The TSS descriptors are present in ……
(a) GDT (b) LDT
(c) IDT (d) Both (a) and (b)

51. What is the type number of task gate descriptor?
(a) 4 (b) 5
(c) 6 (d) 7

52. What is the type number of TSS descriptor of 80386?
(a) 9 (b) B
(c) c (d) both (a) and (b)

53. What is the type number of CALL gate descriptor of 80386?
(a) A (b) B
(c) C (d) D

54. What is the type number of trap gate descriptor of 80386?
(a) A (b) B
(c) E (d) F

55. What is the type number of interrupt gate descriptor of 80386?
(a) A (b) B
(c) D (d) E

56. The limit field of GDTR contains 00FFH, then the size of GDT is ……
(a) 255 bytes (b) 256 bytes
(c) 254 bytes (d) 257bytes

57. In segment descriptor, Access Right Byte is from …… to ……
(a) D40 to D47 (b) D48 to D55
(c) D56 to D63 (d) D0 to D7

58. What is the size of GDTR?
    (a) 16 bit (b) 24 bit
    (c) 32 bit (d) 48 bit
59. What is the size of LDTR?
    (a) 16 bit (b) 24 bit
    (c) 32 bit (d) 48 bit
60. What is the size of IDTR?
    (a) 16 bit (b) 24 bit
    (c) 32 bit (d) 48 bit
61. What is the size of MSW?
    (a) 16 bit (b) 24 bit
    (c) 32 bit (d) 48 bit
62. What is the use of LDTR?
    (a) To point to memory segment
    (b) To point to LDT
    (c) It gives selector which points to an LDT descriptor present in LDT
    (d) It gives selector which points to an LDT descriptor present in GDT
63. The 80386DX contains ……
    (a) logical address (b) linear address
    (c) physical address (d) all of above
64. If paging is not used then ……
    (a) physical address is same as logical address
    (b) physical address is same as linear address
    (c) linear address is same as logical address
    (d) all addresses are same
65. During execution of program, if an attempt is made to access the segment, then the access is allowed only if the selector has ……
    (a) same privilege level (b) lower privilege level
    (c) higher privilege level (d) (a) or (c)
66. In aliasing, if a data segment descriptor and a code segment descriptor have the same base address and limit fields, then we can ……
    (a) write into code space
    (b) execute data space
    (c) both (a) and (b)
    (d) the 80386 generates an exception
67. Privileged instructions are executed at privilege level ……
    (a) 0 (b) 1
    (c) 2 (d) 3
68. In 80386, privilege levels are defined by ……
    (a) DPL (b) CPL

(c) RPL (d) All of above

69. Which is not privileged instruction?
    (a) HLT (b) LOCK
    (c) LTR (d) LMSW
70. An application cannot execute input/output instruction if ……
    (a) CPL > IOPL (b) CPL = IOPL
    (c) CPL < IOPL
71. In which segment descriptor word count field is present?
    (a) Interrupt gate (b) Trap gate
    (c) Call gate (d) None of these
72. …… instruction can be used to change privilege levels.
    (a) FAR CALL (b) Near JMP
    (c) FAR JMP (d) NEAR CALL
73. Which following statement is right for call gate?
    (a) Target DPL <= Max (RPL< CPL) <= Gate DPL
    (b) Max(RPL, CPL) <= Target DPL <= Gate DPL
    (c) Gate DPL <= Max (RPL, CPL) <= Target DPL
    (d) Target DPL <= Gate DPL <= Max (RPL, CPL)
74. DPL indicates the privilege level of ……
    (a) memory segment (b) segment descriptor
    (c) current program (d) memory segment to be accessed
75. RPL indicates the privilege level of ……
    (a) memory segment (b) segment descriptor
    (c) current program (d) memory segment to be accessed
76. CPL indicates the privilege level of ……
    (a) memory segment (b) segment descriptor
    (c) current program (d) memory segment to be accessed
77. A program running at privilege level 2 can access the stack which is at privilege level ……
    (a) 2 (b) 0, 1
    (c) 3 (d) 2, 3
78. The task state segment saves stack segment selector and stack pointers for privilege levels …… and ……
    (a) 0, 1 (b) 1, 2
    (c) 0, 1, 2 (d) 0, 1, 2, 3
79. In changing stack operation, what is pushed onto the new stack?
    (a) old SS : ESP (b) old CS : EIP
    (c) parameters of old stack (d) all of above
80. If paging is enabled then ……
    (a) logical address is converted to physical address

(b) linear address is converted to physical address
(c) logical address is converted to linear address
(d) logical address is converted to virtual address

81. If paging is disabled then,
(a) logical address is same as physical address
(b) virtual address is same as physical address
(c) all three addresses are same
(d) all three addresses are different

82. In paging, for converting linear address to physical address …… register is used.
(a) CR0 (b) CR1
(c) CR2 (d) CR3

83. Which component is required for paging mechanism?
(a) page directory (b) page table
(c) PDBR (d) all of these

84. In linear address, … bit directory field is used as an index to the page directory.
(a) 10 (b) 12
(c) 13 (d) 24

85. In linear address, …… bit page field is used as an index to the page table.
(a) 10 (b) 12
(c) 13 (d) 24

86. In linear address, …… bits are used as offset field.
(a) 10 (b) 12
(c) 24 (d) 32

87. What is the size of page directory?
(a) 4 KB (b) 8 KB
(c) 64 KB (d) changeable

88. What is the size of page table?
(a) 4 KB (b) 8 KB
(c) 64 KB (d) changeable

89. What is the size of page frame?
(a) 4 KB (b) 8 KB
(c) 64 KB (d) changeable

90. Paging can be enabled or disabled by using PG bit present in …… register.
(a) CR0 (b) CR1
(c) CR2 (d) CR3

91. The TLB holds the recent …… entries of page tables.
(a) 16 (b) 32
(c) 64 (d) none of these

92. In page table entry, ……bits are used to store address of a page frame.
(a) 12 bits (b) 20 bits

(c) 24 bits (d) 32 bits

93. What is the privilege level of supervisor code?
(a) 0 (b) 1
(c) 2 (d) all of these

94. In 80386, …… page alignment is done on all pages.
(a) 0 byte (b) 1 byte
(c) 4 KB (d) 64 KB

95. What is the exception number of page fault?
(a) 12 (b) 13
(c) 14 (d) 15

96. If present (P) bit in Page Table Entry is 0, then …… of memory is not present.
(a) 4 KB (b) 4 MB
(c) 8 KB (d) 4 GB

97. If present (P) bit in Page Directory Entry is 0, then …… of memory is not present.
(a) 4 KB (b) 8 KB
(c) 4 MB (d) 4 GB

98. What is the size of page table entry and page directory entry?
(a) 16 bit (b) 24 bit
(c) 32 bit (d) 64 bit

99. If page fault generates then …… address is stored in …… register.
(a) physical, CR2 (b) physical, CR3
(c) linear, CR2 (d) linear, CR3

100. One Page Directory Entry is used to access …… of memory.
(a) 4 KB (b) 4 MB
(c) 1 MB (d) 1 byte to 4 GB

101. One Page Table Entry is used to access …… of memory.
(a) 4 KB (b) 4 MB
(c) 1 MB (d) 1 byte to 4 GB

102. What is included in segment level protection?
(a) Type check and limit check
(b) Restriction of procedure entry point
(c) Restriction of instructions
(d) All of above

103. Which bit of PTE or PDE is not used in page level protection?
(a) P (b) $U/\overline{S}$
(c) $R/\overline{W}$ (d) A

104. In 80386, the protection mechanism supports …… levels of protection.
(a) 3 (b) 4
(c) 5 (d) 6

105. What is the minimum size of TSS in 80386?
   (a) 64 bytes (b) 104 bytes
   (c) 4 KB (d) 64 KB
106. What is the size of visible part present in TR of 80386?
   (a) 16 bit (b) 20 bit
   (c) 24 bit (d) 32 bit
107. How task switching can be obtained in 80386?
   (a) The current task JMPs or CALLs a TSS descriptor
   (b) The current task JMPs or CALLs a task gate
   (c) An interrupt or exception selects a task gate
   (d) All of above
108. To return from a task, …… instruction is used.
   (a) RET (b) IRET
   (c) JMP (d) CALL
109. Nested task switching is done by ……
   (a) using FAR CALL instruction (b) exception
   (c) fault or trap (d) all of above
110. In input/output permission bitmap, each bit corresponds to a single …… wide input/output address.
   (a) bit (b) byte
   (c) word (d) double word
111. To enter in protected mode, …… bit should be at logic 1.
   (a) PG (b) ET
   (c) PE (d) NT
112. The interrupt vector table of 80386 has been allocated …… space starting from …… to ……
   (a) 1Kbyte, 00000H, 003FFH (b) 2Kbyte, 10000H, 004FFH
   (c) 3Kbyte, 01000H, 007FFH (d) 4Kbyte, 01000H, 009FFH
113. The …… bit decides whether it is a system descriptor or code/data segment descriptor
   (a) P (b) S
   (c) D (d) G

Answers

1. (d)	*2. (a)*	*3. (d)*	*4. (a)*	*5. (d)*	*6. (d)*	*7. (c)*	*8. (d)*	*9. (d)*	*10.(a)*
11.(d)	*12.(a)*	*13.(a)*	*14.(b)*	*15.(b)*	*16.(c)*	*17.(a)*	*18.(b)*	*19.(d)*	*20.(a)*
21.(c)	*22.(a)*	*23.(b)*	*24.(c)*	*25.(d)*	*26.(d)*	*27.(c)*	*28.(a)*	*29.(d)*	*30.(c)*
31.(a)	*32.(a)*	*33.(a)*	*34.(d)*	*35.(b)*	*36.(a)*	*37.(a)*	*38.(d)*	*39.(c)*	*40.(d)*
41.(c)	*42.(a)*	*43.(b)*	*44.(d)*	*45.(d)*	*46.(a)*	*47.(d)*	*48.(d)*	*49.(a)*	*50.(a)*
51.(b)	*52.(d)*	*53.(c)*	*54.(d)*	*55.(d)*	*56.(b)*	*57.(a)*	*58.(d)*	*59.(a)*	*60.(d)*
61.(a)	*62.(d)*	*63.(d)*	*64.(b)*	*65.(d)*	*66.(c)*	*67.(a)*	*68.(d)*	*69.(b)*	*70.(a)*

71.(c)	*72.(a)*	*73.(a)*	*74.(a)*	*75.(d)*	*76.(c)*	*77.(a)*	*78.(c)*	*79.(d)*	*80. (b)*
81.(b)	*82.(d)*	*83.(d)*	*84.(a)*	*85.(a)*	*86.(b)*	*87.(a)*	*88.(a)*	*89.(a)*	*90.(a)*
91.(b)	*92.(b)*	*93.(d)*	*94.(c)*	*95.(c)*	*96.(a)*	*97.(c)*	*98.(c)*	*99.(c)*	*100.(b)*
101.(a)	*102.(d)*	*103.(d)*	*104.(b)*	*105.(b)*	*106.(a)*	*107.(d)*	*108.(b)*	*109.(d)*	*110.(b)*
111.(c)	*112.(a)*	*113.(b)*							

MULTIPLE CHOICE QUESTIONS (MCQ's)

1. How much virtual memory can be accessed by 80386?
   (a) 64 KB (b) 1 MB
   (c) 4 GB (d) 64 TB
2. In virtual 86 mode of 80386, one program can access …… of memory.
   (a) 64 KB (b) 1 MB
   (c) 4 GB (d) 64 TB
3. What is the advantage of virtual 86 mode?
   (a) Execution of 8086 applications with protection
   (b) Multitasking
   (c) Multiuser
   (d) All of above
4. In virtual 86 mode of 80386, what is the size of address bus?
   (a) 20 bit (b) 21 bit
   (c) 24 bit (d) 32 bit
5. How 80386 can switch to virtual 86 mode?
   (a) Through a task switch
   (b) An IRET instruction from a procedure
   (c) both (a) and (b)
   (d) after reset
6. Which descriptor table should be maintained for switching to virtual 86 mode?
   (a) Interrupt Descriptor Table (IDT) (b) Global Descriptor Table
   (c) Local Descriptor Table (d) None of above
7. Which control register is used when a virtual mode is invoked?
   (a) CR0 (b) CR1
   (c) CR2 (d) CR3
8. In virtual 8086 mode ……
   (a) paging can be enabled (b) paging can be disable
   (c) (a) or (b)
9. Which register is used in virtual 86 mode?
   (a) CR0 (b) CR1

(c) CR2 (d) CR3

10. What is the size of memory segment in virtual 86 mode?
    (a) 64 KB (b) 1 MB
    (c) 4 GB (d) changeable from 1 byte to 4 GB
11. If CS = F000H and IP = FFF0H, what is the linear address generated in virtual 86 mode?
    (a) FFFF0H (b) FFFFFH
    (c) 000FFFFH (d) Give data is invalid
12. Virtual Mode Flag bit can be set using …… instruction or any task switch operation only in the …… mode.
    (a) IRET, Virtual (b) POPF, Real
    (c) IRET, protected (d) POPF, protected
13. In a virtual memory system, the addresses used by the programmer belongs to ……
    (a) memory space (b) physical addresses
    (c) address space (d) main memory address

Answers

1. (d)	*2. (b)*	*3. (d)*	*4. (b)*	*5. (c)*	*6. (d)*	*7. (d)*	*8. (c)*	*9. (d)*	*10. (a)*
11. (a)	*12. (c)*	*13. (c)*							