Unit - III

5 Protection

Q.1 The 80386 uses _____ level protection mechanism(s) to protect critical sections.

[a] segment [b] privilege
[c] a and b both [d] none of these [Ans. : c]

Q.2 Which of the following checking mechanisms are provided by 80386 ?

[a] Limit [b] Type [c] Privilege [d] All of these
[Ans. : d]

Q.3 The 80386 does _____ checking during segment level protection.

[a] limit [b] type [c] limit and type [d] privilege
[Ans. : c]

Q.4 _____ field of the descriptor specifies the type of descriptor and the intend usage of the segment.

[a] Type [b] Limit
[c] Type and limit [d] None of these [Ans. : a]

Q.5 Which of the following is/are the type(s) of segment ?

[a] Readable [b] Conforming
[c] Expanded-down [d] All of these. [Ans. : d]

Q.6 The 80386DX uses _____ field of a segment descriptor to prevent program from addressing outside the segment.

[a] type [b] limit
[c] type and limit [d] none of these [Ans. : b]

Q.7 In which of the following case(s), the 80386DX causes a general protection exception when program attempts to _____.

[a] access memory byte at an address > limit
[b] access memory word at an address ≥ limit
[c] access memory D word at an address ≥ (limit-2)
[d] All of these [Ans. : d]

Q.8 Selector holds _____.

[a] RPL [b] DPL [c] CPL [d] All of these
[Ans. : a]

Q.9 Privilege level for user applications program is _____.

[a] 0 [b] 1 [c] 2 [d] 3 [Ans. : d]

Q.10 Privilege level for custom device drivers is _____.

[a] 0 [b] 1 [c] 2 [d] 3 [Ans. : c]

Q.11 Privilege level for system services such as BIOS procedures is _____.

[a] 0 [b] 1 [c] 2 [d] 3 [Ans. : b]

Q.12 Privilege level for operating system kernel is _____.

[a] 0 [b] 1 [c] 2 [d] 3 [Ans. : a]

Q.13 The access right bytes of a segment contains FEH. Which of the following statement is true ?

[a] Privilege level 2 [b] Not readable code segment
[c] Conforming code segment
[d] Segment selector has been loading into segment register.
[Ans. : c]

Q.14 The access right bytes of a segment contains FEH. What is the DPL ?

[a] 0 [b] 1 [c] 2 [d] 3 [Ans. : d]

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Q.15 The access right bytes of a segment contains FEH. What is type of segment ?

[a] Readable [b] Executable
[c] Conforming code [d] All of these **[Ans. : d]**

Q.16 If a system descriptor has an access rights byte equal to 82H. What type of descriptor does it represent ?

[a] LDT descriptor [b] Call gate descriptor
[c] Task gate descriptor [d] Trap gate descriptor **[Ans. : a]**

Q.17 If a system descriptor has an access rights byte equal to 82H. What is its privilege level ?

[a] 0 [b] 1 [c] 2 [d] 3 **[Ans. : a]**

Q.18 The DPL = 2 and CPL = 0. What should be the privilege level of RPL so that data access will take place ?

[a] 0 [b] 1 [c] 2 [d] All of these **[Ans. : d]**

Q.19 The CPL = 0 and RPL = 1. What should be the privilege level of DPL to get data access ?

[a] 0 [b] 1 [c] 2 [d] 1 or 2 **[Ans. : d]**

Q.20 _____ gate allows to access the segment which has higher privilege level.

[a] Trap [b] Task [c] Call [d] None of these **[Ans. : c]**

Q.21 _____ code segment has no inherent privilege level of its own.

[a] Trap [b] Task [c] Call [d] Conforming **[Ans. : d]**

Q.22 If the segment is _____ it can be accessed from lower privilege level.

[a] code segment [b] conforming code segment
[c] data segment [d] stack segment **[Ans. : b]**

Q.23 The DPL of the conforming descriptor must always be _____ the current CPL for valid access.

[a] less than [b] less than or equal to
[c] greater than [d] greater than or equal to **[Ans. : b]**

Q.24 _____ descriptor do not define any memory space.

[a] Call gate [b] Data segment
[c] Code segment [d] Stack segment **[Ans. : a]**

Q.25 _____ descriptor do not have base address and limit fields.

[a] Call gate [b] Data segment
[c] Code segment [d] Stack segment **[Ans. : a]**

Q.26 _____ acts as an interface layer between code segments at different privilege levles.

[a] Call gate [b] Trap gate [c] Task gate [d] All of these **[Ans. : a]**

Q.27 _____ gate defines the code segment and the exact offset where the control is to be transferred.

[a] Call gate [b] Trap gate [c] Task gate [d] All of these **[Ans. : a]**

Q.28 Call gate descriptors are put in _____.

[a] GDT [b] LDT
[c] GDT or LDT [d] none of these **[Ans. : c]**

Q.29 _____ field decides the number of passing parameters to the new stack.

[a] DPL [b] Type [c] P [d] Word count **[Ans. : d]**

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Q.30 Page level protection involves two kinds of protections : _____.

[a] Restriction of addressble domain
[b] Type checking
[c] Both a and b
[d] None of these

[Ans. : c]

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Unit - III

6 Multitasking

Multitasking

Q.1 Which of the following is/are used to support multitasking ?

[a] TSS
[b] TR
[c] Task gate descriptor
[d] All of these

[Ans. : d]

Q.2 _____ can cause task switches.

[a] Interrupts
[b] Exceptions
[c] a and b
[d] None of these

[Ans. : c]

Q.3 To have an isolated tasks which of the following statement(s) is/are true ? Each task can have _____.

[a] seperate LDT and page directory
[b] different logical to linear mapping
[c] different linear to physical mapping
[d] all of these

[Ans. : d]

Q.4 The task environment (context) is stored in _____.

[a] TSS descriptor
[b] TSS
[c] TR
[d] none of these

[Ans. : b]

Q.5 TSS is not accessible to _____.

[a] user program
[b] program at PL0
[c] a and b
[d] none of these

[Ans. : c]

Q.6 Which of the following is/are the fields of dynamic set of TSS ?

[a] General purpose registers
[b] Segment registers
[c] Instruction pointers
[d] All of these

[Ans. : d]

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Q.7 Which of the following is/are the fields of dynamic set of TSS ?

[a] Flag register [b] Back link
[c] Instruction pointer [d] All of these **[Ans. : d]**

Q.8 Saving _____ during task switch guarantees that the task can be restarted at the point at which it was stopped.

[a] EFLAGS [b] segment registers
[c] EIP [d] general purpose registors
[Ans. : c]

Q.9 _____ is used by the 80386 to keep track of a previous task.

[a] EFLAGS [b] EIP [c] Back link [d] None of these
[Ans. : c]

Q.10 Which of the following is/are the field(s) of static set of TSS ?

[a] Selector of the task's LDT [b] PDBR register
[c] T-bit [d] All of these **[Ans. : d]**

Q.11 Which of the following is/are the field(s) of static set of TSS ?

[a] I/O map offset [b] Pointers to the stacks
[c] PDBR register [d] All of these **[Ans. : d]**

Q.12 TSS descriptor must appear in the _____.

[a] LDT [b] GDT [c] a or b [d] None of these
[Ans. : b]

Q.13 Privilege level of the stack segment must be _____ the privilege level of the code segment.

[a] same [b] greater than
[c] less than [d] greater than or equal to
[Ans. : a]

Q.14 Fields ESP0, ESP1, ESP2, SS0, SS1 and SS2 of TSS hold the _____ for privilege levels 0, 1 and 2.

DPL ≤ CPL

[a] stack selectors [b] stack sequence pointers
[c] both a and b [d] none of these **[Ans. : c]**

Q.15 _____ field in TSS holds the 16-bit offset of the beginning of the I/O permission bit map.

[a] Bit map offset [b] Back link
[c] CR3 [d] EIP **[Ans. : a]**

Q.16 The B-bit = 1 in the type field of TSS descriptor indicates _____.

[a] operand is byte [b] operand is 16-bit
[c] operand is 32-bit [d] task is busy **[Ans. : d]**

Q.17 The 80386 requires minimum _____ bytes of storage in order to perform a context save.

[a] 80 [b] 104 [c] 128 [d] 256 **[Ans. : b]**

Q.18 What is the size of task state segment ?

[a] 80 [b] 104 [c] 128 [d] 256 **[Ans. : b]**

Q.19 The maximum limit for TSS is _____.

[a] 64 kbytes [b] 1 Mbytes [c] 4 Gbytes [d] 64 Terabytes
[Ans. : c]

Q.20 _____ specifies the currently executing task by pointing to the TSS.

[a] TP [b] TR [c] TSSD [d] None of these
[Ans. : b]

Q.21 The invisible portion of the task register holds _____.

[a] base [b] limit [c] a and b [d] none of these
[Ans. : c]

Q.22 Several programs can be executed simultaneously because of _____.

[a] page protection [b] segment protection
[c] multitasking [d] segmentation **[Ans. : c]**

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Q.23 Program control switches from one task to the another task after a fixed interval of time in case of _____.

a time-share systems b frequency shared systems
c both (a) and (b) d none of these [Ans. : a]

Q.24 With the help of task management data structures 80386 can switch from one _____ to another.

a interrupt b procedure
c task d stack [Ans. : c]

Q.25 _____ may cause task switches.

a Interrupts b Exceptions
c Both (a) and (b) d None of these [Ans. : c]

Q.26 Each task have_____ mapping.

a logical to linear b linear to physical
c sequential d both (a) and (b) [Ans. : d]

Q.27 Each task can have _____.

a different logic to linear mapping
b linear to physical mapping
c separate LDT and page directory
d all of these [Ans. : d]

Q.28 80386 invokes the task _____.

a directly b indirectly
c both (a) and (b) d none of these [Ans. : c]

Q.29 _____ is used by the 80386 to keep a track of previous task.

a Return b Back link c Stack d None of these
[Ans. : b]

Q.30 In task state segment the field "T" is used for _____.

a enabling task switch trap b disabling task switch trap
c both (a) and (b) d none of these [Ans. : c]

RPL, CPL ≤ DPL D..

Task Switching

EIP →
TSS – GDT
CALL – GDT, LDT

Q.31 Processor selects a task gate descriptor only when the maximum of selector's _____ and the _____ of the procedure is numerically less than or equal to the _____ of the descriptor.

a DPL, RPL, CPL b CPL, DPL, RPL
c RPL, CPL, DPL d CPL, RPL, DPL [Ans. : c]

Q.32 When task gate is used, the _____ of the target TSS descriptor is not used for privilege checking.

a RPL b CPL c a and b d DPL [Ans. : d]

Q.33 Which of the following statement(s) is/are true ?

a Task switches cannot be recursive
b Tasks are not re-entrant.
c Currently running task is always a busy task.
d All of these. [Ans. : d]

Q.34 Which of the following case(s) 80386 does the task switch ?

a A long jump or call instruction contains a selector which refers to a TSS descriptor.
b Selector in a long jump or call instruction refer to a task gate.
c Interrupt selector refers to a task gate.
d All of these. [Ans. : d]

Q.35 Which of the following check(s) is/are performed during task switching without task gate ?

a Priviledge check b Limit check
c Present check d All of these [Ans. : d]

Q.36 In the indirect method, task switching is done by _____ a task gate.

a jumping to b calling
c a or b d none of these [Ans. : c]

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Q.37 When _____ is used for task switch, the DPL of the new TSS descriptor is not used for privilage checking.

[a] trap gate [b] call gate [c] task gate [d] none of these

[Ans. : c]

Q.38 When task gate is used, the _____of the task gate is compared with the _____ and _____ of the gate selector ?

[a] DPL, CPL, RPL [b] CPL, DPL, RPL

[c] RPL, CPL, DPL [d] none of these [Ans. : a]

Q.39 Which field of selector is used to identify descriptor table ?

[a] Index [b] TI [c] RP [d] All of these

[Ans. : b]

Nested Tasks

Q.40 _____ instruction doesn't nest the task.

[a] JMP [b] CALL [c] RET [d] All of these

[Ans. : a]

Q.41 The _____ bit shows that current task is child task.

[a] G [b] TS [c] B [d] NT [Ans. : d]

I/O Protection

Q.42 Which of the following is /are the I/O sensitive instructions ?

[a] INS [b] OUTS [c] IN [d] All of these

[Ans. : d]

Q.43 Which of the following is/are the sensitive instruction (s) ?

[a] INS [b] OUT [c] CLI [d] All of these

[Ans. : d]

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Unit - IV

7 Input-Output

Q.1 Input/output to be performed in 80386 can be done by ?

[a] Separate I/O address space

[b] Memory-mapped I/O

[c] Both a and b

[d] None of the above

[Ans. : c]

Q.2 Input/output ports in 80386 can be used for how many external devices ?

[a] 32 external devices [b] 16 external devices

[c] 8 external devices [d] 64 external devices [Ans. : b]

Q.3 How does the program specify the address of the port ?

[a] Using an immediate byte constant

[b] Using a value in DX

[c] Both a and b

[d] None of the above

[Ans. : c]

Q.4 What is the use of IN instruction ?

[a] Move data from a register to a port in the I/O address space

[b] Move data between two registers

[c] Move data from a port in the I/O address space to a register

[d] Both a and c

[Ans. : c]

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Q.5 What is the use of OUT instruction ?

a Move data from a register to a port in the I/O address space
b Move data between two registers
c Move data from a port in the I/O address space to a register
d Both a and c

[Ans. : a]

Q.6 Which instructions are used to move strings of data between the memory address space and ports in the I/O address space ?

a IN and OUT
b INS and OUTS
c Both a and b
d None of the above

[Ans. : b]

Q.7 Which of the following provides maximum flexibility ?

a Separate I/O address space
b Memory-mapped I/O
c Both a and b
d None of the above

[Ans. : b]

Q.8 Which instructions are used to manipulate bits in the internal registers ?

a AND
b OR
c TEST
d All of the above

[Ans. : d]

Q.9 Memory-mapped I/O is subject to access protection and control while executing in which mode ?

a Real Mode
b Protected Mode
c Virtual Mode
d Controlled Mode

[Ans. : b]

Q.10 Classes of I/O instruction are :

a Register I/O Instructions
b String I/O instructions
c Both a and b
d None of the above

[Ans. : c]

Q.11 Class of I/O instruction which transfer strings of items (strings of bytes, words, or doublewords) located in memory is known as ?

a Block I/O instructions
b String I/O instructions
c Both a and b
d Register I/O Instructions

[Ans. : c]

Q.12 Which instructions are included in Register I/O Instructions ?

a IN and OUT
b INS and OUTS
c Both a and b
d None of the above

[Ans. : a]

Q.13 Which instructions are included in Block I/O Instructions ?

a IN and OUT
b INS and OUTS
c Both a and b
d None of the above

[Ans. : b]

Q.14 What mechanisms are used for protecting I/O ports in protected mode of 80386 ?

a IOPL field in EFLAG
b I/O permission bit map in TSS segment
c Both a and b
d None of the above

[Ans. : c]

Q.15 Which exception is caused if the I/O privilege is violated ?

a Divide by 0
b General protection exception
c NMI Interrupt
d Double Exception

[Ans. : b]

Q.16 Which instructions are called as 'sensitive instructions' ?

a IN and OUT
b INS and OUTS
c CLI and STI
d All of the above

[Ans. : d]

Q.17 Each task has _____ .

a Copy of flag register
b IOPL

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c Both a and b d None of the above [Ans. : c]

Q.18 Procedure executing at which privilege level can change IOPL?

a Privilege level 0 b Privilege level 1
c Privilege level 2 d Privilege level 3 [Ans. : a]

Q.19 The I/O permission bit map is a ?

a Bit vector b Array c Integer d Class [Ans. : a]

Q.20 Size of the bit map is ?

a 32 bit b 16 bit c Variable d 8 bit [Ans. : c]

Q.21 To access I/O port the corresponding bit in the I/O bitmap must be ?

a 1 b 0
c Can be 0 or 1 d Marked Invalid [Ans. : b]

Q.22 How many privileged instructions supported by 80386 ?

a 19 b 20 c 16 d 32 [Ans. : a]

Q.23 Privileged instructions are those that affect _____ .

a segmentation and protection mechanism
b alter the interrupt flag
c perform peripheral I/O.
d all of the above [Ans. : d]

Q.24 In order to execute the privilege instructions, the CPL of a procedure or task must be _____ than the number represented by the IOPL bits.

a same or a lower b same
c same or a greater d greater [Ans. : a]

Q.25 The instructions that affect the system data structures must be executed when CPL is ?

a 3 b 2 c 1 d 0 [Ans. : d]

Q.26 What is the function of CLTS ?

a Controls LDTR bit of task segment
b Controls logical bit of task segment
c Clears task-switched flag
d Controls registers of task segment [Ans. : c]

Q.27 What are the sources for External Interrupts ?

a Maskable interrupts (INTR)
b Nonmaskable interrupt (NMI)
c Both a and b
d None of the above [Ans. : c]

Q.28 What are the Processor detected exceptions ?

a Faults b Traps c Aborts d All of the above
[Ans. : d]

Q.29 Which instructions can trigger software interrupts ?

a INT0, INT 3, BOUND b IN, OUT
c INS,OUTS d All of the above [Ans. : a]

Q.30 Faults are exceptions that are reported _____ the instruction causing the exception.

a before b during c after d Either a or b
[Ans. : d]

Q.31 What happens if fault is detected during the instruction ?

a It continues its execution
b That instruction is skipped and the processor executes next instruction

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[c] The fault is reported with the machine restored to a state that permits the instruction to be restarted

[d] None of the above [Ans. : c]

Q.32 In what case 'Aborts' are used ?

[a] Hardware errors

[b] Inconsistent values in system tables

[c] Illegal values in system tables

[d] All of the above [Ans. : d]

Q.33 Traps are exceptions that are reported _____ the instruction causing the exception.

[a] before [b] during [c] after [d] Either a or b

[Ans. : c]

Q.34 Which is INT 3 ?

[a] Debug exceptions [b] Breakpoint

[c] Overflow [d] Bounds check [Ans. : b]

Q.35 While an NMI handler is executing, the processor ignores further interrupt signals at the NMI pin until which instruction is executed ?

[a] INT 0 [b] IRET [c] RET [d] INT 21H

[Ans. : b]

Q.36 If If = 0, INTR interrupts are :

[a] Inhibited [b] Enabled [c] Serviced [d] Handled

[Ans. : a]

Q.37 Which instructions alter the setting of IF ?

[a] STI [b] CLI [c] Both a and b [d] FLAG

[Ans. : c]

Q.38 The IF controls the acceptance of external interrupts signaled via which pin ?

[a] INTR [b] INT [c] NMI [d] All of the above

[Ans. : a]

Q.39 The processor clears IF in response to which signal(s) ?

[a] STI [b] CLI [c] RESET [d] Both b and c

[Ans. : d]

Q.40 Which bit in EFLAG controls the recognition of debug faults ?

[a] TF [b] IF [c] RF [d] AF [Ans. : c]

Q.41 Which interrupts have lowest priority ?

[a] NMI interrupt

[b] INTR interrupt

[c] Faults except debug faults

[d] Debug traps [Ans. : b]

Q.42 Interrupt descriptors are stored in a special descriptor table called ?

[a] IDTR [b] LDTR [c] GDTR [d] IVT [Ans. : a]

Q.43 Where is IDTR located ?

[a] Location 0H [b] Fixed location

[c] Anywhere in memory [d] None of the above [Ans. : c]

Q.44 What are the types of descriptors which can be used in the IDT ?

[a] Trap gate descriptor [b] Interrupt gate descriptor

[c] Task gate descriptor [d] All of the above [Ans. : d]

Q.45 An interrupt gate or trap gate points indirectly to _____ .

[a] procedure

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b general purpose register
c first instruction in the executing program
d previous instruction in the executing program [Ans. : a]

Q.46 What does the offset field of the gate point to ?

a Base address of the interrupt descriptor
b Beginning of the interrupt or exception handling procedure
c First instruction in the executing program
d Previous instruction in the executing program [Ans. : b]

Q.47 What is the difference between the trap gate and interrupt gate ?

a No change in flag register in case of trap gate
b No change in flag register in case of interrupt gate
c No change in general purpose registers in case of interrupt gate
d No change in general purpose registers in case of trap gate [Ans. : a]

Q.48 The 80386 uses an IDT to store how many entries of interrupt descriptors ?

a 256 b 128 c 512 d 32 [Ans. : a]

Q.49 What is the base address and limit of IVT in real mode of 80386 ?

a Base 0 and limit of 03FFH
b Base 0 and limit of 0400H
c Base 40H and limit of 0400H
d Base 0 and limit of 0256H [Ans. : a]

Q.50 Which instruction is used to exit from an interrupt procedure ?

a RET b IRET c INT d RESET [Ans. : b]

Q.51 Which registers are reloaded by IRET instruction ?

a CS b EIP
c All of the above d None of the above [Ans. : c]

Q.52 What is invoked by interrupts or exceptions instead of CALL instructions ?

a ISR b CALL c IRET d RET [Ans. : a]

Q.53 ISR terminate with _____ instruction.

a ISR b IRET c CALL d RET [Ans. : b]

Q.54 The _____ field of a trap, task or interrupt gate determines the minimum privilege level required to pass through the gate.

a DPL b CPL c IOPL d GPL [Ans. : a]

Q.55 The _____ must be equal or higher privileged than the gate's _____.

a DPL,CPL b CPL,DPL c IOPL,CPL d GPL,DPL [Ans. : b]

Q.56 The task activated is determined by which selector ?

a ITS b TSG c TSS d DPL [Ans. : c]

Q.57 The new task generated by exception will have its NT (nested task) bit _____ in EFLAGs.

a invalid b ignored c clear d set [Ans. : d]

Q.58 In case of task gate, exception handler can run at _____ privilege level.

a only 0 b only 3
c only 2 d none of the above [Ans. : d]

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Q.59 Task gate has _____ LDT.

a same as that of previous running code
b separate
c does not have LDT
d none of the above

[Ans. : b]

Q.60 Time required is more to perform task switch in case of _____.

a task gate
b interrupt gate
c both a and b
d none of the above

[Ans. : a]

Q.61 INDEX field in error code is used for_____.

a uniquely identifies a descriptor depending on the status of the I and TI bits
b uniquely identifies a descriptor depending on the status of the EX and TI bits
c uniquely identifies a descriptor depending on the status of the EX and I bits.
d none of the above

[Ans. : a]

Q.62 Which interrupt is triggered when the quotient from either a DIV or IDIV instruction is too large to fit in the result register ?

a Interrupt 0
b Interrupt 1
c Interrupt 2
d Interrupt 3

[Ans. : a]

Q.63 Debug exception is caused by _____.

a instruction address breakpoint fault
b data address breakpoint trap
c single-step trap
d all of the above

[Ans. : d]

Q.64 Which interrupt cannot be disabled by any software ?

a Interrupt 0
b Interrupt 1

c Interrupt 2
d Interrupt 3

[Ans. : c]

Q.65 NMI interrupt is activated by _____ on 80386/486/Pentium NMI input pin ?

a low to high transition
b high to low transition
c constant high
d constant low

[Ans. : a]

Q.66 The type 3 interrupt is used to implement _____ function in the system.

a DEBUG
b BREAK POINT
c OVERFLOW
d UNDERFLOW

[Ans. : b]

Q.67 The breakpoint interrupt is produced by execution of which instruction ?

a INT 0
b INT 1
c INT 2
d INT 3

[Ans. : d]

Q.68 If the overflow flag is set, the 80386/486/Pentium will trigger a type 4 interrupt after executing the _____ instruction.

a INT 0
b INTO
c INT 2
d INT 3

[Ans. : b]

Q.69 Interrupt 5 is caused if the processor notices that the operand has crossed the limits specified by the previously executed _____ instruction.

a OVERFLOW
b BOUND
c UNBOUND
d DIV

[Ans. : b]

Q.70 Which interrupt is caused when an invalid opcode is detected by the execution unit ?

a Interrupt 4
b Interrupt 5
c Interrupt 6
d Interrupt 7

[Ans. : c]

Q.71 Interrupt 7 can occur at which instructions ?

a ESC
b WAIT
c Both a and b
d None of the above

[Ans. : c]

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Q.72 Which interrupt is caused when two exceptions cannot be handled serially ?

[a] Overflow [b] Double Fault
[c] Both a and b [d] Breakpoint **[Ans. : b]**

Q.73 Which interrupt is reserved by Intel ?

[a] Interrupt 9 [b] Interrupt 10
[c] Interrupt 11 [d] Interrupt 12 **[Ans. : a]**

Q.74 What is interrupt 10 ?

[a] Segment Not Present [b] Invalid TSS
[c] Stack Exception [d] Reserved by Intel **[Ans. : b]**

Q.75 What is pushed into stack to help identify the cause of the fault when interrupt 10 occurs ?

[a] Interrupt number [b] Invalid TSS
[c] Program name [d] Error code **[Ans. : d]**

Q.76 Which interrupt occurs when the processor detects that the present bit of a descriptor is zero ?

[a] Interrupt 9 [b] Interrupt 10
[c] Interrupt 11 [d] Interrupt 12 **[Ans. : c]**

Q.77 Which instructions can caused stack exceptions ?

[a] ENTER [b] LEAVE [c] PUSH [d] All of the above
[Ans. : d]

Q.78 General Protection Exception is caused due to_____.

[a] exceeding segment limit when using CS, DS, ES, FS or GS
[b] transferring control to a segment that is not executable
[c] switching to a busy task
[d] all of the above **[Ans. : d]**

Q.79 Page Fault exception occurs when paging is _____.

[a] enabled [b] disabled
[c] invalid [d] none of the above **[Ans. : a]**

Q.80 Which exception is caused when the processor detects a signal from the 80287 or 80387 on the 80386/486/Pentium's ERROR input pin ?

[a] Interrupt 13 [b] Interrupt 14
[c] Interrupt 15 [d] Interrupt 16 **[Ans. : d]**

Privileged and I/O Sensitive Instructions

Q.81 Which of the following is/are IOPL sensitive instruction(s) ?

[a] CLI [b] STI [c] IN [d] All of these
[Ans. : d]

Q.82 _____ field in the EFLAG register defines the right to use I/O related instructions.

[a] NT [b] VM [c] IOPL [d] None of these
[Ans. : c]

Special Protection Mode Instructions

Q.83 Which of the following is/are special protected mode instructions ?

[a] SGDT [b] SIDT [c] LGDT [d] All of these
[Ans. : d]

Q.84 Which of the following is/are special protected mode instruction(s) ?

[a] LTR [b] LLDT [c] ARPL [d] All of these
[Ans. : d]

Q.85 Which of the following is/are privilege instruction(s) ?

[a] LGDT [b] LIDT [c] LLDT [d] All of these
[Ans. : d]

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