

[5152]-569

S.E. (Computer) (Semester - IV)
MICROPROCESSOR
(2015 Pattern)

Time : 2 Hours]

[Maximum Marks : 50]

Instructions to the candidates:

- 1) Answer Question No.1 or 2, 3 or 4, 5 or 6 and 7 or 8.
- 2) Neat diagram must be drawn wherever necessary.
- 3) Figures to the right indicate full marks.
- 4) Assume suitable data, if necessary.

Q1) a) What is the use of following instructions? [2]

- i) Wait
 - ii) Lock
- b) Explain segment address translation in detail. [4]
- c) Draw and explain segment descriptor. [6]

OR

Q2) a) What is the use of Direction Flag? [2]

- b) Draw and explain the system address and system segment registers. [4]
- c) Explain the following instructions, mention flags affected: [6]
 - i) CWD
 - ii) BT
 - iii) LAHF

Q3) a) List the registers and data structures that are used in multitasking. [2]

- b) Differentiate between memory mapped I/O and I/O mapped I/O. [4]
- c) Explain what happens when an interrupt calls a procedure as an interrupt handler. [6]

OR

Q4) a) Write the two mechanisms that provide protection for I/O functions. [2]

P.T.O

- b) What is IDT and how to locate IDT? [4]
- c) Explain the different exception conditions-Faults, Traps and Aborts. [6]
- 27.251.173.154 24/05/2017 09:34:03 CEGPUL15721 SERVER36*
- Q5)** a) Write short note on "Task Switch Breakpoint". [3]
- b) Write short note on "Protection within a V86 task". [4]
- c) Explain various debugging features of 80386. [6]
- OR
- 27.251.173.154 24/05/2017 09:34:03 CEGPUL15721 SERVER36*
- Q6)** a) Write short note on "General Detect Fault". [3]
- b) Which bit of EFLAGS indicates V86 mode? Explain, how hardware and software cooperate with each other to emulate V86 mode? [4]
- c) Explain, how test registers are used in testing TLB? [6]
- 27.251.173.154 24/05/2017 09:34:03 CEGPUL15721 SERVER36*
- Q7)** a) Explain following signals [3]
i) ADS#
ii) READY#
iii) NA#
- b) Write note on CLK2 and internal processor clock. [4]
- c) Which data types are supported by 80387? [6]
- 27.251.173.154 24/05/2017 09:34:03 CEGPUL15721 SERVER36*

OR

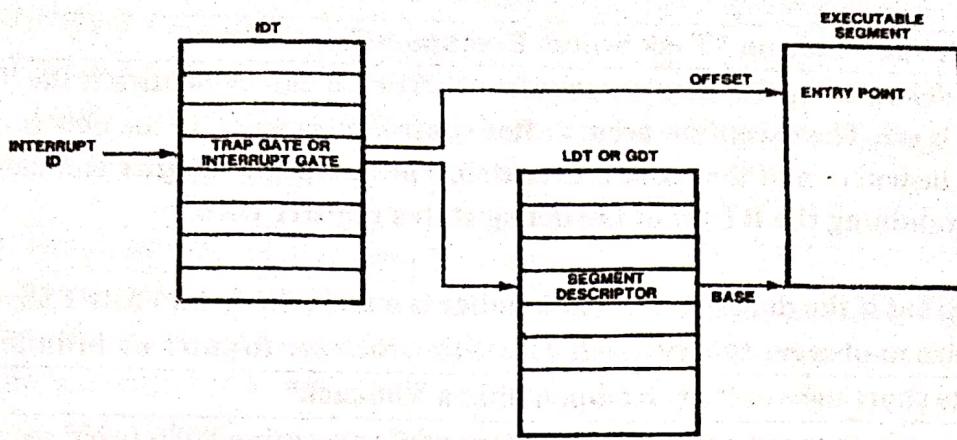
- Q8) a) Explain following signals [3]
BE0# through BE3#.
- b) Explain following signals [4]
- i) PEREQ
 - ii) BUSY#
 - iii) ERROR#
- c) Draw read cycle with pipelined address timing [6]

**SE Computer 2015 course
Microprocessor(2015)(210253)**

Solution

Q1)	a)	What is the use of following instructions?	[02]
		(i) Wait (ii) Lock	
Answer		(i) WAIT — Wait until Coprocessor not Busy (ii) LOCK — Assert Bus-Lock Signal	
	b)	Explain segment address translation in detail	[04]
Answer		Diagram 2 marks and explanation 2 marks	
		Explanation of each block expected	
	c)	Draw and explain segment descriptor	[06]
Answer		Diagram 3 marks and explanation 3 marks	
		OR	
Q2)	a)	What is the use of Direction Flag?	[02]
Answer		The value in the direction flag (DF) determines whether the processor automatically increments ESI or EDI (DF=0) or whether it automatically decrements these registers (DF=1).	
	b)	Draw and explain the system address and system segment registers.	[04]
Answer		Diagram 2 marks and explanation 2 marks	

	<p style="text-align: center;">32-BIT LINEAR BASE ADDRESS</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 10%;">47</td><td style="width: 45%; text-align: center;">16 15</td><td style="width: 45%; text-align: center;">0</td></tr> <tr> <td>GDTR</td><td></td><td></td></tr> <tr> <td>IDTR</td><td></td><td></td></tr> </table> <p style="text-align: center;">SYSTEM SEGMENT REGISTERS</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 10%;">15</td><td style="width: 45%; text-align: center;">0</td><td style="width: 45%;"></td></tr> <tr> <td>TR</td><td>SELECTOR</td><td></td></tr> <tr> <td>LDTR</td><td>SELECTOR</td><td></td></tr> </table>	47	16 15	0	GDTR			IDTR			15	0		TR	SELECTOR		LDTR	SELECTOR		
47	16 15	0																		
GDTR																				
IDTR																				
15	0																			
TR	SELECTOR																			
LDTR	SELECTOR																			
c)	Explain the following instructions, mention flags affected: (i) CWD (ii) BT (iii) LAHF	[06]																		
Answer	<p>2 marks each</p> <p>CWD: Convert Word to Doubleword, no flags affected</p> <p>BT: Bit test: affects CF</p> <p>LAHF: LAHF transfers the low byte of the flags word to AH.</p>																			
Q3) a)	List the registers and data structures that are used in multitasking.	[02]																		
Answer	<ul style="list-style-type: none"> • Task state segment • Task state segment descriptor • Task register • Task gate descriptor 																			
b)	Differentiate between memory mapped I/O and I/O mapped I/O.	[04]																		
Answer	<p>Minimum 4 points of comparison</p> <p>I/O Mapped I/O: The I/O address space consists of 216 (64K) individually addressable 8-bit ports; any two consecutive 8-bit ports can be treated as a 16-bit port; and four consecutive 8-bit ports can be treated as a 32-bit port. I/O Specific instructions can be used e.g. IN, OUT etc.</p> <p>Memory Mapped I/O: I/O devices also may be placed in the 80386 memory address space. Any instruction that references memory may be used to access an I/O port located in the memory space. For example, the MOV instruction.</p>																			
c)	Explain what happens when an interrupt calls a procedure as an interrupt handler.	[06]																		
Answer	Diagram 2 marks and explanation 4 marks																			



1. Stack of interrupt procedure
2. Flags usage by interrupt procedure
3. Returning from an interrupt procedure
4. Protection in interrupt procedures

OR

Q4)	a)	Write the two mechanisms that provide protection for I/O functions.	[02]
------------	-----------	---	------

Answer

Two mechanisms provide protection for I/O functions:

1. The IOPL field in the EFLAGS register defines the right to use I/O-related instructions.
2. The I/O permission bit map of a 80386 TSS segment defines the right to use ports in the I/O address space.

b)

What is IDT and how to locate IDT?

[04]

Answer

IDT: Interrupt Descriptor Table

IDTR: Interrupt Descriptor Table Register

With diagram and explanation 2 marks each

c)

Explain the different exception conditions – Faults, Traps and Aborts.

[06]

Answer

Exceptions are classified as faults, traps, or aborts depending on the way they are reported and whether restart of the instruction that caused the exception is supported.

Faults

Faults are exceptions that are reported "before" the instruction causing the exception. Faults are either detected before the instruction begins to execute, or during execution of the instruction. If detected during the instruction, the fault is reported with the machine restored to a state that permits the instruction to be restarted.

Traps

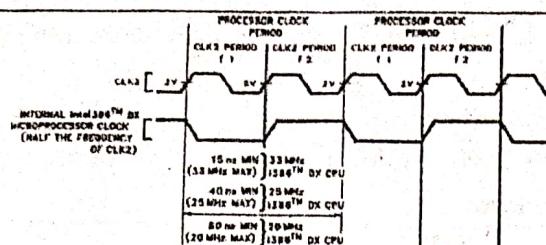
A trap is an exception that is reported at the instruction boundary immediately after the instruction in which the exception was detected.

Aborts

An abort is an exception that permits neither precise location of the instruction causing the exception nor restart of the program that caused the exception. Aborts are used to report severe errors, such as hardware errors and inconsistent or illegal values in system tables.

Q5)	a)	Write short note on "Task Switch Breakpoint".	[03]
Answer		The debug exception also occurs after a switch to an 80386 task if the T-bit of the new TSS is set. The exception occurs after control has passed to the new task, but before the first instruction of that task is executed. The exception handler can detect this condition by examining the BT bit of the debug status register DR6. Note that if the debug exception handler is a task, the T-bit of its TSS should not be set. Failure to observe this rule will cause the processor to enter an infinite loop.	
	b)	Write short note on "Protection within a V86 task".	[04]
Answer		Because it does not refer to descriptors while executing 8086 programs, the processor also does not utilize the protection mechanisms offered by descriptors. To protect the systems software that runs in a V86 task from the 8086 program, software designers may follow either of these approaches: <ul style="list-style-type: none"> • Reserve the first megabyte (plus 64 kilobytes) of each task's linear address space for the 8086 program. An 8086 task cannot generate addresses outside this range. • Use the U/S bit of page-table entries to protect the virtual-machine monitor and other systems software in each virtual 8086 task's space. When the processor is in V86 mode, CPL is 3. Therefore, an 8086 program has only user privileges. If the pages of the virtual-machine monitor have supervisor privilege, they cannot be accessed by the 8086 program. 	
	c)	Explain various debugging features of 80386.	[06]
Answer		<p>The features of the 80386 architecture that support debugging include:</p> <p><i>Reserved debug interrupt vector:</i> Permits processor to automatically invoke a debugger task or procedure when an event occurs that is of interest to the debugger.</p> <p><i>Four debug address registers:</i> Permit programmers to specify up to four addresses that the CPU will automatically monitor.</p> <p><i>Debug control register:</i> Allows programmers to selectively enable various debug conditions associated with the four debug addresses.</p> <p><i>Debug status register:</i> Helps debugger identify condition that caused debug exception.</p> <p><i>Trap bit of TSS (T-bit):</i> Permits monitoring of task switches.</p> <p><i>Resume flag (RF) of flags register:</i> Allows an instruction to be restarted after a debug exception without immediately causing another debug exception due to the same condition.</p> <p><i>Single-step flag (TF):</i> Allows complete monitoring of program flow by specifying whether the CPU should cause a debug exception with the execution of every instruction.</p> <p><i>Breakpoint instruction:</i></p>	

		Permits debugger intervention at any point III program execution and aids debugging of debugger programs. <i>Reserved interrupt vector for breakpoint exception:</i> Permits processor to automatically invoke a handler task or procedure upon encountering a breakpoint instruction.
		OR
Q6)	a)	Write short note on "General Detect Fault". [03]
Answer		This exception occurs when an attempt is made to use the debug registers at the same time that ICE-386 is using them. This additional protection feature is provided to guarantee that ICE-386 can have full control over the debug-register resources when required. ICE-386 uses the debug-registers; therefore, a software debugger that also uses these registers cannot run while ICE-386 is in use. The exception handler can detect this condition by examining the BD bit of DR6.
	b)	Which bit of EFLAGS indicates V86 mode? Explain, how hardware and software cooperate with each other to emulate V86 mode? [04]
Answer		<p>The processor executes in V86 mode when the VM (virtual machine) bit in the EFLAGS register is set.</p> <p>The emulation of an 8086 is the result of cooperation between hardware and software:</p> <ul style="list-style-type: none"> • The hardware provides a virtual set of registers (via the TSS), a virtual memory space (The first megabyte of the linear address space of the task), and directly executes all instructions that deal with these registers and with this address space. • The software controls the external interfaces of the virtual machine (I/O, interrupts, and exceptions) in a manner consistent with the larger environment in which it executes. <p>In the case of I/O, software can choose either to emulate I/O instructions or to let the hardware execute them directly without software intervention.</p>
	c)	Explain, how test registers are used in testing TLB? [06]
Answer		<p>Diagram 3 and explanation 3</p>
Q7)	a)	Explain following signals i. ADS# ii. READY# iii. NA# [03]
Answer		1 mark each
	b)	Write note on CLK2 and internal processor clock. [04]
Answer		Diagram 2 marks and explanation 2 marks



c) Which data types are supported by 80387?

[06]

Answer

Data Formats	Range	Precision	Most Significant Byte								HIGHEST ADDRESSED BYTE							
			7	0	7	0	7	0	7	0	7	0	7	0	7	0	7	0
Word Integer	10^4	16 Bits																
Short Integer	10^8	32 Bits																
Long Integer	10^{16}	64 Bits																
Packed BCD	10^{16}	18 Digits	6	X	d ₁₅	d ₁₄	d ₁₃	d ₁₂	d ₁₁	d ₁₀	d ₉	d ₈	d ₇	d ₆	d ₅	d ₄	d ₃	
Single Precision	10^{-38}	24 Bits	5	BIASED EXPONENT	SIGNIFICAND	71	23	14	0									
Double Precision	10^{-308}	53 Bits	5	BIASED EXPONENT	SIGNIFICAND	43	52	14	0									
Extended Precision	10^{-4932}	64 Bits	5	BIASED EXPONENT	1	64	63	1	0									

OR

Q8) a) Explain following signals i. BE0# through BE3#.

[03]

Answer 3 marks for correct answer or partial depending on answer.

b) Explain following signals

[04]

i. PEREQ

ii. BUSY#

iii. ERROR#

Answer 1 mark each and if all are correct 4

c) Draw read cycle with pipelined address timing.

[06]

Answer

