Comparison between 8086, 80386 and Intel i7 processor

Sr. No	Parameter	8086	80386	Intel i7
1.	**Year of Introduction**	1978	1985	2008
2.	**Data Bus**	16 bit	32 bit	64 bit
3.	**Address Bus**	20 bit	32 bit	32/64 bit
4.	**Physical Memory**	1 MB	4 GB	64 GB
5.	**Register Size**	16 bit	32 bit	64 bit
6.	**Voltage Required**	5 V	5 V	1.4 V
7.	**Clock Type**	1x	2x	Above 2x
8.	**Pins in Architecture**	40	132	1366
9.	**Pipelining** (Increases throughput by executing multiple instructions at a same time)	Yes	Yes	Yes
10.	**Instruction Set**	117 Instructions	129 Instructions	8086+80386+SIMD instructions
11.	**Front Side Bus**	16 bit	32 bit	Intel QPI
12.	**On chip Cache Memory**	NA	NA	**L1**: 32KB instruction cache +32 KB data cache **L2**: 256 KB for each core **L3**: 8 MB shared by all four cores
13.	**On chip FPU**	NA	NA	Yes
14.	**Hyper Threading Support** (Each core execute different threads)	NO	NO	Yes

15.	**Multiprocessor Support**	NO	NO	Yes
16.	**Overclocking Feature**	NO	NO	Yes
17.	**Branch Predication**	Not Supported	Not Supported	Supported
18.	**Instruction Cache**	6 Bytes	16 Bytes	18 Bytes
19.	**RAM**	NA	NA	DDR3
20.	**Operating Modes**	1. Maximum Mode 2. Minimum Mode	1. Real Mode 2. Protected Mode 3. Virtual Mode	1. Compatibility Mode 2. 64 Bit Mode
21.	**General Purpose Registers**	4 (16 bit)	8 (32 bit)	16 (64 bit)
22.	**Segment Registers**	4 (16 bit)	6 (16 bit)	6 (16 bit)
23.	**Flag Registers**	16 bit	32 bit (Eflag)	64 bit (Rflag)
24.	**Stack Pointer**	16 bit	32 bit	64 bit
25.	**Control Register**	NA	32 bit	64 bit
26.	**Debug Register**	NA	32 bit	64 bit
27.	**FPU Register**	NA	NA	**Data** : 8 (80 bit) **Status** : 16 bits **Control** : 16 bits **Opcode**: 11 bits **Instruction Pointer**: 64 bit **Data Pointer**: 64 bit **Tag Register**: 16 bit
28.	**Descriptor Registers**	NA	**GDTR**: 48 bits **IDTR**: 48 bits **LDTR**: 16 bits **TR**: 16 bits **Selector**: 16 bits **Limit**: 16 bits **Base**: 32 bits	**GDTR**: 80 bits **IDTR**: 80 bits **LDTR**: 16 bits **TR**: 16 bits **Selector**: 16 bits **Limit**: 32 bits **Base**: 64 bits

29.	**MMX Registers** (Used for SIMD instructions)	NA	NA	**MMX**: 8 (64 bit) **XMM**: 16 (128 bit) **MXCSR**: (32 bit)
30.	**Special Features**		1. Memory Management 2. Virtual Addressing 3. Segmentation and Paging 4. Protection Mechanism 5. Multitasking	1. Smart Cache 2. Virtualization Technology 3. Turbo Boost Technology 4. Quick Path Interconnect