Total No. of Questions—8] [Total No. of Printed Pages—2

Seat No.	

[5459]-193

S.E. (Comp. Engg.) (II Sem.) EXAMINATION, 2018

MICROPROCESSOR

(2015 PATTERN)

Time : 2 Hours **Maximum Marks : 50**

N.B. :— (*i*) Attempt Q. No. **1** *or* Q. No. **2**, Q. No. **3** *or* Q. No. **4**, Q. No. **5** *or* Q. No. **6** and Q. No. **7** *or* Q. No. **8**.

(*ii*) Neat diagrams must be drawn wherever necessary.

(*iii*) Figures to the right indicate full marks.

(*iv*) Assume suitable data, if necessary.

1. (*a*) With the help of neat diagram explain how logical address is converted into physical address ? Assume paging mechanism is disabled. [6]

(*b*) Explain any *three* control transfer instructions of 80386. [6]

Or

2. (*a*) Explain how linear address is converted into physical address by 80386 memory management. [6]

(*b*) What is the use of the following instructions in 80386 ? Mention which flags gets effected with each instruction : [6]

ADC, DIV, CMP

3. (*a*) With the help of suitable diagram, explain how call gate descriptor is used to change the privilege levels in protected mode ? [6]

(*b*) Explain the procedure of handling interrupts in protected mode. [6]

P.T.O.

Or

4. (*a*) What is the role of TSS in multitasking ? Explain I/O permission bitmap in TSS. [6]

(*b*) Draw the format of interrupt gate and trap gate descriptor. What is the difference between them ? [6]

5. (*a*) What is the role of DR0 to DR3 registers in debugging ? Explain task switch breakpoint. [4]

(*b*) What are content of CR0 register after RESET in 80386 ? Explain all related bits. [3]

(*c*) Explain linear address formation in virtual mode of 80386. [6]

Or

6. (*a*) Explain any *four* debugging features of 80386. [4]

(*b*) List any *three* differences between Virtual 86 mode and 8086. [3]

(*c*) With the help of neat diagram explain format of DR6 register. [6]

7. (*a*) Compare Pipelined and Non-pipelined bus cycle. [2]

(*b*) Explain the following signals of 80386 : [6]
M/IO#, W/R#, READY#

(*c*) Explain the following instructions of 80387 : [5]
FLD, FSQRT, FLDZ, FBSTP

Or

8. (*a*) Explain any *two* instructions used in 80387 to pop data from its stack registers. [2]

(*b*) With the help of neat diagram, explain the pipelined read bus cycle. [6]

(*c*) When WAIT state is required in 80386 read bus cycle ? Explain with neat diagram. [5]

Q. 1 **a) Logical address to physical address Translation (Paging Disabled)**

Diagram for segmentation address translation – 2M

Explanation – 4M

i) Logical address contain selector and offset address.

ii) Segment selector select one of the descriptor present in GDT/LDT.

iii) Selected segment descriptor will contain base address of target segment. This base address is added in offset address to generate lin address.

iv) The physical address will be same as above linear address as paging disabled.

b) For each instruction **2M. (2 *3 = 6M)**

Instructions are – CALL, JMP, RET, IRET

OR

Q.2 **a) Conversion of Linear address into physical address.**

Diagram for paging address translation - **2M**

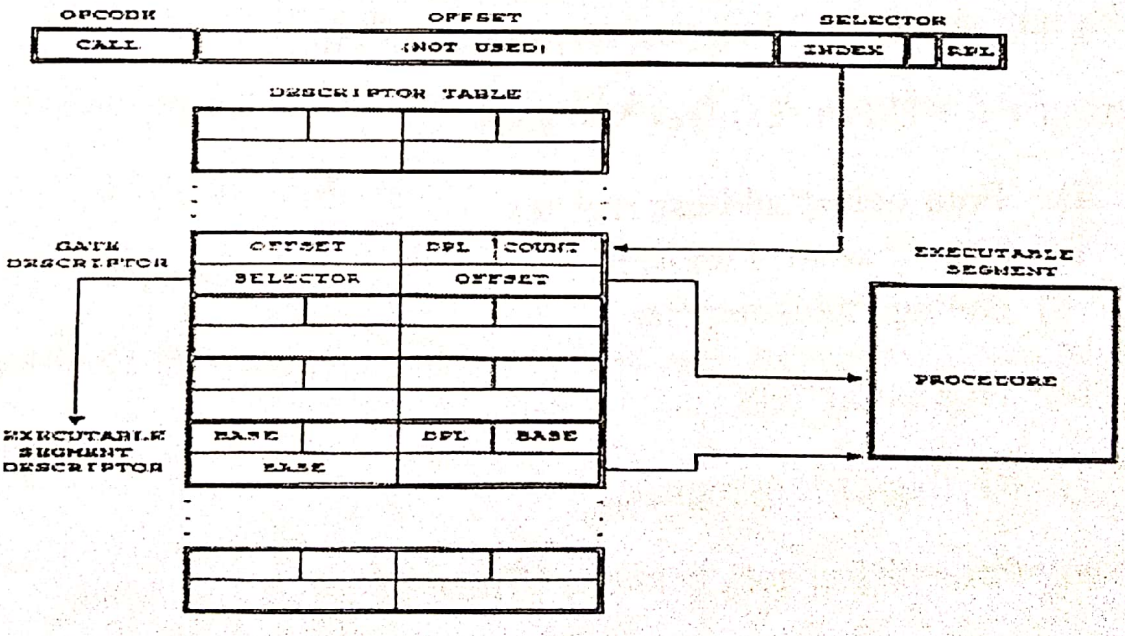
Explanation – 4M

b) For each instruction **2M. (Explanation-** 1M and Flags affected- 1M)

(2*3 = 6M)

Q.3 **a) Diagram – 2M, Explanation- 4M**

Working of CALL gate descriptor:



b) Procedure of handling interrupts in Protected mode (6M)

i) When interrupt occurs execution of current instruction is completed.

ii) One of the descriptor present in IDT is selected.

iii) Using selected descriptor control is transferred to ISR.

iv) After execution of IRET instruction in ISR control is transferred back to interrupted program.

OR

Q.4 a) Role of TSS in multitasking -2M

I/O permission bitmap – 4M

b) **Draw format of interrupt gate and trap gate descriptor**

Format of interrupt gate descriptor- 2M

Format of trap gate descriptor- 2M

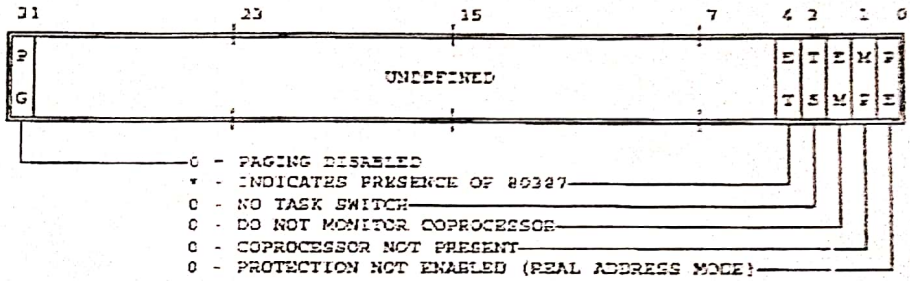
Difference – 2M

Q.5 a) What is role of DR0 to DR3 registers in debugging? Explain task switch breakpoint.

Role of DR0 to DR3 – 1M

Task switch breakpoint- 3M

b) What are content of CR0 register after RESET in 80386? Explain all related bits. 3M



c) Linear address formation in virtual mode of 80386- 6M

OR

Q.6 a)) Explain any four debugging features of 80386.

One feature for 1M (**4 features *1= 4M**)

i) Four debug address register
ii) Debug control register
iii) Debug status register
iv) Trap bit of TSS
v) RF flag of flag register

b) List any three differences between Virtual 86 mode and 8086.

One difference for **1M (3*1=3M)**

c) With the help of neat diagram explain format of DR6 register.

Format of DR6 register – 2M

Explanation- 4M

Q.7 a) Comparison between pipeline and nonpipelined bus cycle

One point for **1M (2 Points *1=2M)**

i) Address of next bus cycle appears on address bus when previous bus cycle is under process.

ii) NA# signal

b) Explanation of each signal - **2M (3 Signals *2 = 6M)**

i) M/IO#

ii) W/R#

iii) READY#

c) Instructions of 80387.

FLD (1M)

FSQRT (1M)

FLDZ (1M)

FBSTP (2M)

OR

Q.8 a) Explain any two instructions used in 80387 to pop data from its stack registers.

One instruction – 1M (2 instructions *1M=2M)

Example Instructions are FST, FSTP, FBSTP

b) Explain pipelined read bus cycle with the help of neat diagram.

Diagram – **3M**

Explanation- **3M**

(c) When WAIT state is required in 80386 read bus cycle? Explain with neat diagram.

Diagram **-2M**

Explanation- **3M**

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