Total No. of Questions—8] [Total No. of Printed Pages—3

Seat No.	

[5152]-564

S.E. (Computer) (I Sem.) EXAMINATION, 2017

COMPUTER ORGANIZATION AND ARCHITECTURE

(2015 PATTERN)

Time : Two Hours **Maximum Marks : 50**

N.B. :— (*i*) Neat diagrams must be drawn wherever necessary.

(*ii*) Figures to the right indicate full marks.

(*iii*) Use of calculator is allowed.

(*iv*) Assume suitable data, if necessary.

1. (*a*) Multiply the following using Booth' algorithm [6]

Multiplicand = +11

Multiplier = –6.

(*b*) Explain in brief seven RAID levels. [6]

Or

2. (*a*) Show the general structure of IAS Computer and explain. [6]

(*b*) Draw and explain the flowchart of restoring division algorithm. [6]

P.T.O.

3. (*a*) What is the use of DMA ? Explain cycle stealing in DMA. [6]

(*b*) Explain the following addressing modes with one example each : [6]

(*i*) Immediate

(*ii*) Register Indirect

(*iii*) Direct Addressing

Or

4. (*a*) Differentiate between programmed I/O and interrupt driven I/O. [6]

(*b*) What is machine instruction ? Explain types of instructions. [6]

5. (*a*) What are various hazards in instruction pipelining ? Explain. [7]

(*b*) Write a short note on superscalar execution and superscalar implementation. [6]

Or

6. (*a*) Explain the instruction cycle in detail. [6]

(*b*) List and explain various ways in which an instruction pipeline can deal with conditional branch instructions. [7]

7. (*a*) Compare horizontal and vertical microinstruction format. [6]

(*b*) Explain in detail microinstruction sequencing organization. [7]

Or

8. (*a*) Compare Hardwired control over micro-programmed control. [6]

(*b*) Write a control sequence for the following instruction for single bus organization : ADD (R3), R1. [7]

Marking Scheme

Q.1 a) Answer = -66 [6]
Each cycle = 1 ½ Mark
1 ½ * 4 = 6 Marks

b) [6]
1 Level = 1 Marks
1*6 = 6 Marks

OR

Q.2 a) structure of IAS Computer = 2 Marks [6]
explanation of MAR, MBR,IBR, IR, PC,AC & MQ = 4 Marks

b) Flowchart = 4 Marks [6]
Explanation = 2 Marks

Q.3 a) use of DMA = 2 Marks [6]
Explanation of cycle stealing in DMA = 4 Marks

b) [6]
i) Immediate 2 Marks = Explanation = 1 + Example 1
(ii) Register Indirect 2 Marks = Explanation = 1 + Example 1
(iii) Direct Addressing 2 Marks = Explanation = 1 + Example 1

OR

Q.4 a) Each point of Differentiation = 2 Marks [6]
2*3=6 Marks

b) machine instruction Definition =1 Marks [6]
Types of instructions = 5 Marks (Explanation with examples of each type)
Data Processing = 1 Marks
Data storage = 1 Marks
Data Movement =1 Marks
Control = 2 Marks

Q.5 a) Data Hazards =3 Marks [7]
Resource Hazard =2 Marks
Control Hazards =2 Marks

b) Explanation of superscalar execution = 3 Marks [6]
Explanation of superscalar implementation = 3 Marks

OR

Q.6 a) State Diagram = 3 Marks [6]
Explanation = 3 Marks

P.T.O

b) Listing = 2 Marks [7]
Explanation of following point =1 Marks each

- Multiple Streams
- Prefetch branch target
- Loop Buffer
- Branch prediction
- Delayed branch

Q.7 a) Each point of comparison = 2 Marks [6]
2*3=6 Marks

b) micro instruction sequencing Diagram = 3 Marks [7]
Explanation = 4 Marks

OR

Q. 8 a) Each point of comparison = 2 Marks [6]
2*3=6 Marks.

b) Instruction fetch = 2 Marks [7]
Operand Fetch= 2 Marks
Execution of instruction steps= 3 Marks

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