1. Segmentation unit allows segments of _____ size at maximum.
a) 4 Gbytes
b) 6 Mbytes
c) 4 Mbytes
d) 6 Gbytes
ANS: a)

2. If _____input pin of 80386 if activated, allows address pipelining during 80386 bus cycles.

a) BS16
b) NA
c) PEREQ
d) ADS
ANS: b)

3. Virtual Mode Flag bit can be set using ____ instruction or any task switch operation only in the _____ mode

a) IRET, Virtual
b) POPF, Real
c) IRET, protected
d) POPF, protected
ANS: c)

4. The interrupt vector table of 80386 has been allocated _____ space starting from _____ to _____.

a) 1Kbyte, 00000H, 003FFH
b) 2Kbyte, 10000H, 004FFH
c) 3Kbyte, 01000H, 007FFH
d) 4Kbyte, 01000H, 009FFH
ANS: a)

5. The ___ bit decides whether it is a system descriptor or code/data segment descriptor

a) P
b) S
c) D
d) G
ANS: b)

6. 80386 support which type of descriptor table from the following?

a) TDS
b) ADS
c) GDT
d) MDS
ANS: c)

7. 80386 support overall ___ addressing modes to facilitate efficient execution of higher level language programs.

a) 9

b) 10
c) 11
d) 12
ANS: a)

8. If the bus cycle indication code M/IO# D/C# W/R# EQUALS 010, what type of bus cycle is taking place?
a) I/O read bus cycle
b) I/O write bus cycle
c) Memory read bus cycle
d) Memory write bus cycle

ANS: a)

9.Which processor structure is pipelined?
a)all x80 processors
b) all x85 processors
c) all x86 processors
ANS: c)

10.In 8086 microprocessor one of the following statements is not true.
a)Coprocessor is interfaced in MAX mode
b)Coprocessor is interfaced in MIN mode
c)I/O can be interfaced in MAX / MIN mode
d)Supports pipelining
ANS: b)

11.Who invented the microprocessor?
a)Marcian E Huff
b)Herman H Goldstein
c)Joseph Jacquard
d)none of above
ANS:a)

12.When the RET instruction at the end of subroutine is executed,
a) the information where the stack is iniatialized is transferred to thestack pointer
b) the memory address of the RET instruction is transferred to the program counter
c) two data bytes stored in the top two locations of the stack are transferred to the program counter
d) two data bytes stored in the top two locations of the stack aretransferred to the stack pointer
ANS: c)

13.I n a microprocessor, the service routine for a certain interrupt starts from a fixed location of memory which cannot be externally set, but the interrupt can be delayed or rejected. Such aninterrupt is
a) non-maskable and non-vectored

b) maskable and non-vectored
c) non-maskable and vectored
d) maskable and vectored
ANS: d)

14. What does microprocessor speed depends on
a) Clock
b) Data bus width
c) Address bus width
d) Size of register
ANS: c)

15. The necessary steps carried out to perform the operation of accessing either memory or I/O Device, constitute a _____

a) fetch operation

b) execute operation

c) machine cycle

d) instruction cycle
ANS: c)

16. An interrupt instruction

a) causes an unconditional transfer of control
b) causes a conditional transfer of control
c) modifies the status register
d) is an I/O instruction
ANS:a)

17. Programs are written in assembly language because they

a) run faster than High-level language
b) are portable
c) easier to write than machine code programs
d) they allow the programmer access to registers or instructions that are not usually provided by a High-level language

ANS: d)

18.In which microprocessor does the concept of pipeline first introduced?

a) 8086
b) 80286
c) 80386
d) 80486

ANS: c)

19.Which of the following is a math co-processor?

a) 8085
b) 8086
c) 8087
d) 8088

ANS:c)

20. The 80386DX can address up to ---------- virtual memory.
    a) 1 Terabytes
    b) 8 Terabytes
    c) 16 Terabytes
    d) 64 Terabytes

    ANS: d)

21. Active low ---------- signal indicates that the valid address is present on the address bus.
    a) D/C
    b) ADS
    c) LOCK
    d) BUSY
    ANS: b)

22. What is the status of W/R and M/IO signals to read data from memory?
    a) W/R= 0 and M/IO = 0
    b) W/R= 0 and M/IO = 1
    c) W/R= 1 and M/IO = 0
    d) W/R= 1 and M/IO = 1
    ANS: b)

23. After reset 80386 starts execution in ---------- mode.
    a) Real
    b) protected
    c) virtual 8086
    d) none of these
    ANS: a)

24. HOLD and HLDA signals are ---------- interface signals.
    a) Interrupt
    b) DMA
    c) coprocessor
    d) none of these.
    ANS: b)

25. BUSY, ERROR and PEREQ are interface signals.
    a) Interrupt
    b) DMA
    c) coprocessor
    d) none of these
    ANS: c)

26. If the TI = 0 then the selector indicates which table?
    a) GDT
    b) LDT
    c) IDT
    d) Both a) and b)

ANS: a)

27. Which unit translates logical address into linear address?
    a) Instruction decoder
    b) Paging
    c) Segmentation
    d) Control

ANS: c)

28. ---------- unit translate linear address into physical address.
    a) Segmentation
    b) Instruction decoder
    c) Instruction predecoder
    d) Paging

ANS: d)

29. The least significant 5 bits of the _____ are called MSW.
    a) CR0
    b) CR1
    c) CR2
    d) CR3

ANS: a)

30. The entire 1 MB memory space is divided into _____ segments.
    a) 32 KB
    b) 4 KB
    c) 64 KB
    d) 48 KB

ANS: c)

31. How many 64 KB segments can be active at a time in real mode
    a) 4
    b) 6
    c) 10
    d) 8

ANS: b)

32. For memory addressing in real mode only _____ and _____ can be used as index registers.
    a) SI,BI
    b) SI,DI
    c) DI,BI
    d) PI,SI

ANS: b)

33. GD is a _____ bit register
    a) 48
    b) 16
    c) 32
    d) none of above

ANS: a)

34. Segment registers CS,DS,SS and ES in real mode are 64 kilobytes. If effective address > 64KB then 80386 triggers exception
    a) INT 1
    b) INT 12
    c) INT13

d) INT 10

ANS: c)

35. 80386 can enter real mode if there is an active low on the _____ pin.

a) BUSY
b) HOLD
c) HALT
d) RESET

ANS: d)

36. It also enters real mode if PE bit of _____ register is clear.

a) CR 0
b) CR 1
c) CR2
d) CR 3

ANS: a)

37. The _____ is also called as "private table" which defines a local memory address space used by the task.

a) LDT
b) GDT
c) IDT
d) Both a and b

ANS: a)

38. The functions of memory management protection and multitasking become active only when 80386 is operating in _____ mode

a) real
b) Protected
c) Virtual
d) None of above

ANS: b)

39. The TR is a_____ bit registor

a)16
b)32
c)48
d)64

ANS: a)

40. The IDT and IBT are the same in real mode

a) true
b) false
c)
d)

ANS: a)

41. for memory addressing in real mode only _____ and _____ can be used as base registers.

a) BX,BP
b) BX,SP
c) SP,BP
d) IP,BP

ANS: a)

42. If DS=B000H and offset=5F00H then the physical address will be
    a) BF500H
    b) FB500H
    c) F0B50H
    d) B5H00H
ANS: d)

43. The segment descriptor in LDT are unique for each specific task
    a) true
    b) false
    c)
    d)
ANS: a)

44. LDT is a type _____ descriptor
    a) 0
    b) 2
    c) 4
    d) 3
ANS: b)

45. a TSS descriptor appears in
    a) GDT
    b) LDT
    c) IDT
    d) NONE
ANS: a)

46. LDT descriptor can be accessed if the privileged level is _____
    a) 0
    b) 1
    c) 2
    d) none
ANS: a)

47.IN ORDER TO ENABLE WE MUST INTIALISE _____ AND _____
    a) CR3 and CR0
    b) CR1 and CR0
    c) CR0 and CR1
    d) all of above
ANS: a)

48.The TSS decriptor defines the _____ segment.
    a) code
    b) data
    c) task state
    d) none
ANS:b)

49. In order to perform a context save operation the value of limit field should b>= 103
    a)true
    b)false
    c)
    d)
ANS: a)

50. If ET=0 _____ Processor is selected.

a) 80287
b) 80387
c) 8087
d) none of the above

ANS: a

51. For which of the following INT 13 is generated

a) A jump to data segment
b) Writing to a read only segment
c) Attempting to address a memory location with an offset address that exceeds the limit for the specified segment
d)All of the above

ANS: d)

52.If 80287 ERROR# pin detects an error then _____ interrupt is generated

a) INT 16
b) INT 17
c) INT 14
d) INT 8

ANS: a)

53. If a WAIT instruction is detected with both MP and TS bits of MSW set then exception is generated

a) Math Fault Exception
b) No math unit available
c) Page Fault Exception
d) INT 13

ANS: b)

54. Due to which of the following INT 10 is generated

a) Writing to a read only segment
b) A task state segment is too small
c) An illegal backlink in a TSS.
d) Both b and c.

ANS: d)

55. Which of the following is an undefined opcode exception?

a) INT 6
b) INT 8
c) INT 13
d) INT 12

ANS: a)

56. Which of the following instructions are sensitive IOPL whenever the 80386 is executing an 8086 virtual mode task.

a) CLI
b) RET
c) Both a and b
d) None of the above

ANS: c)

57. A call gate is Type _____ descriptor.

a) 3
b) 2

c) 4
d) 6

ANS: 4

58. Current task is permitted to switch to the new task only when _____
a) Task gate DPL <= max(CPL,RPL)
b) Task gate DPL >= max(CPL,RPL)
c) Both a and b
d) None of these

ANS: b)

59. _____ instruction doesn't nest the task.
a) JMP
b) CALL
c) RET
d) All of the above

ANS: a)

60. If DPL is ____ then privilege constraints prevent procedure from causing task switch.
a) 3
b) 0
c) 1
d) 2

ANS: b)

61. The internal processor clock signal is at _____ the frequency of external clock input signal
a) half
b) twice
c) one fourth
d) None of the above

ANS: a)

62. The _____ input signal is used to select a pipelined or non pipelined address
a) NA#
b) BS16#
c) BE3#
d) BE0#

ANS: a)

63. The clock speeds at which the 80386 processor can operate are
a) 16MHz
b) 25 MHz
c) 20 MHz
d) All of the above

ANS: d)

64. To extend the duration of the 80386's bus cycle it is necessary to insert _____
a) Idle states
b) T1 states
c) T2 states
d) Wait states

ANS: d)

65. _____ is active for shutdown condition.
a) BE1#

b) BE0#
c) BE2#
d) BE3#

ANS: b)

66. _____ is active for halt condition.
a) BE1#
b) BE0#
c) BE2#
d) BE3#

ANS: c)

67. _____ allows bus cycles to be overlapped.
a) Pipelining
b) Non Pipelining
c) Dynamic sizing
d) None of the above

ANS: a)

68. The _____ instruction is used to translate a byte from one code to another code.
a) MOV
b) XLAT
c) CALL
d) POP

ANS: b)

69. _____ instruction inhibits all interrupts, including NMI interrupt
a) POP AX
b) POP BX
c) POP SP
d) POP SS

ANS: d)

70. On DIV instruction on a word, quotient is stored in _____ accumulator
a) higher byte
b) lower byte
c) upper nibble
d) lower nibble

ANS: b)

71. For IDIV instruction _____ is implicit.
a) dividend
b) quotient
c) remainder
d) All of these

ANS: d)

72. The _____ instruction will convert signed bit in EAX to signed quadword in the EDX : EAX register.
a) CBW
b) CDQ
c) CWDE
d) CWD

ANS: c)

73. SLDT can only be executed in
    a) Protected mode
    b) Real mode
    c) Both a and b
    d) None of these
ANS: a)

74. _____ of the instruction following CALL is pushed onto the stack.
    a) Address
    b) Offset
    c) None of the above
    d)
ANS: b)

75. Virtual addressing does not support _____ addressing
    a) Scaled
    b) Indexed
    c) Segmented
    d) All of these
ANS: a)

76. BSF generates interrupt 13 if _____
    a) all encountered bits are 1
    b) any part of operand would lie outside 0 to 0FFFFH
    c) any part of operand would lie outside 1000 to FFFF0H
    d) None of the above.
ANS: b)

77. For IN instruction port address is stored in _____
    a) AX
    b) BX
    c) CX
    d) DX
ANS: d)

78. _____ flag is normally used to check for data transmission errors.
    a) Sign
    b) Zero
    c) Parity
    d) All of these
ANS: c)

79. _____ is called as the debug status register
    a) DR3
    b) DR2
    c) DR4
    d) DR6
ANS: D)

80. _____ is called as the data testing register of TLB
    a) TR0
    b) TR1
    c) TR3
    d) TR7
ANS: d)