Id	Keep it blank
Question	paging can be used in -------
A	Protected mode
B	real mode
C	virtual mode
D	both 1 and 3
Answer	D
Marks	1
Unit	Unit 2
Id	Keep it blank
Question	------- instruction is used to load gdt register
A	LGDT
B	IGDT
C	SGDT
D	RGDT
Answer	A
Marks	1
Unit	Unit 4
id	
QUESTION	Each entry in page directory table/ page table is of ---
A	64 bits
B	48 bits
C	32 bits
D	16 bits
Answer	C
Marks	1
Unit	4

id	
QUESTION	If Granularity bit G=1 and limit=00002h, maximum segment size is ……
A	4GB
B	4KB
C	8KB
D	8GB
Answer	C
Marks	2
Unit	2
id	
QUESTION	paging converts ------- address to ---------address
A	logical, physical
B	linear, physical
C	logical, linear
D	linear, logical
Answer	B
Marks	2
Unit	2
id	
QUESTION	Each entry in page directory table and page table contains base address of ---------- and ------ respectively
A	page frame, page directory
B	page directory, page table
C	page table , page frame
D	page frame, page table
Answer	C
Marks	2

Unit	2
id	
QUESTION	If current privilege level i.e. cpl=2 , an attempt to access data segment at level 2---------
A	access is granted
B	general protection fault exception will be generated
C	access is denied
D	none of the above
Answer	A
Marks	2
Unit	2
id	
QUESTION	To switch to protected mode ---- bit of----------register is to be set
A	PG,CR1
B	PG,CR0
C	PE,CR0
D	PE,CR3
Answer	C
Marks	2
Unit	1
id	
QUESTION	If dirty bit is set,it indicates.....
A	page (in main memory) has been modified
B	page (in main memory) has not been modified
C	page (in cache)has been modified
D	page (in cache) has not been modified
Answer	A
Marks	2
Unit	2

id	
QUESTION	..... is incorrect statement
A	TSS described by TSS descriptor does not contain data or code segment.
B	TSS contains state of the task and linkage so task can be nested.
C	TSS descriptor is addressed by task register TR.
D	TSS gate descriptor gives the base address of TSS.
Answer	D
Marks	2
Unit	2
id	
QUESTION	If TI bit of segment register is set, it selects.....
A	GDT
B	IDT
C	LDT
D	Both A and C
Answer	C
Marks	1
Unit	1
id	
QUESTION	..... is incorrect statement about privileged rule
A	For comforming segment: trasfer is allowed when CPL = DPL
B	When control is transferred to a conforming segment, the CPL must change.
C	For non-comforming segment: transfer is allowed when CPL >= DPL.
D	for call gate : transfer is allowed when CPL <= DPL of the call gate and DPL of the target code segment< = CPL
Answer	B
Marks	2

Unit	2
QUESTION	The CPL (Current Privilege Level) of the task or program must be------- IOPL in order for the task or program to access I/O ports.
A	> (greater than)
B	<= (less than or equal to)
C	>= (greater than or equal to)
D	<(less than)
Answer	B
Marks	2
Unit	2

QUESTION	following code
	mov bx,0001
	mov eax,FFFFFFFFh
	div bx
	generates

A	exception
B	syntax error
C	correct output
D	none
Answer	A
Marks	2
Unit	4
QUESTION	if p bit in descriptor is 0 generates .....exception
A	page fault
B	segment not present

C	general protection fault
D	invalid task state segment
Answer	B
Marks	1
unit	2
id	

QUESTION	following code
	mov esi,s1
	mov edi,s2
	mov cx,[strlen]
	cld
	repe cmpsb

A	compare two strings left to right as long as they are equal or cx is not equal to zero
B	compare two strings left to right as long as they are equal and cx is not equal to zero
C	compare two strings right to left as long as they are equal or cx is not equal to zero
D	compare two strings right to left as long as they are equal and cx is not equal to zero
Answer	B
Marks	2
Unit	4
id	
QUESTION	In 8086 ,If CS=EF3A and IP=000A which memory location being accessed ?
A	FE3A0

B	FE3B4
C	FE3AA
D	0000A
Answer	C
Marks	2
Unit	1
id	
QUESTION	In 8086 after reset execution starts from …….. Physical address
A	0FFFF
B	FFFFF
C	FFFF0
D	0FFFF
Answer	C
Marks	1
Unit	1
id	
QUESTION	IF bit in flag register controls……..
A	Maskable Interrupt

B	non maskable interrupt
C	Both a and b
D	None of the above
Answer	A
Marks	1
Unit	1
id	
QUESTION	----- is incorrect statement about procedure call
A	In near procedure call processor pushes only contents of Ip (eip) on to the stack.
B	In near procedure call processor pushes both contents of Ip (eip) and CS on to the stack.
C	In far procedure call processor pushes both contents of Ip (eip) and CS on to the stack.
D	In near procedure call processor does not pushes flag register on to the stack.
Answer	B
Marks	2
Unit	4
id	
QUESTION	----- is incorrect statement
A	Unconditional Jmp instruction allows near jump
B	Call instruction allows near jump

C	Conditional jmp instruction (e.g. jz/jnz) allows far jump
D	Unconditional Jmp instruction allows far jump
Answer	C
Marks	2
Unit	4
id	

id	
QUESTION	NA# pin is a……pin of 80386DX
A	Output
B	input
C	bidirectional
D	none
Answer	B
Marks	1
Unit	1
id	
QUESTION	80386DX reset address is…..
A	0XFFFFFFF0
B	0X0FFFFFF0
C	0X0FFFFFFF
D	0XFFFFFFFF
Answer	A
Marks	1
Unit	1
id	
QUESTION	During pipelined bus cycle to send the address of next bus cycle which of the following true.
A	Both BS16# and NA# signal must be asserted
B	Bs16# signal must be negated and NA# signal must be asserted
C	Only NA# signal must be asserted
D	Ready# signal must be negated and NA# signal must be asserted
Answer	B
Marks	2
Unit	3
id	
QUESTION	During non pipelined bus cycle for NA# signal to be sampled asserted which one of the must be true
A	Ready# signal must be negated

Format for MCQs.