UNIT 1

1. The first microprocessor with the PMOS microprocessor was
   a. Intel 4004 b. Intel 8008 c. Intel 80386 d. Intel 8086
2. 8086 microprocessor has
   a. 16 bit address bus b. 20 bit address bus c. 32 bit address bus d. 48 bit address bus
3. 8086 microprocessor has
   a.16 bit data bus b. 20 bit data bus c. 32 bit data bus d. 48 bit data bus

4. 8086 consists of registers named:

a. code segment register b. Stack segment register c. Data segment register d. all of these

5. The segment registers of 8086 are of:

a. 16 bits b.32 bits c. 48 bits d. 20 bits

6. There are active flags

a. 6 b. 9 c.12 d. 5

7.Setting which flag puts the processor into ingle step mode for debugging:

a. TF b. DF c. IF d. ZF

8. Which flag indicates the overflow from magnitude to the sign bit of result:

a. ZF b. DF c. SF d. OF

9.What is the part of memory from which BIU fetches the instruction code bytes

a. CS b. DI c. SI d. BP

10. What is the section of the memory which is reserved to store addresses & data while executing the subroutine program:

a. data b. Stack c. Code d. Segment

11. Features of the 80386 microprocessor:

a. multitasking support b. memory management c. Page translation d. All of the above

12.80386 can access:

a. 4 GB physical memory b.8 GB physical memory c. 12 GB physical memory d. 16 GB physical memory

13. 80386 is a

a. 32 bit processor b. 16 bit processor c. 12 bit processor d. 64 bit processor

14.Which signal ensures that the 80386 has uninterrupted control of bus system & shared resources.
a. READY b. LOCK c. Next address d. HOLD

15.A high on this pin indicates that DMA controller is requesting for bus cycle:

a. HOLD b. HLDA

16. What is the input used by wait instruction of a co processor:

a. BUSY b. Error

17. Which register holds the temporary result after an arithmetic & logical operation.

a. EBX b.EAX

18. Which register works as a random pointer for stack segment:

a. ESI b.EBP

19.Which register holds the source data for string instruction:

a. ESI b.EBP

20. Which address register points to the Task state table:

a.TR b. GDTR

21.Which address register points to the global descriptor table:

a. LDTR b. GDTR

22.Control registers are:

a. CR0 b.CR1 c.CR2 d. All of the above

23. It indicates that the area accessed by TLB entry is available:

a. W b. C

24.This bit is set by arithmetic instructions that generate a carry or borrow:

a. PF b. CF

25. This bit is set when one task invokes another task:

a. RF b. NT

UNIT 2:

1.The least significant 5 bits of the CR0 are called :

a. Machine status word b.PE bits

2. Total memory space of 80386 is:

a. 4 GB b. 1 GB

3. In real mode of the 80386 processor the linear addresses & the physical addresses are

a. same b. Different

4. What does the 80386 use to locate the base of vector table & to determine its length:

a. IDTR b. GDTR

5. In case of real mode , the interrupt vector table consists of:

a. 8 bytes b. 4 bytes

6. Which pair provides the address of the first instruction in the ISR:

a. CS:IP b. ES:DS

7.The effective CPL for executing programs in the real mode is always:

a. 0 b.1

8. If the offset is greater than FFFFH than which fault is generated:

a. interrupt fault b. Stack fault

9.Whenever the user wants to return to real mode without turning off the power, the user can simply reset:

a. PE bit b. PG bit

10.GDTR is a:

a. 48 bit register b. 16 bit register

11. LDTR is a:

a. 48 bit register b. 16 bit register

12. IDTR is a:

a. 48 bit register b. 16 bit register

13. The segment selectors point to a structure called:

a. segment descriptor b. Segment selector

14. Task register is :

a. 16 bit selector for TSS b. 32 bit selector for TSS

15.Which method divides the programs into different module such that each module will work independently:

a. paging b. Segmentation

16. What is used to index descriptor from table of descriptor:

a. descriptor b. Selector

17. Which bit is used to select one out of GDT or LDT:

a. Table indicator b. Null descriptor

18. Which are the non system descriptor:

a. code b. Data c. stack d. All of above

19. A selector which has index value zero & if it points to GDT then selector is:

a. NULL selector b. NULL descriptor

20. Which bit allows us to get segment larger than 1 MB:

a. PE bit b. Granularity bit

21. The TSS descriptor appears only in:

a. GDT b. LDT

22.Privilege level rule is:

a. MAX(RPL,CPL)<=TSS,DPL b.MAX(RPL,CPL)>=TSS,DPL

23.Paging cache can be cleared by clearing:

a. CR0 b. CR3

24.The I/O address space of 80386 in real mode is:

a. 64 TB b. 64 KB

25. Real mode is selected if :

a. PE=0 b. PE=1

UNIT 3:

1.The activity that is done by the microprocessor so that it can access data from memory is called as:

a. data cycle b. Bus cycle

2.Which input provides the fundamental timing in 80386:

a. CLK2 b.CLK1

3. The clock signal that is applied to the CLK2 input is how much times of the frequency rating of microprocessor:

a. thrice b. Twice

4. Which state indicates that no bus cycle is currently being processed:

a. T1 b. T2

5.Which is the process of fetching the next instruction when the present instruction is being executed.

a. segmentation b. pipelining

6. What indicates that the addressing for the next bus cycle needs to be given when the current bus cycle is in progress:

a. segmentation b. Pipelining

7.BE0(bar) is active for:

a. shut down b. Halt condition

8.BE2(bar) is active for:

a. shut down b. Halt condition

9. Which instruction puts the 80386 processor into halt state:

a. Halt b. Shut down

10.Which instruction occurs when double fault occurs and protection fault is being found:

a. halt b. Shut down

11.Which signal when asserted low indicates to the processor that the 80386 bus cycle is locked:

a. LOCK(bar) b. WAIT

12. Data transfer takes place from memory due to:

a. bus cycle b. Data cycle

13.How many CLK2 clocks do pipelining addressing method have:

a. 4 b. 5

14. The duration of the single idle state is equal to how many CLK2 cycles:

a. 2 b. 4

15.Which signal is used to select the physical data bus dynamically:

a. BS16(bar) b. LOCK

16. The bus enable signal is used to select the access of:

a. byte b. Word c. Double word d. All of these

17. The data transfer can be:

a. 8 bit b.16 bit c. 24 bit d. All of these

18.If in a single cycle the data transfer operation is completed then the data transfer is called as:

a. aligned data transfer b. Non aligned data transfer

19.If there are the overlaps at the double word boundary then the data transfers are called as:

a. aligned data transfer b. Non aligned data transfer

20. Which signal specifies the size of each bus cycle:

a. BS16(bar) b. PG

21.Cycle 1 is without any :

a. wait state b. lock state

22. How many wait state do cycle 2 have:

a. 2 b. 1

23.During the read bus cycle the data is transferred from external device to:

a. T1 state b. Processor

24.To extend the duration of 80386 bus cycle it is necessary to insert:

a. WAIT state b. LOCK state

25. Which signal do the ready signal return back:

a. READY(bar) b. LOCK

UNIT 4

1.Which instruction is used to extract string from word or double word :

a. XBIS b. XCHG

2.Which instruction is used to scan bbits in second word or the double word:

a. BSR b. CBW

3. Which instruction is a privileged instruction:

a. HLT b. XCHG

4. Which instruction converts signed byte in AL to signed byte in AX:

a. MSW b. CBW

5. Which instruction is used to set carry flag to zero:

a. CLD b. CLC

6. Which instruction transfers the data from port numbered by DX register to memory byte or word:

a. CBW b. INS

7. Which flags are affected due to IMUL instruction:

a. OF & CF b. OF & SF

8. Which interrupt occurs if second operator is a register:

a. 6 b. 13

9.Which instruction stores the MSW in two byte register:

a. SMSW b. SMW

10. Which instruction sets direction flag to zero:

a.STD b. AAA

11.Thw function WAIT is

a. wait until BUSY# pin is active b. Wait until BUSY# pin is inactive

12.For system call of print instruction value present in EBX register is:

a. 0 b. 1

13. .For system call of print instruction value present in EAX register is:

a. 1 b. 0

14.In system call to store length of the message which register is used:

a. EBX b.EDX

15. To accept single digit number the value stored in EAX register is:

a. 1 b. 3

16. To accept single digit number the value stored in EDX register is:

a. 2 b. 1

17.Which pair gives the address of the top stack:

a. CS:IP b. SS:SP

18.Which pair is used as a pointer in stack:
a. SS:BP b. DS:SI

19.Which pair is used as a destination pointer:

a. GS:DI b. FS:DI c. Both

20. Which pair is used as a general purpose pointer for copying & data processing:

a. ES:DI b. SS:BP

21.Which instruction is used to remove the word out of stack:

a. PUSH b. POP

22.Flags affected due to XCHG instruction:

a. No flags are affected b .OF

23. Which instruction allows interrupt service routines to be activated:

a. interrupt b. ADD

24. Which directive indicates the beginning of the data segment:

a. .CODE b. .DATA

25.Which directive helps the user to control the format of listing of an assembled program:

a. PAGE b .TITLE