1.	Feature of fetching the next instruction while current instruction is executing called
	a. Fetching b. Executing c. Pipelining d. Decoding
2.	flag of 8086 is used for BCD operations.
	a. ZF b. TFc. IFd. AF
3.	Which unit translates logical address into linear address?
	a. Paging b. Instruction Decode c. Segmentation d. Control
4.	80386DX supports simultaneously accessible
	a. Paging b. Instruction Decode c. Segmentation d. Control
5.	After reset 80386 starts execution of program from memory address
	a. FFFF FFFF H b. FFFF 0000 H c. FFFF FFF0 H d. 0000 0000 H
6.	control register gives page directory base address
	a. CR0 b. CR1 c. CR2 d. CR3
7.	control register gives page directory base address
	a. CR0 b. CR1 c. CR2 d. CR3
8.	In which mode 80386 DX maintains the compatibility of the object code with 8086 and 80286 ?
	a. Real b. Protected c. Virtual 8086 d. Min mode
9.	After every task switch, 80386 sets bit.
	a. T b. TF c. TS d. ET
10	. Page size in 80386 is
	a. 1 Kb b. 2 Kb c. 3 Kb d. 4Kb
11	. In 8086, the segment can start at any memory address which is divisible by
	a. 8 b. 16 c. 20 d. 24
12	allows to use separates memory area for program , data , and stack.
	a. Segmentation b. Pipelining c. Main memory d. MMU
13	For 8086 bus is bidirectional and bus is unidirectional

a. Address, data b. data, address c. Control, data d. Address, control
14. The ALU of 8086 is bits.
a. 8 b. 6 c. 20d. 24
15. The 8086 supports flags.
a. 5 b. 6 c. 8 d. 9
16 flags is used to hold privilege level
a. IOPL b. IPL c. IF d. NT
17. One common use of register is to reference parameters that were passed to subroutine way of stack.
a. SI b. DI c. SP d. BP
18 architecture of 80386 allows simultaneous instruction fetching , decoding, and execution of an instruction .
a. Pipelined b. Harvard c. Princeton d. Vonneumann
19. The 80386DX takes clocks for most instruction than 8086/8088.
a. More b. 10 more c. Fewer d. 16 more
20. Register EAX,EBX,ECX,and EDX are registers.
a. Scratch pad b. Pointers c. Index d. New
21. Physical address space of 80386 is and logical address space is
a. 4 GB, 64 TB b. 1MB, 64 MB c. 1 MB, 4GB d. 64 MB 1 GB
22. Length of double word is and quad word is
 a. 2 words, 4/3 words b. 2 words, 4 words c. 4 bits, 4 words d. 64 bits, 80 bits
23. The value in and are normally used as offsets from current value of SS.
a. ESP and EBP b. EIP and EBP c. ESI and EDI d. ESI and ESP
24. The flags which reflects the state of a particular program are known as and flags which reflects status of machine are known as flags.

a.	Status, sys	stem	b. system,	Status	c.	Status, Control	d.	Status, status control
25. The	width of ID	OTR is	bits	and TR is		bits .		
a.	48,16	b. 1	6,48 c.	48,24	d.	16,24		

MULTIPLE CHOICE QUESTIONS (MCQ's)unit -1

1. Which is first microprocessor?										
	(a)	8008	(b)	8085						
	(c)	8086	(d)	4004						
2.	The 8086 microprocessor is designed by									
	(a)	Intel	(b)	Motorola						
	(c)	General instruments	(d)	Zilog						
3.	Mici	roprocessor IC contains								
	(a)	Memory	(b)	input/output ports						
	(c)	CPU	(d)	all above						
4.	808	6 microprocessor is bit microprocessor.								
	(a)	8	(b)	16						
	(c)	24	(d)	32						
5.	The	8086 microprocessor has bit data bus.								
	(a)	8	(b)	24						
	(c)	16	(d)	32						
6.	The	8086 microprocessor has bit address bu	S.							
	(a)	32	(b)	20						
	(c)	16	(d)	8						
7.	The	8086 microprocessor can access upto of	f me	mory.						
	(a)	64 KB	(b)	1 KB						

	(C)	4 GB	(a)	T INIR						
8.	How many pins are present in 8086 microprocessor?									
	(a)	20 pins	(b)	30 pins						
	(c)	40 pins	(d)	64 pins						
9.	The 8086 microprocessor can support pipelining.									
	(a)	2 stage	(b)	3 stage						
	(c)	4 stage	(d)	5 stage						
10.	Wha	at are the operating modes of 8086?								
	(a)	minimum mode	(b)	maximum mode						
	(c)	both (a) and (b)	(d)	none of above						
11.		at is the size of registers in 8086 microprocess	or?							
	(a)	16-bit	(b)	8-bit						
	(c)	20-bit		24-bit						
12.		ch data types are supported by 8086 micropr	oces	ssor?						
	(a)	bit	(b)	byte						
	(c)	word	(d)	all above						
13.	Whi	ch data types are supported by 8086 micropr	oces	ssor?						
	(a)	double word	(b)	quad word						
	(c)	ten bytes	(d)	all above						
14.	<i>,</i>									
		size of data bus is 16-bit								
	(b)	size of registers is 16-bit								
	(c)	size of ALU is 16-bit								
	` '	all above								
15.		8086 microprocessor IC contains								
	(a)	CPU		memory						
		input/output ports	(d)	all above						
16.		at is the function of BIU?								
	(a)	Read data from memory or input port								
	(b)	Write data to memory or output port								
	(c)	Send address on address bus								
17.	(d)	All above	onre	occcor?						
17.	(a)	at is size of segments of memory in 8086 micr 1 KB	-	64 KB						
	(a) (c)	1 MB	٠,	variable						
18.		at is the function of segment registers?	(u)	variable						
10.	(a)	To store the starting address of corresponding	าฮ รศ	egment						
	(b)	To store data required for arithmetic or logic	_	_						
	(c)	To store address within the segment	0	p = 1 = 1 = 1 = 1						
	(d)	all above								
19.	What is the use of IP register?									
	(a)	To store the offset address of code segment								

(b) To store the offset address of data segment

- (c) To store the offset address of stack segment
- (d) To store the offset address of extra segment
- 20. What is the use of SI register?
 - (a) To store the offset address of code segment
 - (b) To store the offset address of data segment
 - (c) To store the offset address of extra segment
 - (d) To store the offset address of stack segment
- 21. What is the use of DI register?
 - (a) To store the offset address of code segment
 - (b) To store the offset address of data segment
 - (c) To store the offset address of extra segment
 - (d) Both (b) and (c)
- 22. What is the use of SP register?
 - (a) To store the offset address of code segment
 - (b) To store the offset address of data segment
 - (c) To store the offset address of stack segment
 - (d) To store the offset address of extra segment
- 23. What is the use of BP register?
 - (a) To store the offset address of stack segment
 - (b) To store the offset address of data segment
 - (c) To store the offset address of extra segment
 - (d) To store the offset address of code segment
- 24. What is the use of code segment (CS) register?
 - (a) To store the starting address of code segment
 - (b) To store the starting address of data segment
 - (c) To store the starting address of extra segment
 - (d) To store the starting address of stack segment
- 25. What is the use of DS register?
 - (a) To store the starting address of code segment
 - (b) To store the starting address of data segment
 - (c) To store the starting address of extra segment
 - (d) To store the starting address of stack segment
- 26. What is the use of ES register?
 - (a) To store the starting address of code segment
 - (b) To store the starting address of data segment
 - (c) To store the starting address of extra segment
 - (d) To store the starting address of stack segment
- 27. What is the use of SS register?
 - (a) To store the starting address of code segment
 - (b) To store the starting address of data segment
 - (c) To store the starting address of extra segment
 - (d) To store the starting address of stack segment
- 28. What is the size of CS, DS, ES and SS registers?

	(a)	16 bit	(b)	64 KB				
	(c)	20 bit	(d)	1 MB				
29.	What is the size of CS, DS, ES and SS segments?							
	(a)	16 bit	(b)	64 KB				
	(c)	20 bit	(d)	1 MB				
30.	The	content of CS, DS, ES or SS register is called a	s					
	(a)	offset address	(b)	logical address				
	(c)	linear address	(d)	physical address				
31.	The	content of IP, SP, BP, SI or DI register is called	l as .					
	(a)	offset address	(b)	logical address				
	(c)	linear address	(d)	physical address				
32.	Wha	at is the size of offset address?						
	(a)	8 bit	(b)	16 bit				
	(c)	20 bit	(d)	(b) or (c)				
33.	Wha	at is the size of logical address?						
	(a)	8 bit	(b)	16 bit				
	(c)	20 bit	(d)	24 bit				
34.	Wha	at is the size of physical address?						
	(a)	8 bit	(b)	16 bit				
	(c)	20 bit	(d)	24 bit				
35.	Wha	at is the size of instruction queue?						
	(a)	16 bit	(b)	20 bit				
	(c)	6 byte	(d)	64 KB				
36.	Whi	ich principal is used in queue?						
	(a)	First in Last Out	(b)	First in First Out				
	(c)	Last in First Out	(d)	None of above				
37.	Whi	ich block is not present in BIU?						
	(a)	Segment registers	(b)	Queue				
	(c)	IP	(d)	Decoder				
38.	Whi	ich block is not present in EU?						
	(a)	ALU	(b)	flag register				
	(c)	Control unit	(d)	IP				
39.	Wha	at is the use of AX register?						
	(a)	Input/Output operations						
	(b)	In multiply and arithmetic instructions						
	(c)	To store data						
	(d)	All above						
40.	What is the use of BX register?							
	(a)	To store the offset address of data segment						

	(b)	To store immediate data		
	(c)	To perform arithmetic or logical open	ration	
	(d)	All above		
41.	Wha	at is the use of CX register?		
	(a)	Input/Output operations		
	(b)	To store offset address of data segm	ent	
		To store counter value		
	(d)	In multiply and arithmetic operations	c	
12		at is the use of DX register?	,	
42.				
	(a)	Input/Output operations		
		To store counter value		
		To store offset address of data segm	ent	
	(d)	Both (a) and (c)		
43.	Wha	at is the size of flag register in 8086 m	icroprocess	or?
	(a)	8 bit	(b)	16 bit
	(c)	20 bit	(d)	24 bit
44.	How	many status flags are present in 808	6 microprod	cessor?
	(a)	3	(b)	6
	(c)	9	(d)	16
45.	Hov	v many control flags are present in 808	86 micropro	ocessor?
	(a)	3	(b)	
	(c)	9		16
46.	٠.	many unused flags are present in 80		
	(a)	3	(b)	
	(c)	9	(d)	7
47.	Wha	at is the use of decoding unit?		
	(a)	To find meaning of opcode		
	(b)	To generate control signals		
	(c)	Both (a) and (b)		
	(d)	None of above		
48.	Wha	at is the use of timing and control unit	?	
	(a)	To find meaning of opcode		
	(b)	To generate control and timing signa	ıl	
	(c)	To execute the instruction completel	ly	
	(d)	All of above		
49.		en carry flag is set?		
	(a)	If carry generated out of MSB	والعاماء عن	
	(b)	If carry generated out of D7 bit in 8 b		nn.
	(c) (d)	If carry generated out of D15 bit in 1 All of above	o bit additi(ות
50.	٠,	en parity flag is set?		
	(a)	If result contains even number of 1's		
	. ,			

 (c) If lower byte of result contains even number of 1's (d) If result contains odd number of 1's 51. When auxiliary flag is set? (a) If carry is generated out of MSB 										
51. When auxiliary flag is set? (a) If carry is generated out of MSB										
(a) If carry is generated out of MSB	· ,									
(b) If carry is generated out of D7 bit										
(c) If carry is generated out of D3 bit										
(d) If carry is generated out of D15 bit										
52. When overflow is set?										
(a) If carry is generated out of D6 bit in signed number operation										
(b) If carry is generated out of D7 bit in signed number operation										
(c) If carry is generated out of D14 bit in signed number operation										
(d) (a) or (c)										
53. What is the use of direction flag?										
(a) To auto increment SI and DI										
(b) To auto decrement SI and DI										
(c) To perform string operations										
(d) All of above										
54. What is the use of trap flag?										
(a) to debug the program										
(b) to execute one instruction at a time										
(c) to check registers or memory contents before complete execution	n									
(d) all of above										
55. What is the maximum value of segment registers?										
(a) FFFFH (b) FFFFOH										
(c) FF00H (d) F000H										
56. What is the maximum value of offset registers?										
(a) FFFFH (b) FFF0H										
(c) FF00H (d) F000H										
57. Why memory segments are of 64 KB size in 8086 microprocessor?										
(a) Size of offset register is 16 bit										
(b) Size of segment register is 16 bit										
(c) Size of all registers is 16 bit										
(d) All of above										
58. The total number of an non-overlapped segments are										
(a) unlimited (b) 16	_									
(c) 20 (d) cannot calculate59. In 8086 microprocessor, at a time how many segments an be active?	2									
59. In 8086 microprocessor, at a time how many segments an be active? (a) 2 (b) 3										
(a) 2 (c) 4 (d) 16										
60. In 8086 microprocessor, who converts logical address to physical addr	-ecc5									
(a) BIU (b) EU	CJJ:									
(0) 10										

	(c)	Both (a) and (b)	(d)	None of (a) and (b)							
61.	Whi	ch registers are used to generate physical add	dres	from logical address?							
	(a)	Segment registers	(b)	Offset register							
	(c)	Both (a) and (b)	(d)	General purpose register							
62.	If DS	S = 3000H, CS = 4000H and IP = 7A23H, then p	hysi	cal address is							
	(a)	47A34H	(b)	47A23H							
	(c)	AA230H	(d)	BA230H							
63.	If DS	S = 2000H, IP = 2000H and DI = 3000H, then p	hysid	cal address is							
	(a)	22000H	(b)	40000H							
	(c)	50000H	(d)	23000H							
64.	If ES	S = 5000H, IP = 2000H, SI = 1111H, DI = 2A32H	, the	en physical address is							
	(a)	52A32H	(b)	52000H							
	(c)	51111H	(d)	61110H							
65.	How	many pins are present in 8086 microprocess	or?								
	(a)	40	(b)	28							
	(c)	18	(d)								
66.		at is the duty cycle of clock in 8086 microproc									
	(a)	50%		25%							
	(c)	33%	(d)	100%							
67.	What is the use of S5 signal?										
	(a)	Always low									
		Represents status of interrupt flag (IF)									
	(c)	Reserved for further use									
CO		Indicates which segment is presently being u	ısed								
68.		= 1 and S3 = 1, then which segment is used?	/ I= \	Cada sassassas							
	(a)	Data segment		Code segment							
	(c) 	Stack segment	(u)	Extra segment							
69.	If BHE = 0 and A0 = 0, then data is accessed?										
	(a)	whole word									
	(b)	upper byte from/to odd address									
	(c)	lower byte from/to even address									
	(d)	none									
70.		dy signal is used to synchronisation of 8086 m		•							
	(a)	memory		input/output devices							
	(c)	8087 math coprocessor	(d)	both (a) and (b)							
71.	TES	$^-$ pin is used to synchronize the 8086 micropr	oces	sor and							
	(a)	memory	(b)	input/output devices							
	(c)	8087 math coprocessor	(d)	both (a) and (b)							
72.	If S2	$\frac{1}{2} = 0$, $S1 = 1$ and $S0 = 0$, then it indicates that .									
	(a)	read input/output port		code access							
	(c)	write input/output port	(d)	write to memory							

	73.	. If QS1 = 1 and QS0 = 0 then, it indicates that							
		(a)	no operation						
		(b)	first byte of opcode from queue						
		(c)							
		(d)	• • •						
	74.		er reset						
			SP = FFFFH	(b)	IP = 0000H				
		` '	CS = FFFFH	` '	all above				
	75.	` '	how many clock cycles logic 1 must be provide						
	, 5.	(a)		(b)	•				
			3	(d)					
76	DILL	• •	ds for	(u)	7				
70.			nterface unit	(h)	Base interface unit				
77	(c) A and B (d) None of these 7. EU stands for								
//.				71.3	E contra att				
			ution unit 	• •	Execute unit				
70			ange unit	(a)	None of these				
/8.			the part of architecture of 8086?	/I= \	The area with a result				
			bus interface unit		The execution unit				
70			(a) and (b)	(a)	None of these				
79.			re the four categories of registers?	/h\	Dointer or index registers				
			eral-purpose register		Pointer or index registers Other register				
		_	nent registers f these	(u)	Other register				
8 0			index register can be used for						
80.			metic operation	(h)	Multiplication operation				
			·		Multiplication operation				
01			raction operation	(u)	All of these				
			for	71.3	Laster of Control of Control				
			uction pointer		Instruction purpose				
0.3	(c) CS S		uction paints	(d)	None of these				
82.			e segment	(h)	Coot segment				
			segment		Counter segment				
83			d for:	(u)	Counter segment				
05.	_		segment	(h)	Direct segment				
			are segment		Divide segment				
84.			egment is not present in 8086?	(ω)	Divide segment				
0		CS (DS					
		SS (•	FS					
85.		-	s for						
			stry pointer	(b)	Instruction pointer				
			x pointer		None of these				
86.			as great importance in modular programming						
			k segment		Queue segment				
			y segment		All of these				
87.			egister contains the 8086/8088 flag?	-					

	(a)	Status register	(b)	Stack register
	(c)	Flag register	(d)	Stand reg
	88.	Which flag are used to record specific charac		_
		The stack	` ,	The stand
		The status	(d)	The queue
89.		at is the type of addresses?		
		Logical address		Physical address
00	` '	Both A and B	` '	None of these
90.		e address of a memory is a 20 bit address		
		Physical		Logical
		Both	(d)	None of these
91.		stands for		
		Deal inline package		Dual inline package
	(c)	Direct inline package	(d)	Digital inline package
92.	EA:	stands for		
	(a)	Effective address	(b)	Electrical address
	(c)	Effect address	(d)	None of these
93.	BP :	stands for		
	(a)	Bit pointer	(b)	Base pointer
	(c)	Bus pointer	(d)	Byte pointer
94.	DI s	stands for		
	(a)	Destination index	(b)	Defect index
	(c)	Definition index	(d)	Delete index
95.	SI s	tands for		
	(a)	Stand index	(b)	Source index
	(c)	Segment index	(d)	Simple index
96.	DS	stand for		
	(a)	Default segment	(b)	Defect segment
		Delete segment	` ,	Definition segment
97.		stands for	,	C
		Address latch enable	(b)	Address light enable
		Address lower enable		Address last enable
98.	٠,	stand for	(-)	
		Address data	(b)	Address delete
		Address date	` ,	Address deal
99	٠,	Il stands for	(4)	Tradices deal
<i>JJ</i> .		Non mask able interrupt	(h)	Non mistake interrupt
		Both		None of these
100	` '	AH stand for	(4)	None of these
100		Accumulator high	(b)	Address high
	(a)	•		
101	(c)	Appropriate high AL stands for	(u)	Application high
TOT			/b\	Addross low
	(a) (c)	Accumulator low Appropriate low	` '	Address low Application low
102		Which is/are the categorized of flag?	(α)	. Application low

-	a)		litional fla	ıg				Control fla					
(c)	Both	a and b				(d) None of these						
1	.03		is the m	nost impo	rtant seg	ment and	it contai	ns the act	ual assen	nbly langu	ıage instr	uction to be	
	executed by the microprocessor:												
(a)	Data	segment				(b)	Code segr	nent				
(c)	Stack	k segment				(d)	Extra segr	ment				
104.		The o	offset of a	particula	r segment	t varies fro	m ir	8086 mic	roprocess	or.			
(a)	000F	l to FFFH				(b)	0000H to	FFFFH				
•	c)		to FFH				` '	00000H to					
-	c,						(u)	000001110	,,,,,,,,,				
105.	۵١		stands fo in first otl				(b)	First in fir	ct out				
-	a)		in first ou										
	c)				ا بام مام مد	.h		None of t	nese				
106.				are used	to check	that a		Cinala bit					
•	a)		bit error					Single bit					
	c)		i bit error		all tha au	العدامات بدعدا		None of t		00400000	· m 2		
107.				msible for	all the ot	ıtside worl		nication b	y the micr	oprocesso	orr		
-	a)	BIU (· ·				PIU						
-	c)	TIU (· -	tha .	sian al		EU						
108.			•	thes	signai.		/b\	INTROLIN	DICUT				
-	a)		RUPT REC					INTRRUPT					
109.	c)				inc		(u)	INTRRUPT	KESET				
			t of RAM	sor contai	1115								
	a) b)		t of ROM										
-	c)		heral driv	iors									
	d)				arithmeti	ic logic fun	ctions of a	computer					
110.	uj			or is also o		_	Ctions or t	computer					
	a)	Chip	oprocesso)	iten cane	ua	(h)	Resistor					
	а) c)		citor					Transisto					
		•		onrocesso	r does th	ne concept							
	a)	8086		оргоссээс	n does a	ic concept		80286	roducca.				
	а) c)	8038						80486					
112.	c,			nd IP = 634	lΔ the nh	ıysical addr		00400					
	a)		6: 634A	Id II = 05-	, the pr	iysicai aaai		34F5F					
	c)	2B2/						24F60					
113.	- /			must at le	east consi	st of	(4)	21100					
	a)	Data	-	mast at it	2436 601131	30 01	(b)	Address B	SUS				
	c)		rol Bus					all of the					
				system tha	at allows	several pro				ion at the	same tim	e is called as	
_			, , , , , , , , , , , , , , , , , , ,	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,				о рололи.	ooparac				
(a)	Singl	e progran	n			(b)	Multitask	ing				
(c) Multiprocessing (d) Real time processing													
,	,		•	Ü		ſ			•	J			
_						Į	Answe	rs				•	
	1.	(d)	2. (a)	3. (c)	4. (b)	5. (c)	6. (b)	7. (d)	8. (c)	9. (a)	10. (c)		
	11	(a)	12. (d)	13. (d)	14. (d)	15. (a)	16. (d)	17. (b)	18. (a)	19. (a)	20. (b)		
	21	(d)	22. (c)	23. (a)	24. (a)	25. (b)	26. (c)	27. (d)	28. (a)	29. (b)	30. (b)		
	31	(a)	32. (b)	33. (c)	34. (c)	35. (c)	36. (b)	37. (d)	38. (d)	39. (d)	40. (d)		
	41	L. (c)	42. (d)	43. (b)	44. (b)	45. (a)	46. (d)	47. (a)	48. (b)	49. (d)	50. (c)		
	51	L. (c)	52. (d)	53. (d)	54. (d)	55. (d)	56. (a)	57. (a)	58. (b)	59. (c)	60. (a)		
			62 (1)	62 (1)	64 ()	CF ()	66 ()	c= (L)	60 ()	co ()	70 (1)		

61. (c)

62. (b)

63. (d)

64. (a)

65. (a)

66. (c)

67. (b)

68. (a)

69. (a)

70. (d)

71. (c)	72. (c)	73. (c)	74. (d)	75. (d)	76. (a)	77. (a)	78. (c)	79. (e)	80. (a)
81. (a)	82. (a)	83. (a)	84. (d)	85. (b)	86. (a)	87. (a)	88. (c)	89. (c)	90. (a)
91. (b)	92. (a)	93. (b)	94. (a)	95. (b)	96. (a)	97. (a)	98. (a)	99. (a)	100. (a)
101. (a)	102.(c)	103. (c)	104. (b)	105. (b)	106. (b)	107. (a)	108. (a)	109. (d)	110. (a)
111. (a)	112.(c)	113. (d)	114. (c)		•	•	•	•	

	MULTIPLE CHOICE QUESTIONS (MCQ's)					
1.	The	80386 DX is bit microprocessor.				
	(a)	16	(b)	24		
	(c)	8	(d)	32		
2.	Wha	at is the size of data bus in 80386 DX micropro	oces	sor?		
	(a)	8-bit	(b)	16-bit		
	(c)	32-bit	(d)	64-bit		
3.	Wha	at is the size of address bus in 80386 DX micro	opro	cessor?		
	(a)	8-bit	(b)	32-bit		
	(c)	16-bit	(d)	24-bit		
4.	Wha	at is the size of registers in 80836 microproce	ssor	?		
	(a)	8-bit	(b)	16-bit		
	(c)	24-bit	(d)	32-bit		
5.	Hov	v much physical memory can be accessed by 8	3038	36 microprocessor?		
	(a)	1 MB	(b)	4 MB		
	(c)	4 GB	(d)	64 TB		
6.	Hov	v much virtual memory can be accessed by 80	386	microprocessor?		
	(a)	1 MB	(b)	4 MB		
	(c)	4 GB	(d)	64 TB		
7.	The	80386 DX microprocessor has				
	(a)	pipelined architecture	(b)	separate data bus and address bus		
	(c)	multitasking	(d)	all of above		

8.	What is the size of barrel shifter in 80386 μ_{p} ?				
	(a)	32-bit	(b)	48-bit	
	(c)	64-bit	(d)	80-bit	
9.	Wha	at is the size of prefetch queue in 80386 μ_{p} ?			
	(a)	6 bytes	(b)	10 bytes	
	(c)	12 bytes	(d)	16 bytes	
10.	Wha	at is the function of bus interface in 80386 μ_{p}	?		
	(a)	To communicate between different pars of 8	8038	36 μ _p	
	(b)	To generate control signals			
	(c)	To interface between 80386 μ_{p} and input/or	utpu	t devices and memory	
	(d)	all of above			
11.	If pa	nging unit is enabled then			
	(a)	it translates linear address to physical addre	SS		
	(b)	it translates virtual address to physical addre	ess		
	(c)	(a) and (b) are same			
	(d)	(a) or (b)			
12.	How	many functional units are present in 80386	μ_p ?		
	(a)	6	(b)	8	
	(c)	10	(d)	12	
13.	If PE	E = 1, then 80386 DX microprocessor operates	s in .		
	(a)	Real mode	(b)	Protected mode	
	(c)	Virtual 86 mode	(d)	Special mode	
14.	Actu	ually how many pins are used in address gene	ratio	on of 80386 microprocessor?	
	(a)	32 pins	(b)	34 pins	
	(c)	20 pins	(d)	36 pins	

15.	Which pin is not used for controlling bus action of 80386 microprocessor?				
	(a)	ADS	(b) NA		
	(c)	BS16	(d) RESET		
16.	Wh	ich pin is not present in 8086 microprocessor	but present in 80386 microprocessor?		
	(a)	READY	(b) RESET		
	(c)	M/IO	(d) W/R		
17.	Wh	ich pins acts as hardware interrupt pins in 80	386 microprocessor?		
	(a)	NMI	(b) RESET		
	(c)	INTR	(d) all of above		
18.	Wh	ich pin is not connected to math coprocessor	in 80386 microprocessor?		
	(a)	READY	(b) PEREQ		
	(c)	BUSSY	(d) ERROR		
19.	Wh	at is the use of $\overline{\text{BEO}}$ - $\overline{\text{BE3}}$ pins of 80386 mic	roprocessor?		
	(a)	To enable memory ICs			
	(b)	To enable byte transfer			
	(c)	To generate an address			
	(d)	All of above			
20.	Wh	at happens after providing reset to 80386 mid	croprocessor?		
	(a)	It starts execution from address FFFFFF0H			
	(b)	ESP = FFFFFFFH			
	(c)	80386 operates in real mode			
	(d)	all of above			
21.	Wh	ich hardware interrupt pin has highest priorit	y?		

		(a)	INTR	(b)	NMI
		(c)	RESET	(d)	Cannot define
22.	Wh	en carr	ry flag is set?		
	(a)	If car	ry generated out of MSB		
	(b)	If car	ry generated out of D15 bit		
	(c)	If car	ry generated out of D3 bit		
	(d)	All of	above		
23.	Wh	en pari	ity flag is set?		
	(a)	If res	ult contains even number of 1's		
	(b)	If low	ver byte contains even number of 1s		
	(c)	If low	ver byte contains odd number of 1s		
	(d)	If low	ver word contains odd number of 1s		
24.	Wh	en aux	iliary flag is set?		
	(a)	If car	ry generates out of MSB		
	(b)	If car	ry generates out of D7 bit		
	(c)	If car	ry generates out of D3 bit		
	(d)	If car	ry generates out of D15 bit		
25.	Wh	en ove	erflow flag is set?		
	(a)	If car	ry is generated out of D6 bit in signed number	er o _l	peration
	(b)	If car	ry is generated out of D14 bit in signed numl	ber (operation
	(c)	If car	ry is generated out of D30 bit in signed numl	ber (operation
	(d)	All of	above		
26.	If di	rection	n flag is set then		
	(a)	SI is a	automatically decremented		
	(b)	SI is a	automatically incremented		

	(c)	DI is	automatically decremented			
	(d)	Botl	n (a) and (c)			
27.	Wha	at is the use of trap flag?				
	(a)	To c	debug the program			
	(b)	То є	execute the instruction at a time			
	(c)	To c	check register or memory contents before cor	mplete execution		
	(d)	All c	of above			
28.	Whi	ch fla	ag is not present in 8086 microprocessor but p	present in 80386 microprocessor?		
	(a)	Nes	ted Task Flag	(b) Sign Flag		
	(c)	Trap	o Flag	(d) Zero Flag		
29.	Whi	ch IC	PPL value has highest priority?			
	(a)	0	(b)	2		
	(c)	1	(d)	3		
30.	Whe	en ze	ro flag is set?			
	(a)	Afte	er comparison instruction if source and destin	ation are equal		
	(b)	If Al	LU result is zero			
	(c)	Botl	h (a) and (b)			
	(d)	It depends on programmer.				
	31.	Wha	at is the use of base registers and offset regist	ters?		
		(a)	To hold 16-bit relative address present within	in the segment		
		(b)	To perform arithmetic and logical operation	s		
		(c)	To hold the data temporary			
		(d)	All of above			
	22	\ \/ hi	ich ragistar cannot ha dividad into 9 hit data?			

		(a)	AX	(b)	CX
		(c)	DX	(d)	SI
	33.	How	many segment registers are present in 8038	6?	
		(a)	4	(b)	2
		(c)	6	(d)	8
	34.	How	many data segments are present in 80386 m	nicro	processor?
		(a)	2	(b)	3
		(c)	4	(d)	5
	35.	Wha	at is the size of segment selector in 80386 mic	rop	rocessor?
		(a)	16 bit	(b)	32 bit
		(c)	48 bit	(d)	64 bit
	36.	Wha	at is the size of offset register in 80386 microp	oroc	essor?
	(a)	16 b	it	(b)	32 bits
	(c)	48 b	it	(d)	64 bits
37.	Wha	it is t	he size of general purpose registers in 80386	mic	roprocessor?
	(a)	16 b	it	(b)	32 bits
	(c)	48 b	it	(d)	64 bits
38.	Wha	it is t	he size of control registers in 80386 micropro	cess	sor?
	(a)	16 b	its	(b)	32 bits
	(c)	48 b	its	(d)	64 bits
39.	How	man	ny control registers are present in 80386 micr	opro	ocessor?
	(a)	1	(b)	2	
	(c)	3	(d)	4	
40.	Wha	it is t	he size of debug registers in 80386 microproc	esso	or?
		(a)	16 bits	(b)	32 bits

		(c)	48 bits	(d)	64 bits		
	41.	How many debug registers are present in 80386 microprocessor?					
		(a)	3	(b)	4		
		(c)	7	(d)	8		
	42.	How	many break point addresses we can load in	deb	ug registers of 80386 microprocessor?		
		(a)	4	(b)	5		
		(c)	7	(d)	8		
	43.	Wha	at is the size of test registers?				
		(a)	16 bits	(b)	32 bits		
		(c)	48 bits	(d)	64 bits		
	44.	Wha	at is the use of test registers in 80386?				
		(a)	To test complete memory management unit	.			
		(b)	To test complete 80386 microprocessor				
		(c)	To test translation lookaside buffer				
		(d)	All of above				
	45.	In ta	ask register, how many bits are accessible by	user	?		
		(a)	16 bits	(b)	32 bits		
		(c)	48 bits	(d)	64 bits		
	46.	Wha	at is the size of the LDTR?				
		(a)	16 bits	(b)	32 bits		
	(c)	48 b	oits	(d)	64 bits		
47.	Wha	at is t	he size of GDTR?				
	(a)	16 b	nits	(b)	32 bits		
	(c)	48 b	pits	(d)	64 bits		

48. What is the size of IDTR?

	(a)	16 b	its	(b) 32 bits			
	(c)	48 b	pits	(d) 64 bits			
49.	Wha	it GD	TR and IDTR contains?				
	(a)	Segr	ment base address and limit				
	(b)	Acce	ess Right Byte				
	(c)	Туре	e of segment				
	(d)	All c	of above				
50.	Wha	it is t	he use of segment registers in 80386 micropr	ocessor?			
	(a)	To h	old base address of segment in real mode				
	(b)	To s	elect one of the segment descriptor in protec	ted mode			
	(c)	To select GDT or LDT in protected mode					
		(d)	All of above				
	51.	Wha	at is the use of LDTR in 80386 microprocessor	?			
		(a)	To select segment descriptor for LDT				
		(b)	To contain base address of LDT				
		(c)	To contain limit of LDT				
		(d)	Both (b) and (c)				
	52.	Whi	ch control register is called as page directory	base register?			
		(a)	CRO	(b) CR1			
		(c)	CR2	(d) CR3			
	53.	Whi	ch debug register is called as debug status re	gister in 80386?			
		(a)	DR5	(b) DR5			
		(c)	DR6	(d) DR7			
	54.	Whi	ch debug register is called as debug control re	egister in 80386?			

	(a)	DR4	(b)	DR5
	(c)	DR6	(d)	DR7
55.	Wh	at is the range of 8-bit unsigned integer?		
	(a)	0 to 255	(b)	-128 to +127
	(c)	0 to 65535	(d)	-32,768 to +32,767
56.	Wh	at is the range of 8-bit signed integer?		
	(a)	0 to 255	(b)	-128 to +127
	(c)	0 to 65535	(d)	-32,768 to +32,767
57.	Wha	at is the range of 16-bit unsigned integer?		
	(a)	0 to 255	(b)	-128 to +127
	(c)	0 to 65535	(d)	-32,768 to +32,767
58.	Wh	at is the range of 16-bit signed integer?		
	(a)	0 to 255	(b)	-128 to +127
	(c)	0 to 65535	(d)	-32,768 to +32,767
59.	Wh	at is the range of 32-bit bit unsigned integer?		
	(a)	0 to 65535	(b)	-32, 768 to +32,767
	(c)	0 to 4,294, 967, 295	(d)	$-2.147 \times 10^9 \text{ to } + 2.147 \times 10^9$
60.	Wh	at is the range of 32 bit signed integer?		
	(a)	0 to 65535	(b)	-32, 768 to +32,767
	(c)	0 to 4,294, 967, 295	(d)	$-2.147 \times 10^9 \text{ to } + 2.147 \times 10^9$
61.	Whi	ch data type is not present in 80386 micropro	oces	sor?
	(a)	Byte string	(b)	Word string
	(c)	Double word string	(d)	Quad word string
62.	Wha	at is the maximum size of data which can be h	and	lled by 80386?

		(a)	32 bits	(b)	48 bits		
		(c)	64 bits	(d)	80 bits		
	63.	Wha	at is the range of BCD number?				
		(a)	0 to 7	(b)	0 to 9		
		(c)	0 to 15	(d)	0 to 9 and A to F		
	64.	Whi	ch is not unpacked BCD number?				
		(a)	05H	(b)	00Н		
		(c)	09Н	(d)	10H		
65.	Whe	en an	instruction is read from the memory,	it is called			
	(a)	Mer	mory Read cycle	(b)	Fetch cycle		
	(c)	Inst	ruction cycle	(d)	Memory write cycle		
66.	Whi	ch fla	ng does the 80386 use to check for uns	igned arith	metic overflow?		
	(a)	OF	(b)	CF			
	(c)	SF	(d) Non	e of above			
67.	А ро	rt ca	n be				
	(a)	Stric	ctly Input	(b)	Strictly Output		
	(c)	Bidi	rectional	(d)	All of above		
68.	Whi	ch bu	is is bidirectional?				
	(a)	Con	trol Bus	(b)	Data Bus		
	(c)	Add	ress Bus	(d)	None of these		
	69.	-	orevent another master from taking o	ver the bus	during a critical operation, the 80386 can assert its		
	(a)	LOC	K#	(b)	HOLD or BOFF		
	(c)	HLD	Α	(d)	HOLD		
70.	In 80	n 80386 microprocessor, which interrupt has the highest priority?					

	(a)	INTR	(b) NMI				
	(c)	RESET					
71.	Why	Why 80386 processor is called as 32 bit processor?					
	(a)	Because 80386 processor has 32 bit ALU					
	(b)	Because 80386 processor has 32 bit data bus					
	(c)	(a) and (b)					
72.	Wha	it is meant by Maskable interrupts?					
	(a)	An interrupt which can never be turned off					
	(b)	An interrupt that can be turned off by the progra	nmmer				
	(c)	None					
73.	Wha	t does microprocessor speed depends on?					
	(a)	Clock	(b) Data bus width				
	(c)	Address bus width					
74.	Can	ROM be used as stack?					
	(a)	Yes (b)	No				
	(c)	sometimes yes, sometimes no					
	75.	In 80386 microprocessor, the following has the h	lighest priority among all types of interrupts.				
	(a)	NMI	(b) DIV 0				
	(c)	TYPE 255	(d) OVER FLOW				
76.	Num	nbers are stored and transmitted inside a compute	er in				
	(a)	binary form	(b) ASCII code form				
	(c)	decimal form	(d) alphanumeric form				
77.	The	original ASCII codes were					
	(a)	7 bits	(b) 8 bits				
	(c)	represented 256 characters	(d) represented 127 characters				

78.	The	ASCII code of 'A' is		
	(a)	66D (b)	11H	
	(c)	0100 0010	(d) 0110	0011
79.	The	ASCII code of '0' (zero) is		
	(a)	48D (b)	32H	
	(c)	0011 1000	(d) 42H	
80.	A by	rte corresponds to		
	(a)	4 bits	(b) 8 bits	5
	(c)	16 bits	(d) 32 bi	ts
81.	A gi	gabyte represents		
	(a)	1 billion bytes	(b) 1000	kilobytes
	(c)	2 ³⁰ bytes	(d) 1024	bytes
82.	A m	egabyte represents		
	(a)	1 million bytes	(b) 1000	kilobytes
	(c)	2 ³⁰ bytes	(d) 1024	bytes
83.	A 1k	(B corresponds to		
	(a)	1024 bits	(b) 1000	bytes
	(c)	2 ¹⁰ bytes	(d) 210b	its
84.	A 32	2-bit processor has		
	(a)	32 registers	(b) 32 I/0	O devices
	(c)	32 Mb of RAM	(d) a 32-	bit bus or 32-bit registers
85.	The	minimum number of bits required to store the h	kadecimal	number FFH is
	(a)	2, (b)	4	
	(c)	8 (d)	16	

86. A parity bit is

	(a)	used to indicate uppercase letters	
	(b)	used to detect errors	
	(c)	is the first bit in a byte	
	(d)	is the last bit in a byte	
87.	Cloc	k speed is measured in	
	(a)	bits per second	(b) baud
	(c)	bytes	(d) Hertz
88.	Pipe	lining improves CPU performance due to	
	(a)	reduced memory access time	
	(b)	increased clock speed	
	(c)	the introduction of parallellism	
	(d)	additional functional units	
89.	The	system bus is made up of	
	(a)	data bus	
	(b)	data bus and address bus	
	(c)	data bus and control bus	
	(d)	data bus, control bus and address bus	
90.	A ma	achine cycle refers to	
	(a)	fetching an instruction	
	(b)	clock speed	
	(c)	fetching, decoding and executing an instruction	า
	(d)	executing an instruction	
91.	CPU	performance may be measured in	
	(a)	BPS (b)	/IIPS
	(c)	MHz (d)	VLSI

92. Stack overflow causes

(a) Hardware interrupt

(b) External interrupt

(c) Internal interrupt

(d) Software interrupt

- 93. A 32-bit processor has
- (a) 32 register
- (b) 32 I/O devices
- (c) 32 Mb of RAM
- (d) a 32-bit data bus and 32-bit registers
- 94. What is meant by Maskable interrupts?
- (a) An interrupt that can be turned off by the programmer
- (b) An interrupt that cannot be turned off by the programmer
- (c) An interrupt that can be turned off by the system
- (d) An interrupt that cannot be turned off by the system
- 95. Which of the following is not possible by a microprocessor?
- (a) Reading from Memory

(b) Writing into Memory

(c) Reading from Input port

(d) Writing into Input port

Answers

115.	(116.	(117.	(118.	(119.	(120.	(121.	(122.	(123.	(124.	(
d)		c)		b)		d)		c)		d)		d)		c)		d)		d)	
125.	(126.	(127.	(128.	(129.	(130.	(131.	(132.	(133.	(134.	(
c)		a)		b)		b)		d)		d)		d)		a)		d)		d)	
135.	(136.	(137.	(138.	(139.	(140.	(141.	(142.	(143.	(144.	(
c)		a)		b)		c)		d)		d)		d)		a)		a)		c)	
145.	(146.	(147.	(148.	(149.	(150.	(151.	(152.	(153.	(154.	(
a)		d)		c)		c)		a)		b)		b)		b)		d)		b)	
155.	(156.	(157.	(158.	(159.	(160.	(161.	(162.	(163.	(164.	(
d)		a)		b)		c)		a)		a)		c)		c)		a)		d)	
165.	(166.	(167.	(168.	(169.	(170.	(171.	(172.	(173.	(174.	(
a)	d)			c)		d)		a)		b)		c)		d)		c)		d)	
175.	(176.	(177.	(178.	(179.	(180.	(181.	(182.	(183.	(184.	(

d)		d)		b)		d)		b)		b)		d)		b)		a)		c)	
185.	(186.	(187.	(188.	(189.	(190.	(191.	(192.	(193.	(194.	(
c)	c) b) c)			b) a)		a)			a)		b)		a)		b)				
195.	(196.	(197.	(198.	(199.	(200.	(201.	(202.	(203.	(204.	(
a)	a) b)			c)		d)		c)		b)		d)		c)		d)		c)	
205.	(206.	(207.	(208.	(209.	(
b)		c)		d)		a)		d)											