Total No. of Questions—8] [Total No. of Printed Pages—2

Seat No.	

[5252]-564

S.E. (Computer) (I Sem.) EXAMINATION, 2017
COMPUTER ORGANIZATION AND ARCHITECTURE
(2015 PATTERN)

Time : Two Hours **Maximum Marks : 50**

N.B. :— (*i*) Neat diagrams must be drawn wherever necessary.
(*ii*) Figures to the right side indicate full marks.
(*iii*) Use of calculator is allowed.
(*iv*) Assume suitable data if necessary.

1. (*a*) Multiply the following using Booth' algorithm. [6]

Multiplicand = + 11

Multiplier = – 6

(*b*) Explain in brief RAID levels in detail. [6]

Or

2. (*a*) Explain in detail IEEE standards for representing floating point numbers in the following formats.

(1) Single Precision

(2) Double Precision [6]

(*b*) Explain cache updating policies in detail. [6]

3. (*a*) What is the use of DMA ? Explain cycle stealing in DMA. [6]

(*b*) What is machine instruction ? Explain any *three* types of operations. [6]

Or

4. (*a*) Compare memory mapped I/O and I/O mapped I/O. [06]

P.T.O.

(*b*) Explain the following addressing modes with *one* example each : [6]

(*i*) Displacement Addressing

(*ii*) Register Indirect

5. (*a*) List the features of 8086 microprocessor. [7]

(*b*) Write a short note on superscalar execution and superscalar implementation. [6]

Or

6. (*a*) Explain the instruction pipelining. [6]

(*b*) Draw and explain architecture of 8086. [7]

7. (*a*) Write a control sequence for the following instruction for single bus organization : ADD (R3), R1 [6]

(*b*) Explain in detail state table design method for hardwired control design. [7]

Or

8. (*a*) Draw and explain in detail block diagram of hardwired control unit. [7]

(*b*) List the applications of microprogramming. [6]

Q.1	a)	Answer = -66 Each cycle = 1 ½ Mark 1 ½ * 4 = 6 Marks	[6]
	b)	1 Level = 1 Marks 1*6 = 6 Marks	[6]
		OR	
Q.2	a)	Single Precision(3Marks) = Diagram 1 ½ Mark Explanation 1 ½ Double Precision(3Marks) = Diagram 1 ½ Mark Explanation 1 ½	[6]
	b)	Write through = 2 Marks Buffered write through = 2 Marks Write back = 2 Marks	[6]
Q.3	a)	use of DMA = 2 Marks Explanation of cycle stealing in DMA = 4 Marks	[6]
	b)	i) Machine Instruction definition = 1 ½ Mark 3 types of operation = each type 1 ½ Total = 4 ½	[6]
		OR	
Q.4	a)	Each point of Differentiation = 2 Marks 2*3=6 Marks	[6]
	b)	Displacement Addressing = 3 Marks Register Indirect = 3 Marks	[6]
Q.5	a)	Each Feature= 1 Marks 6 features= 6 Marks	[7]
	b)	Explanation of superscalar execution = 3 Marks Explanation of superscalar implementation = 3 Marks	[6]
		OR	
Q.6	a)	Instruction pipelining Diagram =3 Marks Explanation = 3 Marks	[6]
	b)	Diagram =3 Marks Explanation = 4 Marks	[7]
Q.7	a)	Instruction fetch = 2 Marks Operand Fetch= 2 Marks Execution of instruction steps= 2 Marks	[6]
	b)	State Table method Explanation= 7 Marks	[7]
		OR	
Q. 8	a)	Diagram = 3 Marks Explanation = 4 Marks	[7]
	b)	At least 4 Applications 6 Marks	[6]