Unit-III Protection and Multitasking
Multiple Choice Questions'- Set 1

1. The Applications are related with _____ privilege level.
a) Level 0 b) Level 1 c) Level 2 d) Level 3

2. The privilege level of the code segment determines the _____.
a) RPL b) DPL c) CPL d) IOPL

3. Which of the following is not protection aspect of 80386 _____.
a) Restriction of addressable domain b) Restriction of interrupt entry point
c) Restriction of procedure entry points d) Restriction of instruction set

4. The limit bit in data segment descriptor is _____.
a) 6-bit b) 3-bit c) 2-bit d) 4-bit

5. In the executable segment descriptor the conforming bit comes under _____.
a) Limit b) Type c) Base d) Offset

6. The linear address is calculated by
a) effective address + segment base address
b) effective address –segment base address
c) effective address + physical address
d) effective address –physical address

7. If the paging unit is enabled, then it converts linear address into
a) Effective address
b) physical address
c) segment base address
d) none of the mentioned

8. If the paging unit is disabled, then the linear address is used as
a) effective address
b) physical address
c) segment base address
d) none of the mentioned

9. The paging unit is enabled only in
a) virtual mode
b) addressing mode
c) protected mode
d) none of the mentioned

10. For a single task in protected mode, the 80386 can address the virtual memory of
a) 32 GB
b) 64 MB
c) 32 TB
d) 64 TB

11. The bit that indicates whether the segment has been accessed by the CPU or not is
a) base address
b) attribute bit
c) present bit
d) granular bit

12. The TYPE field of descriptor is used to find the
a) descriptor type
b) segment type
c) descriptor and segment type
d) none

13. If the segment descriptor bit, S=0, then the descriptor is
a) data segment descriptor
b) code segment descriptor
c) system descriptor
d) all of the mentioned

14. The bit that indicates whether the segment is page addressable is
a) base address
b) attribute bit
c) present bit
d) granularity bit

15. If the Default operation size bit, D=1, the code segment operation size selected is
a) 8-bit
b) 16-bit
c) 32-bit
d) 64-bit

16. The segment descriptor contains
a) access rights
b) limit
c) base address
d) all of the mentioned

17. Which of the following is not a type of segment descriptor?
a) system descriptors
b) local descriptors
c) gate descriptors
d) none

18. The limit field of the descriptor is of
a) 10 bits
b) 8 bits
c) 16 bits
d) 20 bits
Answer: d

19. The starting address of the segment in physical memory is decided by
a) physical memory
b) segment descriptors
c) operating system
d) base address

20. The total descriptors that the 80386 can handle is
a) 2K
b) 8K
c) 4K
d) 16K

21. The advantage of pages in paging is
a) no logical relation with program
b) no need of entire segment of task in physical memory
c) reduction of memory requirement for task
d) all of the mentioned

22. The size of the pages in paging scheme is
a) variable
b) fixed
c) both variable and fixed
d) none

23. To convert linear addresses into physical addresses, the mechanism that the paging unit uses is
a) linear conversion mechanism
b) one level table mechanism
c) physical conversion mechanism
d) two level table mechanism

24. The control register that stores the 32-bit linear address, at which the previous page fault is detected is
a) CR0
b) CR1
c) CR2
d) CR3

25. Which of the following is not a component of paging unit?
a) page directory
b) page descriptor base register
c) page table
d) page

26. The control register that is used as page directory physical base address register is
a) CR0
b) CR1
c) CR2
d) CR3

27. The bits of CR3, that are always zero are
a) higher 4 bits
b) lower 8 bits
c) higher 10 bits
d) lower 12 bits

28. Each directory entry in page directory is maximum of
a) 2 bytes
b) 4 bytes
c) 8 bytes
d) 16 bytes

29. The size of each page table is of
a) 2 Kbytes
b) 2 bytes
c) 4 Kbytes
d) 4 bytes

30. The dirty bit(D) is set, before which operation is carried out
a) write
b) read
c) initialization
d) none of the mentioned

31. The bit that is undefined for page directory entries is
a) P-bit
b) A-bit
c) D-bit
d) all of the mentioned

32. The bit that is used for providing protection is
a) User/Supervisor bit
b) Read bit
c) Write bit
d) all of the mentioned

33. The storage of 32 recently accessed page table entries to optimize the time, is known as
a) page table
b) page descriptor base register
c) page table cache
d) none of the mentioned

34. The page table cache is also known as
a) page table storage
b) storage buffer
c) translation look aside buffer
d) all of the mentioned

35. In TSS of 80386 the field PDBR is associate with _____.

a) static b) dynamic c) reserved d) bank

36. The dynamic set includes the fields that store which of the following:
a) LDT b) PDBR c) Flag register d) GDT

37. The task state segment descriptor the 'B' bit having bit number ___.
a) 7 b) 8 c) 9 d) 10

38. The TSS with a selector that has TI = 1 _____ results in an exception.
a) Indicating the current LDT b) Indicating the current IDT
c) Indicating the current GDT d) Indicating the current IVT

39. The SELECTOR field of a task gate must refer to a _____.
a) TSS b) base address c) Segment Limit d) TSS descriptor

40. The 80386 switches execution to another task, identify the wrong choice from following cases:
a) The current task executes an IRET when the NT flag is set.
b) An interrupt or exception vectors to a task gate in the IDT.
c) The current task executes JMP or CALL that refers to the LDT.
d) The current task executes a JMP or CALL that refers to a task gate.

41. The NT flag indicates whether the _____ field is valid.
a) front-link b) back-link c) next-link d) previous-link

42. The new task releases control by executing _____.
a) IRET instruction b) LAR instruction c) LSL instruction d) VERW instruction

43. The ability for tasks to have _____ is an important aspect of 80386 protection.
a) same address spaces b) contiguous address spaces c) distinct address spaces d) external address spaces

44. In task nesting _____ pointing to the link field.
a) TSS b) TSS descriptor c) Task Gate d) Task Register

45. If CPL=0 then the processor is executing at _____.
a) User level b) Supervised level c) U/S level d) None of these

Answers:

1. d)	2. c)	3. b)	4. d)	5. b)
6. a)	7. b)	8. b)	9. c)	10. d)
11. b)	12. c)	13. c)	14. d)	15. c)
16. d)	17. d)	18. d)	19. c)	20. d)
21. d)	22. b)	23. d)	24. c)	25. b)
26. d)	27. d)	28. b)	29. c)	30. a)
31. c)	32. d)	33. c)	34. c)	35. a)
36. c)	37.c)	38. a)	39. d)	40. c)
41. b)	42. a)	43. c)	44. d)	45. b)