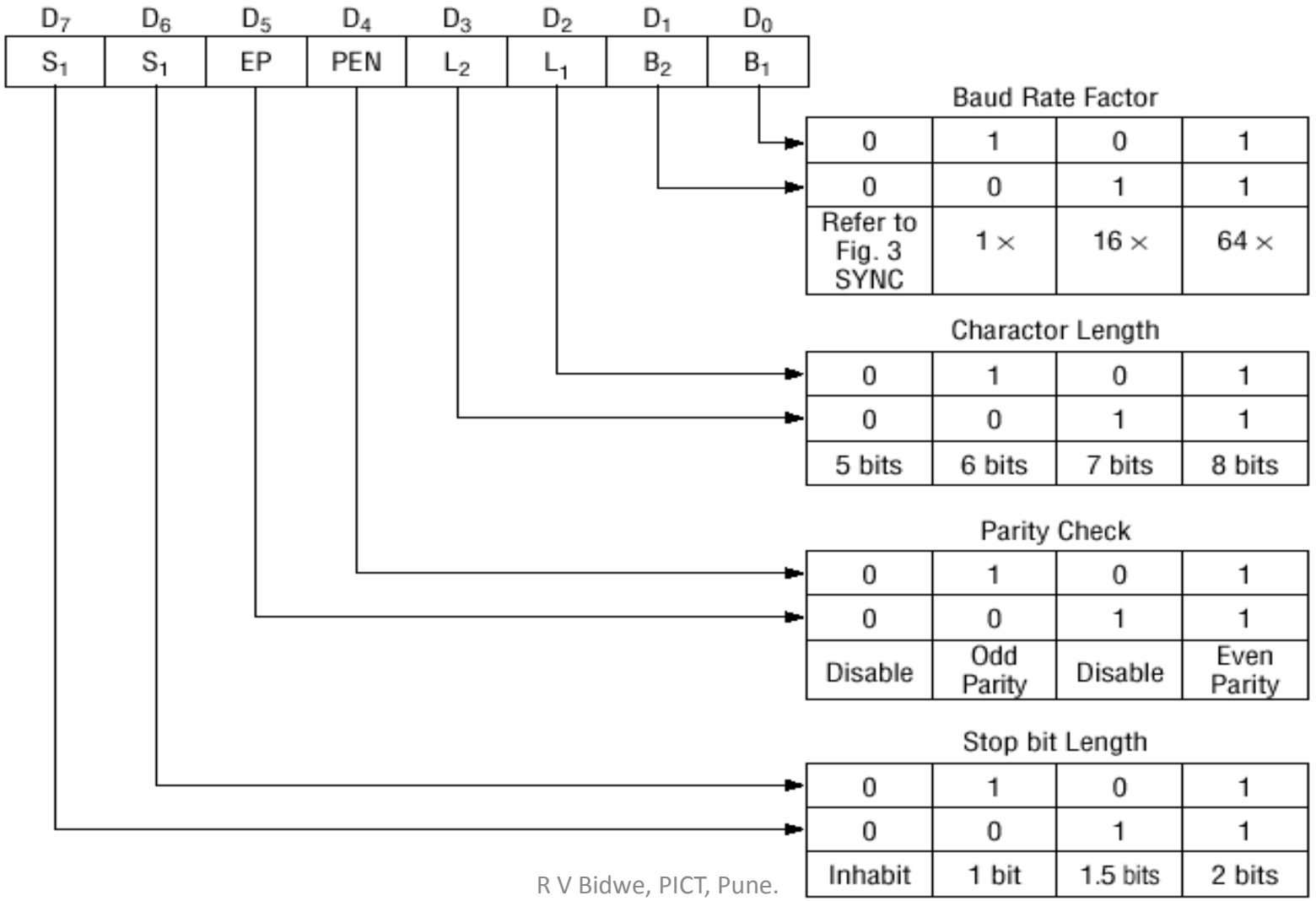
Interfacing with 8086

8251 with 8086

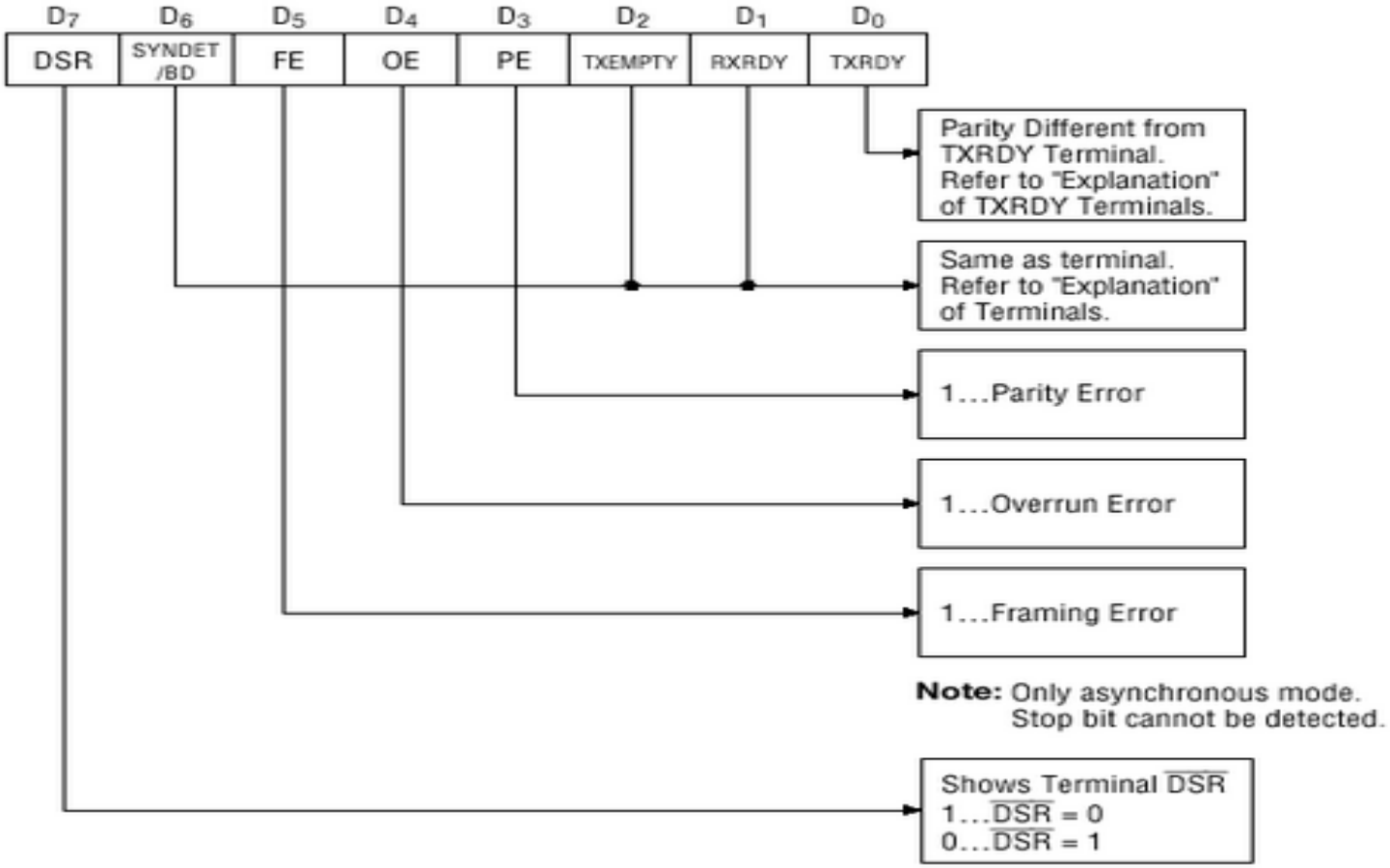
- Perform an experiment to establish communication between two 8251 systems A and B. Program 8251 system A in asynchronous transmitter mode and 8251 system B in asynchronous receiver mode. Write an ALP to transmit the data from system A and receive the data at system B.

  - No of stop bits- 01
  - Parity Disables
  - 1 byte data is to be transmitted
  - Clock used is 1x.

Mode Instruction Control Word (Asynchronous Mode)



Status Word

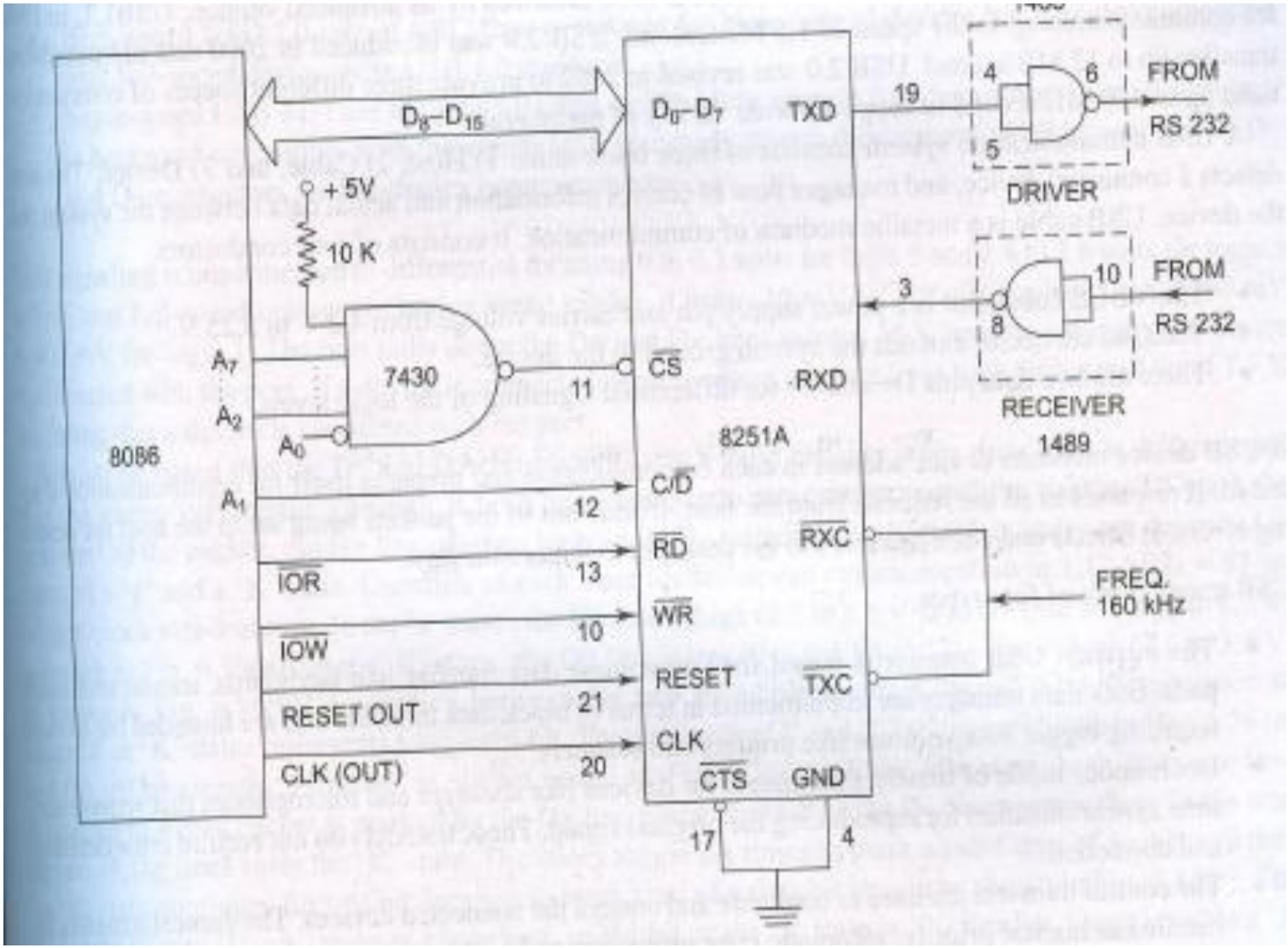

D7
D6
D5
D4
D3
D2
D1
D0
DSR
SYNDET /BD
FE
OE
PE
TXEMPTY
RXRDY
TXRDY
Parity Different from TXRDY Terminal. Refer to "Explanation" of TXRDY Terminals.
Same as terminal. Refer to "Explanation" of Terminals.
1...Parity Error
1...Overrun Error
1...Framing Error
Note: Only asynchronous mode. Stop bit cannot be detected.
Shows Terminal $\overline{DSR}$
1...$\overline{DSR}$ = 0
0...$\overline{DSR}$ = 1

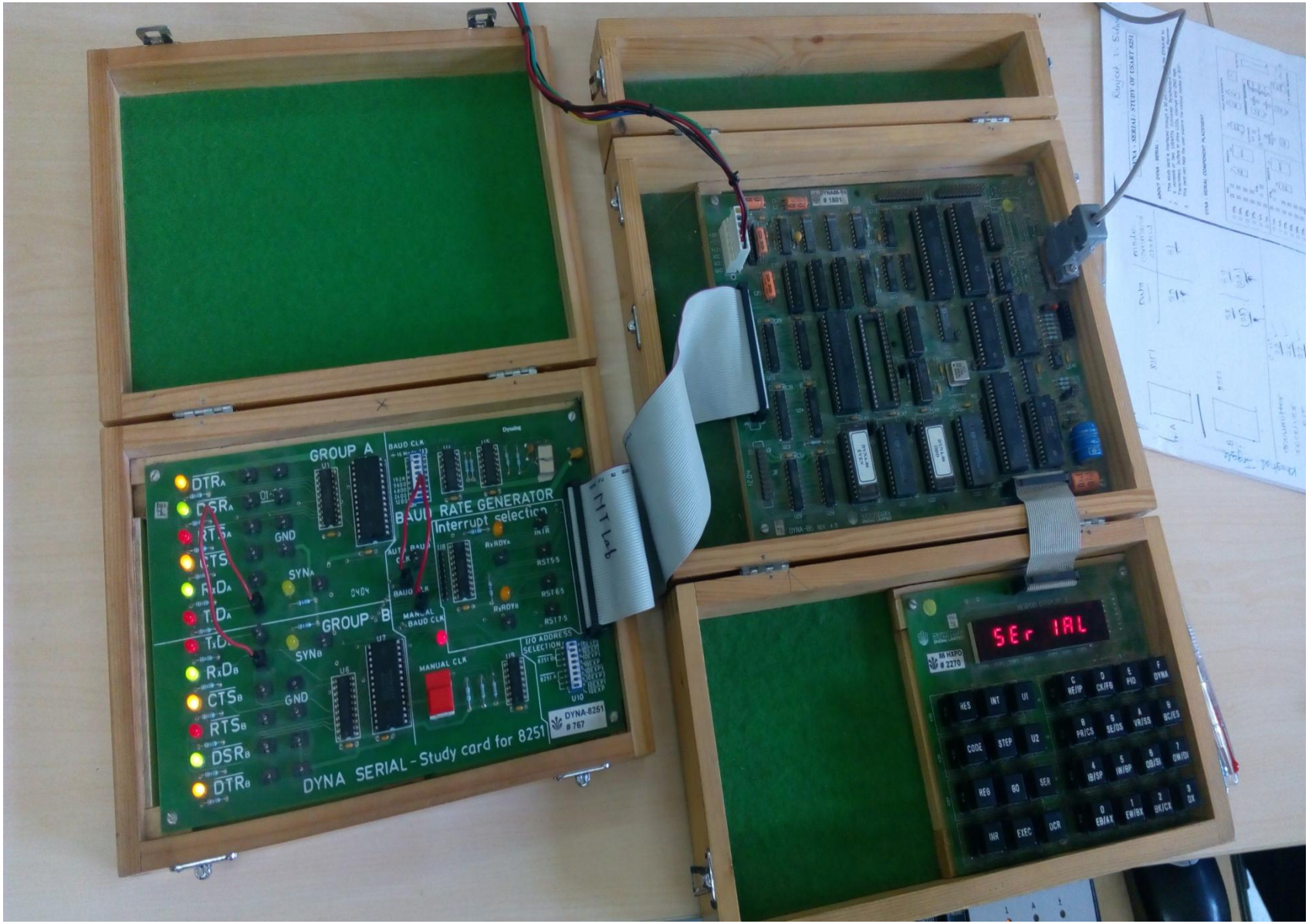
Byte Transfer

```
Dyna-86>A 3000
0000:3000  MOV AL,4D
0000:3002  OUT 31,AL
0000:3004  OUT 29,AL
0000:3006  MOV AL,27
0000:3008  OUT 31,AL
0000:300A  OUT 29,AL
0000:300C  MOV AL,59
0000:300E  OUT 30,AL
0000:3010  IN AL,29
0000:3012  TEST AL,02
0000:3014  JZ 3010
0000:3016  IN AL,28
0000:3018  MOV BL,AL
0000:301A  INT 3
0000:301B
```

Block Transfer

- **Dyna-86>A 5000**
- **0000:5000 MOV AL,4D**
- **0000:5002 OUT 31,AL**
- **0000:5004 OUT 29,AL**
- **0000:5006 MOV AL,27**
- **0000:5008 OUT 31,AL**
- **0000:500A OUT 29,AL**
- **0000:500C MOV SI,6000**
- **0000:500F MOV DI,8000**
- **0000:5012 MOV CL,[SI]**
- **0000:5014 INC SI**
- **0000:5015 MOV AL,[SI]**
- **0000:5017 OUT 30,AL**
- **0000:5019 IN AL,29**
- **0000:501B TEST AL,02**
- **0000:501D JZ 5019**
- **0000:501F IN AL,28**
- **0000:5021 MOV [DI],AL**
- **0000:5023 INC SI**
- **0000:5024 INC DI**
- **0000:5025 DEC CL**
- **0000:5027 JNZ 5015**
- **0000:5029 INT 3**
- **0000:502A**


8086
D_8–D_{15}
+ 5V
10 K
A_7
A_2
A_0
7430
11
A_1
IOR
13
IOW
10
RESET OUT
21
CLK (OUT)
20
D_0–D_7
TXD
19
CS
RXD
8251A
C/D
12
RD
WR
RESET
CLK
CTS
GND
17
4
RXC
TXC
FREQ.
160 kHz
4
6
5
FROM
RS 232
DRIVER
3
10
8
FROM
RS 232
RECEIVER
1489

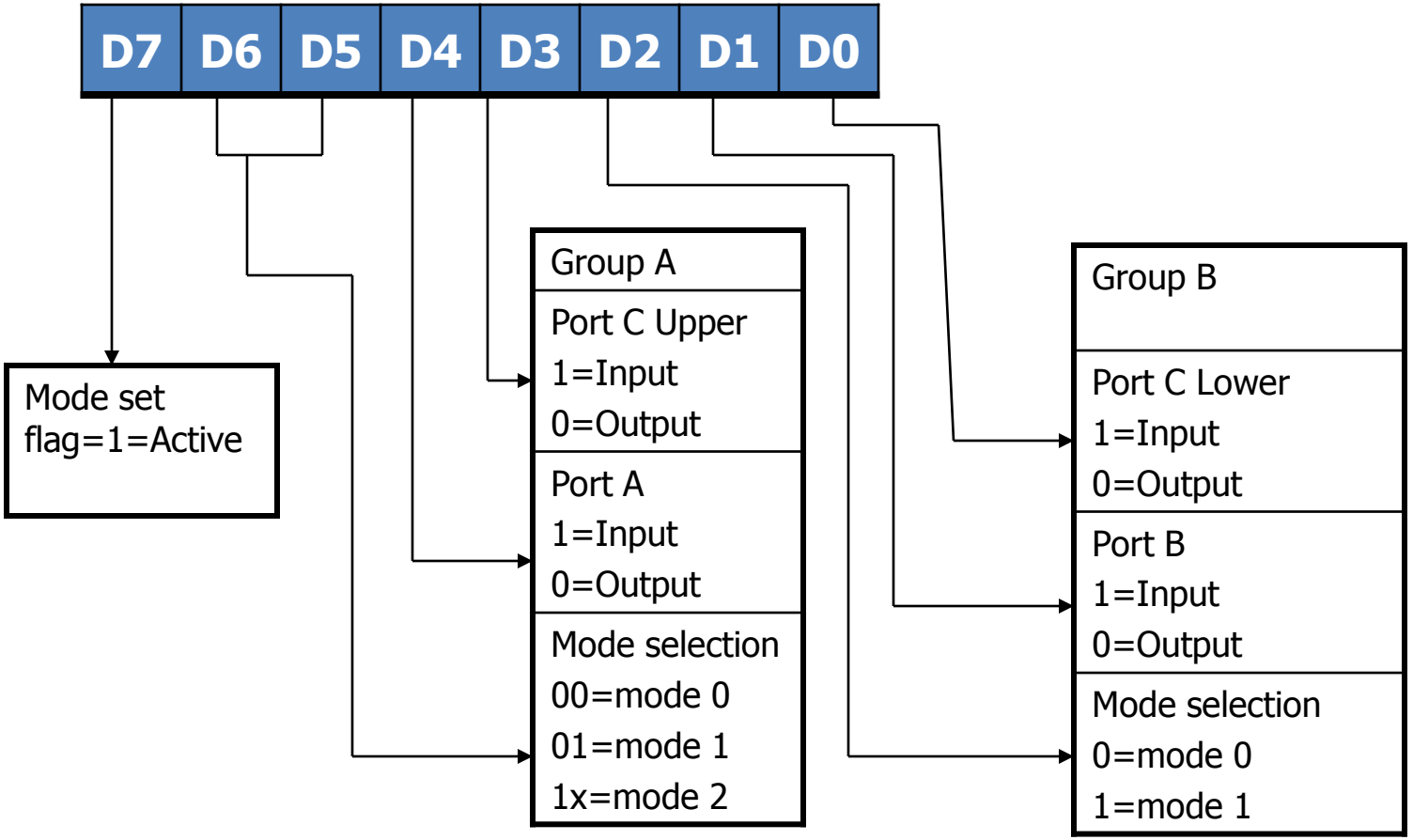

GROUP A
BAUD RATE GENERATOR
Interrupt selection
GROUP B
MANUAL CLK
I/O ADDRESS SELECTION
DYNA-8251 #767
DYNA SERIAL - Study card for 8251
SEr IAL

8255 with 8086 ADC

- Given:
  - PORT A: Input Port (Address: 61H)
  - PORT B: Output Port (Address: 63H)
  - PORT C: Input Port (Address: 65H)
  - Command Port: (Address: 67H)
- Given Voltage Value:
  - For 0 V=00 (Digital Value)
  - For 5 V=FF (Digital Value)
- 8255 Command Word: 99H
- For Port B:
  - Before SOC= 05
  - After SOC=04
- For Port C:
  - After EOC=01
- Make OE=1 and Stop.

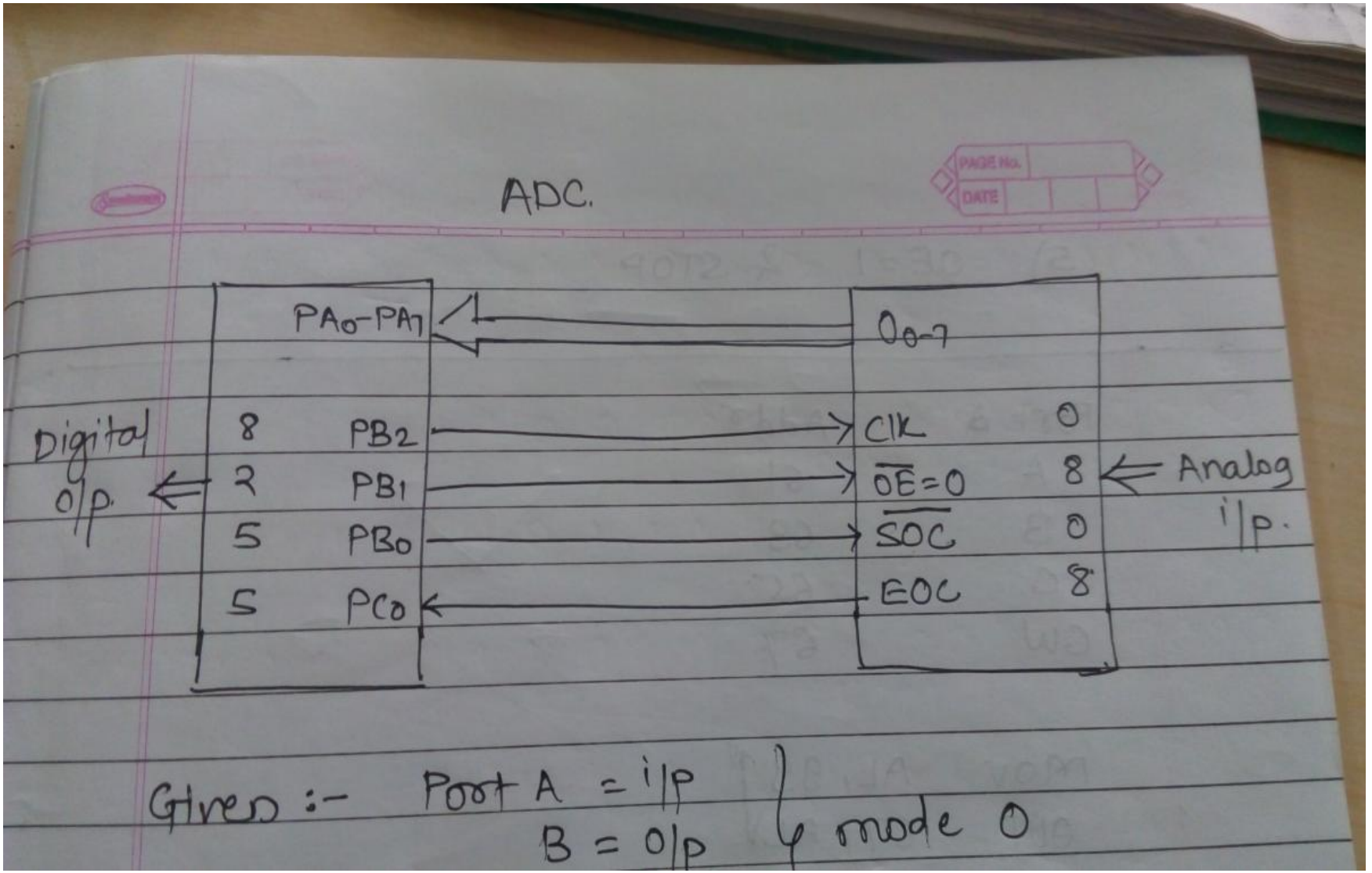
- **FOR I/O MODE: 8255**

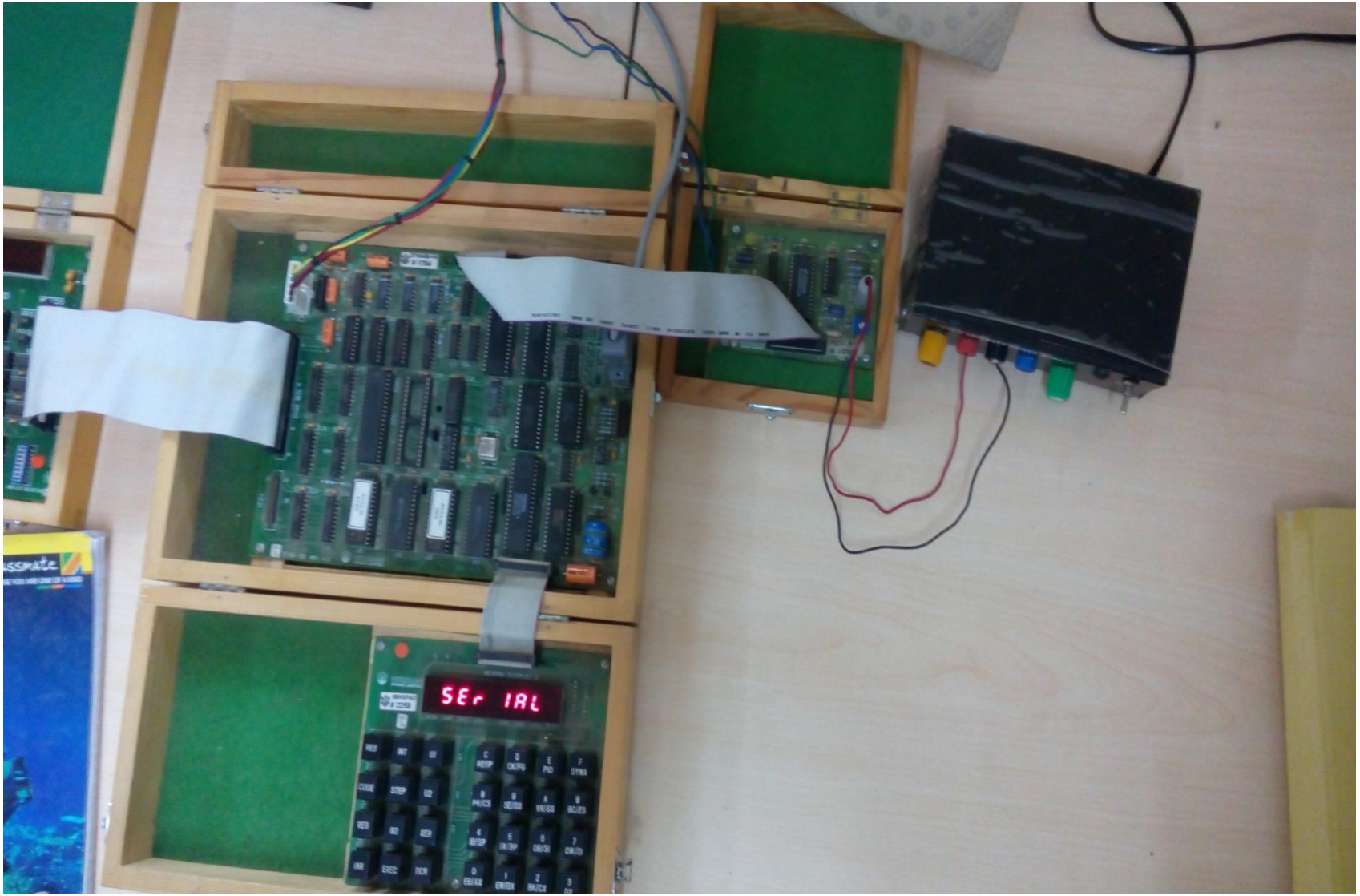
The mode format for I/O as shown in figure



```
Dyna-86>A 1000
0000:1000  MOV AL,99
0000:1002  OUT 67,AL
0000:1004  MOV AL,05
0000:1006  OUT 63,AL
0000:1008  MOV AL,04
0000:100A  OUT 63,AL
0000:100C  IN AL,65
0000:100E  TEST AL,01
0000:1010  JZ 100C
0000:1012  MOV AL,06
0000:1014  OUT 63,AL
0000:1016  IN AL,61
0000:1018  MOV BL,AL
0000:101A  INT 3

Dyna-86>R
AX=0000  BX=0000  CX=0000  DX=0000  SP=06FF  BP=0000  SI=0000
DI=0000  CS=0000  DS=0000  SS=0000  ES=0000  IP=0700  FL=0000
```


ADC.
PA0-PA7
O0-7
Digital
o/p
8
PB2
CLK
0
3
PB1
OE=0
8
Analog
i/p.
5
PB0
SOC
0
5
PC0
EOC
8
Given :- Port A = i/p
B = o/p
mode 0

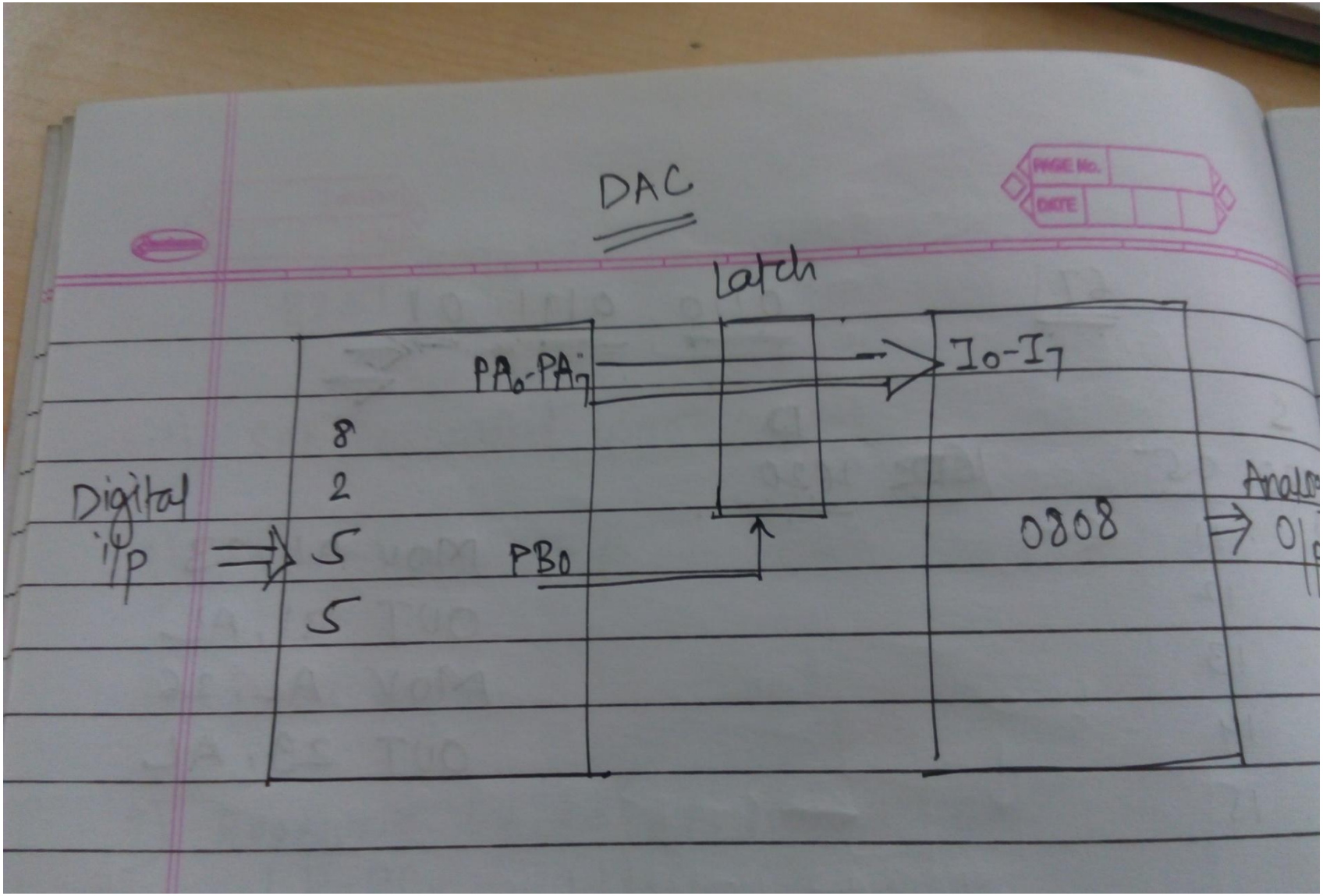

SEr IAL

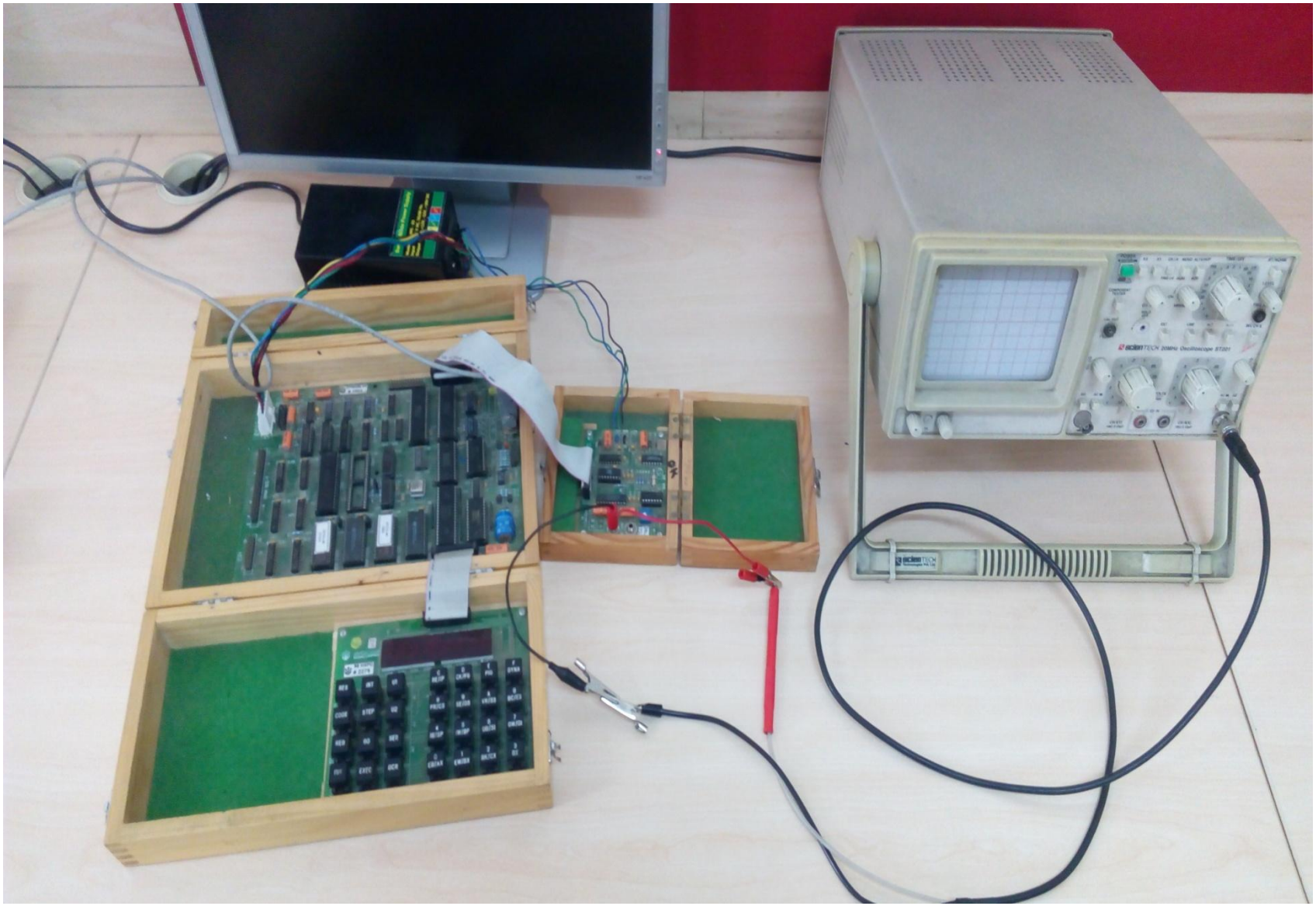
8255 with 8086 DAC

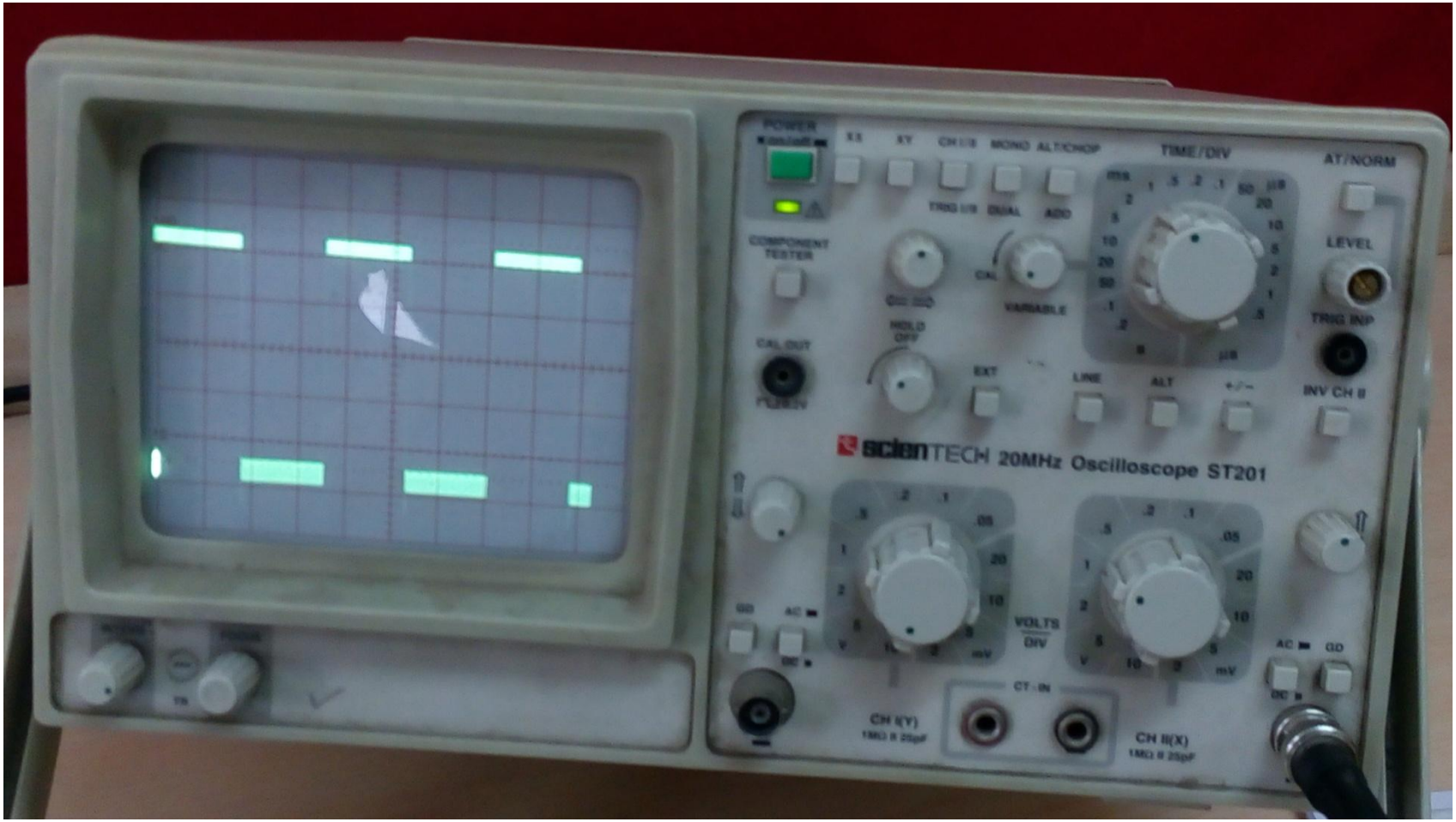
- Given:
  - PORT A: Output Port (Address: 61H)
  - PORT B: Output Port (Address: 63H)
  - PORT C: Input Port (Address: 65H)
  - Command Port: (Address: 67H)
- Given Digital Value:
  - For 00=0 V (Digital Value)
  - For FF=5 V (Digital Value)

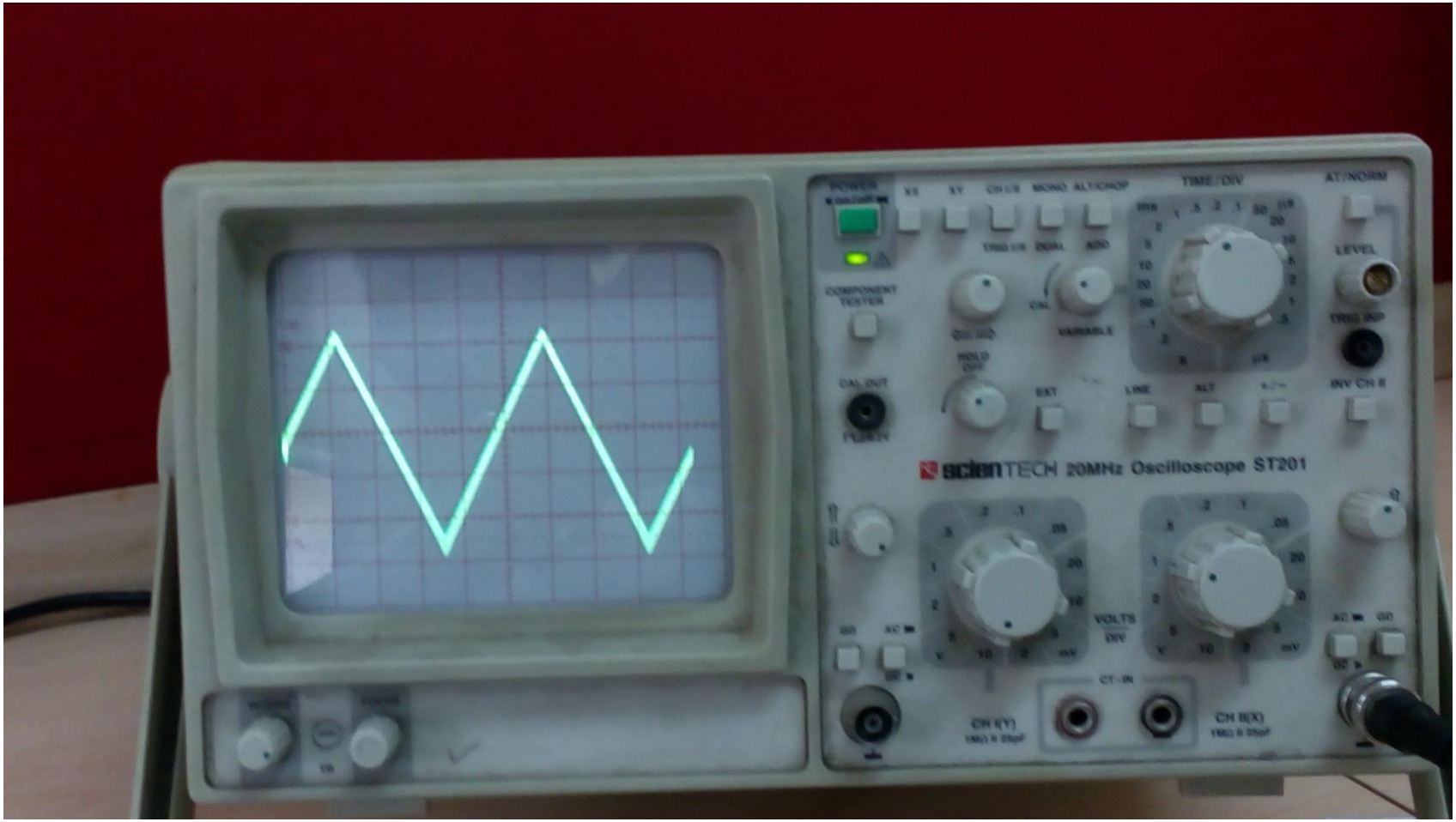
SQUARE WAVE

```
Dyna-86>A 1000
0000:1000  MOV AL, 89
0000:1002  OUT 67, AL
0000:1004  MOV AL, 01
0000:1006  OUT 63, AL
0000:1008  MOV CL, FF
0000:100A  MOV AL, FF
0000:100C  OUT 61, AL
0000:100E  DEC CL
0000:1010  JNZ 100C
0000:1012  MOV CL, FF
0000:1014  MOV AL, 00
0000:1016  OUT 61, AL
0000:1018  DEC CL
0000:101A  JNZ 1016
0000:101C  JMP 1008
0000:101E  INT 3
Dyna-86>G 1000
```


DAC
Latch
PA0-PA7
I0-I7
8
2
5
5
Digital
i/p
PB0
0808




POWER
TIME/DIV
AT/NORM
LEVEL
TRIG INP
INV CH II
scienTECH 20MHz Oscilloscope ST201
VOLTS
DIV
CH I(Y)
CH II(X)


TIME/DIV
LEVEL
VOLTS
DIV
CH I(Y)
CH II(X)

8279 with 8086

Write 8086 ALP to initialize 8279 and to display characters in right entry mode.

Provide also the facility to display

- Character in left entry mode.
- Rolling display.
- Flashing display

8279 working in

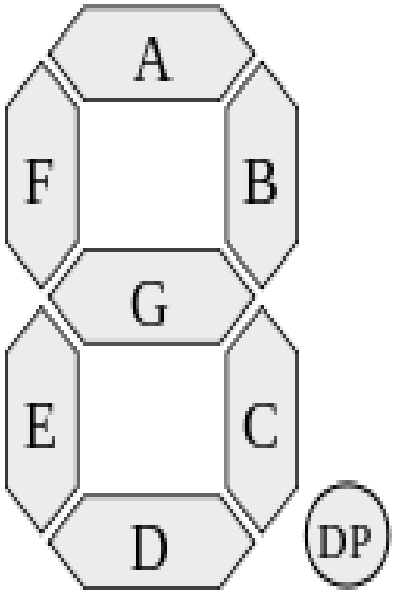
- Eight 8-bit display
- Left entry/ Right Entry
- Encoded scan
- 2-key lock out mode.
- So, **Keyboard Display Mode Set** Command Word Value: 00000000 = **00H (Left Entry)**
- And 00010000 = 10H **(Right Entry)**

For Dynalog KIT:

Command Port= 30H

Data Port= 31H

7 Segment Display



Value calculated using sequence:

DCBA FGEH

Command Words of 8279

All the command words or status words are written or read with **A0 = 1 and CS = 0 to or from 8279.**

A. Keyboard Display Mode Set : The format of the command word to select different modes of operation of 8279 is given below with its bit definitions.

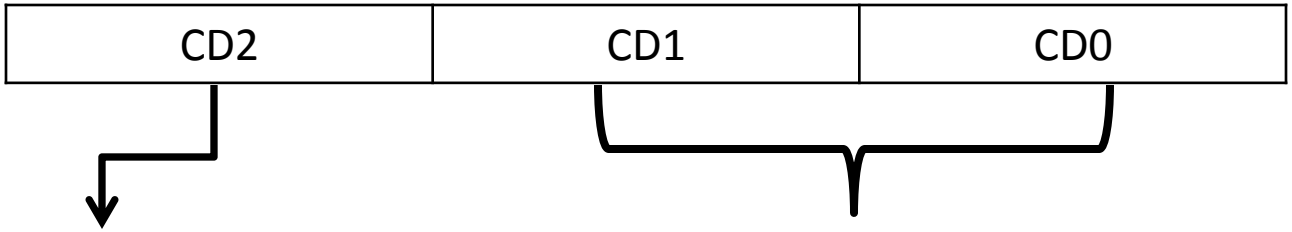
D7	D6	D5	D4	D3	D2	D1	D0	A0
0	0	0	D	D	K	K	K	1

D	D	Display modes
0	0	Eight 8-bit character Left entry
0	1	Sixteen 8-bit character left entry
1	0	Eight 8-bit character Right entry
1	1	Sixteen 8-bit character Right entry

K	K	K	Keyboard modes
0	0	0	Encoded Scan, 2 key lockout (Default after reset)
0	0	1	Decoded Scan, 2 key lockout
0	1	0	Encoded Scan, N- key Roll over
0	1	1	Decoded Scan, N- key Roll over
1	0	0	Encode Scan, **SENSOR MATRIX**
1	0	1	Decoded Scan, **SENSOR MATRIX**
1	1	0	Strobed Input Encoded Scan
1	1	1	Strobed Input Decoded Scan

G. Clear Display RAM :

D7	D6	D5	D4	D3	D2	D1	D0	A0
1	1	0	CD2	CD1	CD0	CF	CA	**1**



ENABLES CLEAR DISPLAY WHEN CD2=1

0X - All zeros (x don't care) AB=00
10 - A3-A0 =2 (0010) and B3-B0=00 (0000)
11 - All ones (AB =FF), i.e. clear RAM

RIGHT ENTRY

```
0000:CCCF  MOV CL, 08
0000:CCD1  MOV AL, 10
0000:CCD3  OUT 31, AL
0000:CCD5  MOV BX, 1000
0000:CCD8  MOV AL, [BX]
0000:CCDA  CALL 4444
0000:CCDD  OUT 30, AL
0000:CCDF  INC BX
0000:CCE0  DEC CL
0000:CCE2  JNZ CCD8
0000:CCE4  INT 3
```

LEFT ENTRY

0000:CCCF MOV CL, 08

0000:CCD1 MOV AL, 00

0000:CCD3 OUT 31, AL

0000:CCD5 MOV BX, 1000

0000:CCD8 MOV AL, [BX]

0000:CCDA CALL 4444

0000:CCDD OUT 30, AL

0000:CCDF INC BX

0000:CCE0 DEC CL

0000:CCE2 JNZ CCD8

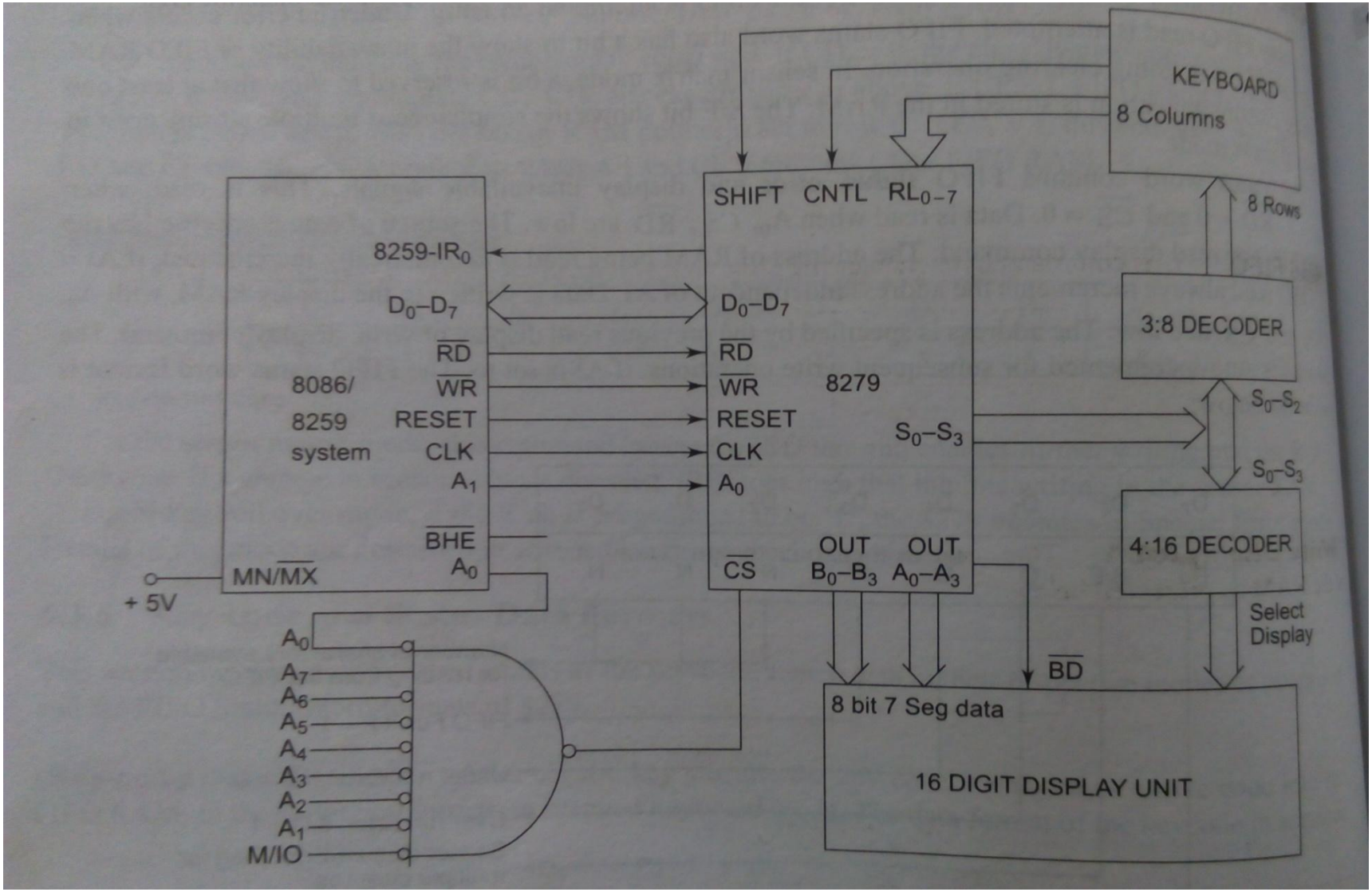
0000:CCE4 INT 3

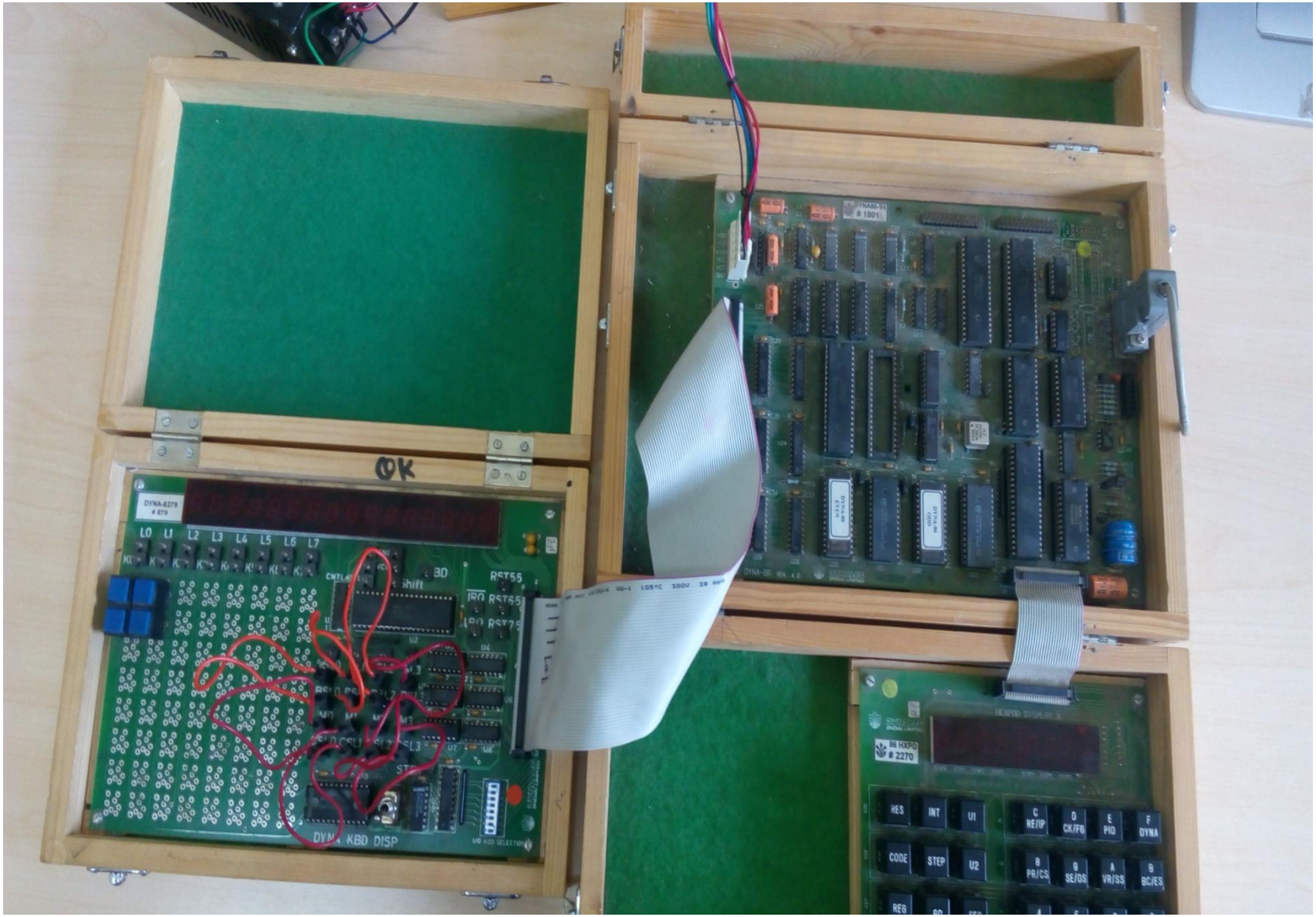
DELAY

```
0000:4444  MOV DX, FFFF
0000:4447  DEC DX
0000:4448  CMP DX, 00
0000:444B  JNZ 4447
0000:444D  RET
```

DATA

```
0000:1000  3E-
0000:1001  0A-
0000:1002  9A-
0000:1003  8E-
0000:1004  DC-
0000:1005  9A-
0000:1006  8E-
0000:1007  06-
0000:1008  00-
0000:1009  00-
0000:100A  00-
0000:100B  00-
0000:100C  00-
0000:100D  00-
0000:100E  00-
0000:100F  00-
```


KEYBOARD
8 Columns
8 Rows
SHIFT CNTL RL0–7
8259-IR0
D0–D7
RD
WR
RESET
CLK
A1
BHE
A0
8086/
8259
system
MN/MX
+ 5V
8279
S0–S3
CS
OUT B0–B3
OUT A0–A3
3:8 DECODER
S0–S2
S0–S3
4:16 DECODER
Select Display
BD
8 bit 7 Seg data
16 DIGIT DISPLAY UNIT
A0
A7
A6
A5
A4
A3
A2
A1
M/IO


OK
DYNA-8279
879
L0 L1 L2 L3 L4 L5 L6 L7
RST55
RST65
RST75
DYNA KBD DISP
1001
86 KXPD
2270
RES
INT
U1
CODE
STEP
U2
REG

8253 with 8086

- Use Counter 1.
- Input is given in BCD format.
- Execute all Modes.

- Answer:
  - **Command word format value = 51H (Mode 0)**

    (command word value will be changed for each mode)

For Dynalog KIT, Port Addresses are:

Counter 0= 30H

Counter 1= 31H

Counter 2= 32H

Command Word Register= 33H

Command Word format

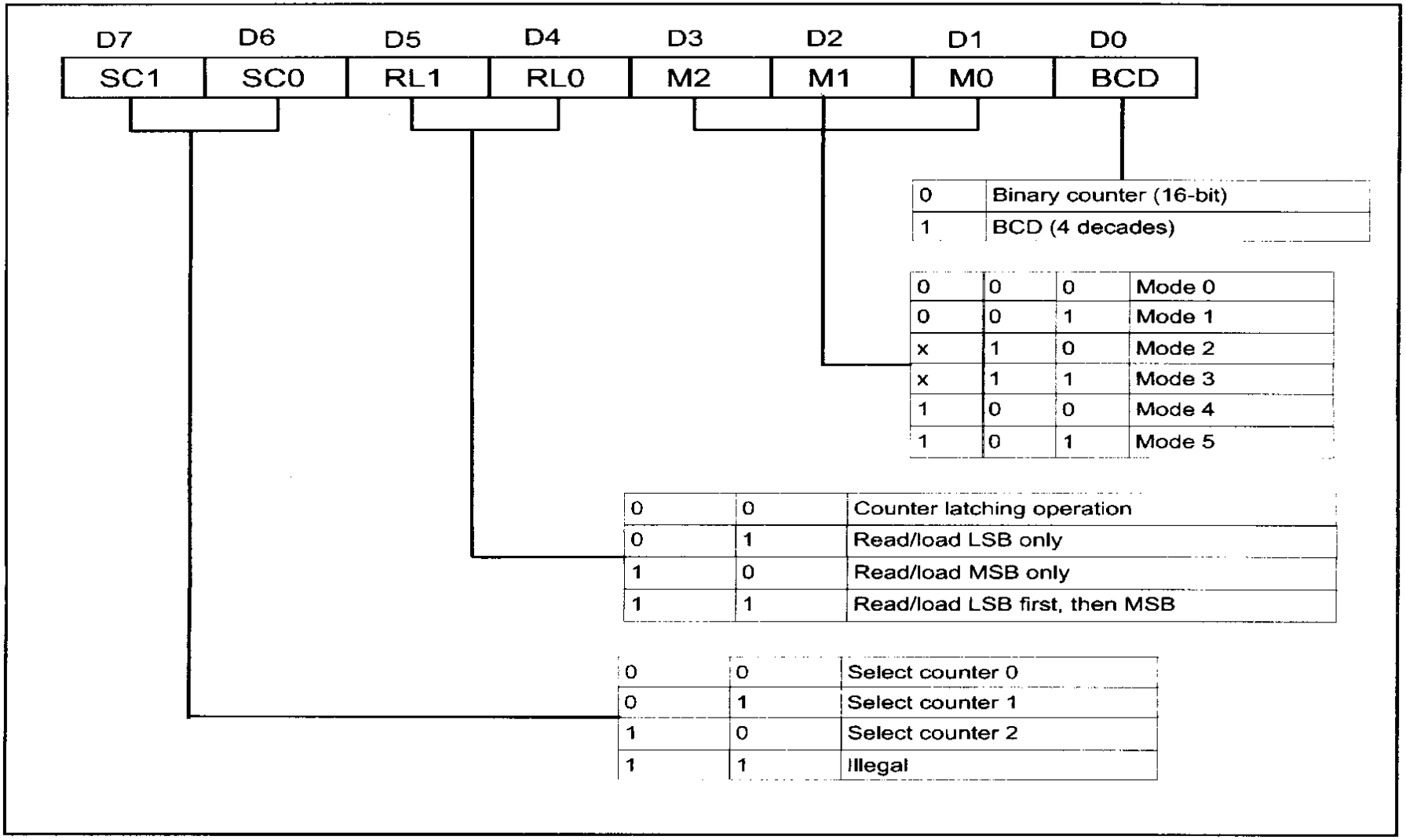
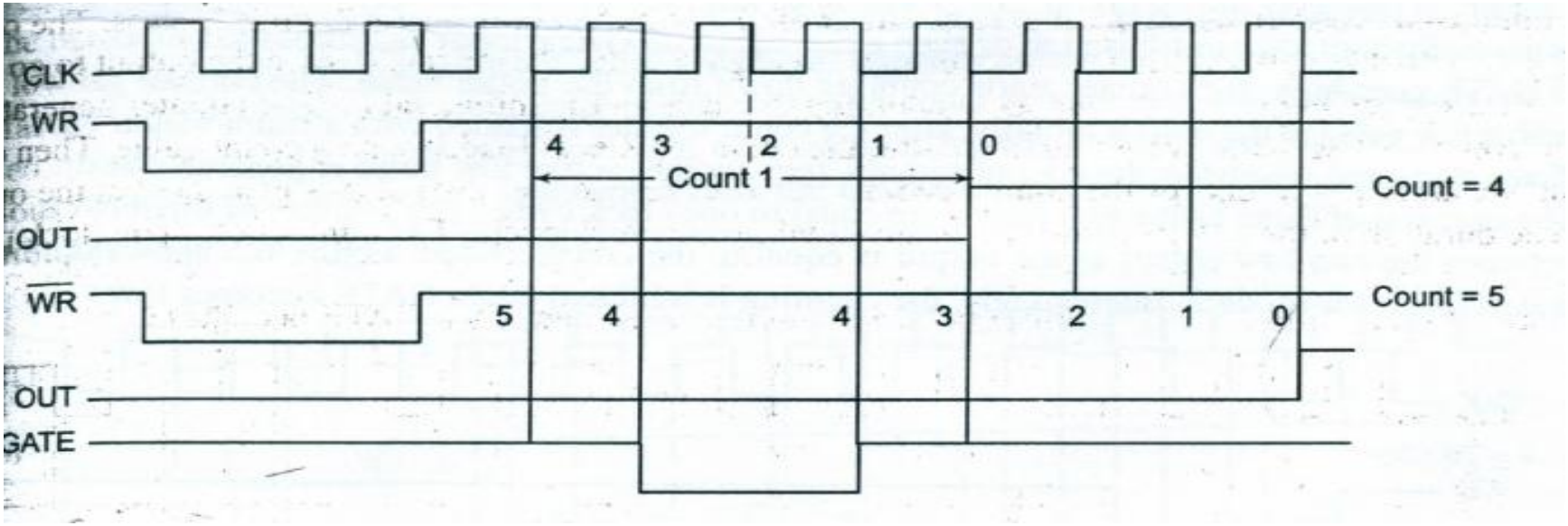


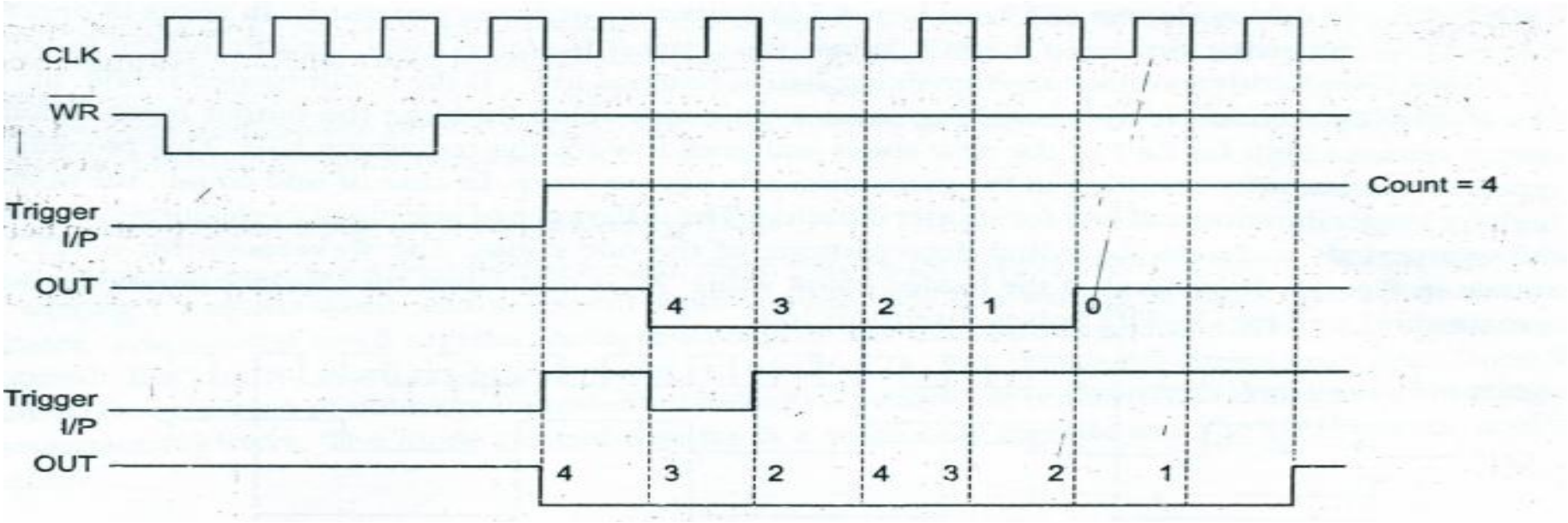
Figure 5-2. 8253/54 Control Word Format

Mode 0: Interrupt on terminal count



- Output is low initially when mode is set. Output is still low when counter value is loaded.
- Counter starts decrementing counter value after falling edge of clock.
- **When terminal count reached to zero, output goes high, and remains high till next mode of operation is selected.**
- This high output may be used to interrupt the processor whenever required.
- **This allow us to set timer, and count us to zero.**

Mode 1: Programmable one shot

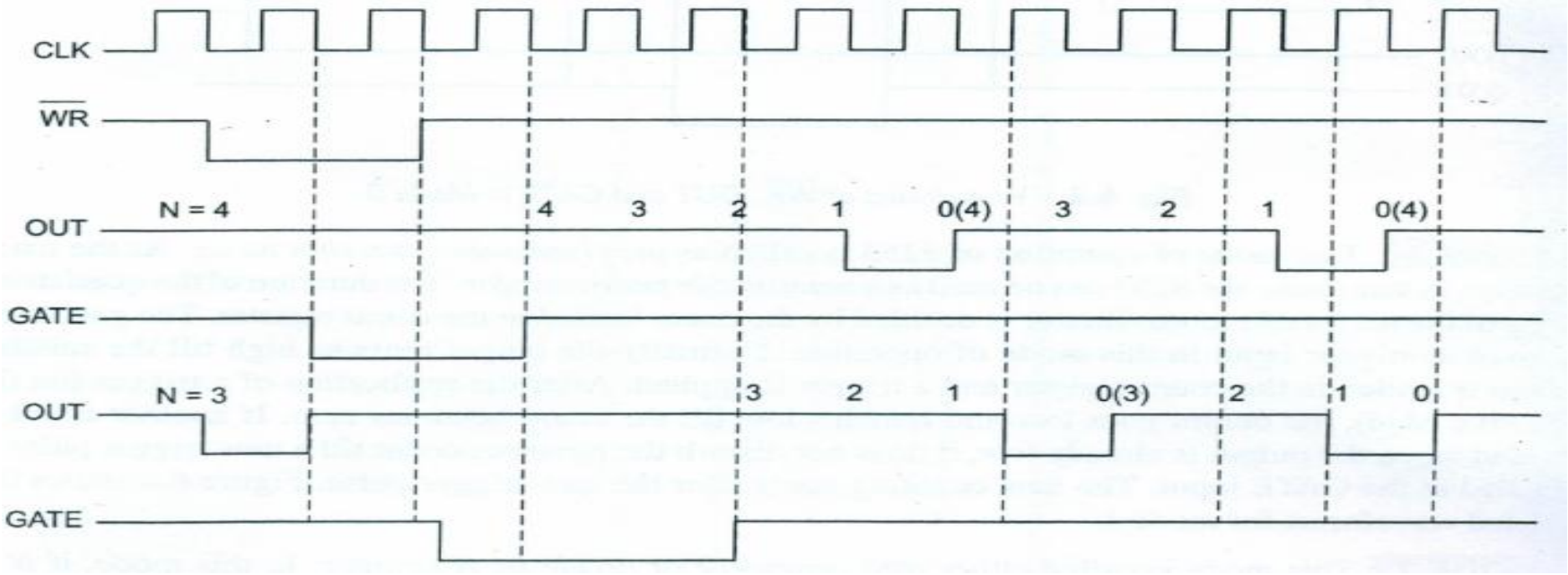


• It is also called as a **monostable multivibrator.** The duration The **duration of the Quasistable** of the Monostable Multivibrator **is decided by the count loaded in the count register.**

• **The gate input is used as trigger input in this mode.** Normally, the output remains high until the count is loaded and a trigger the output remains high until the count is loaded and a trigger is applied.

•It is used for **RAM refreshing.**

Mode 2: Rate generator



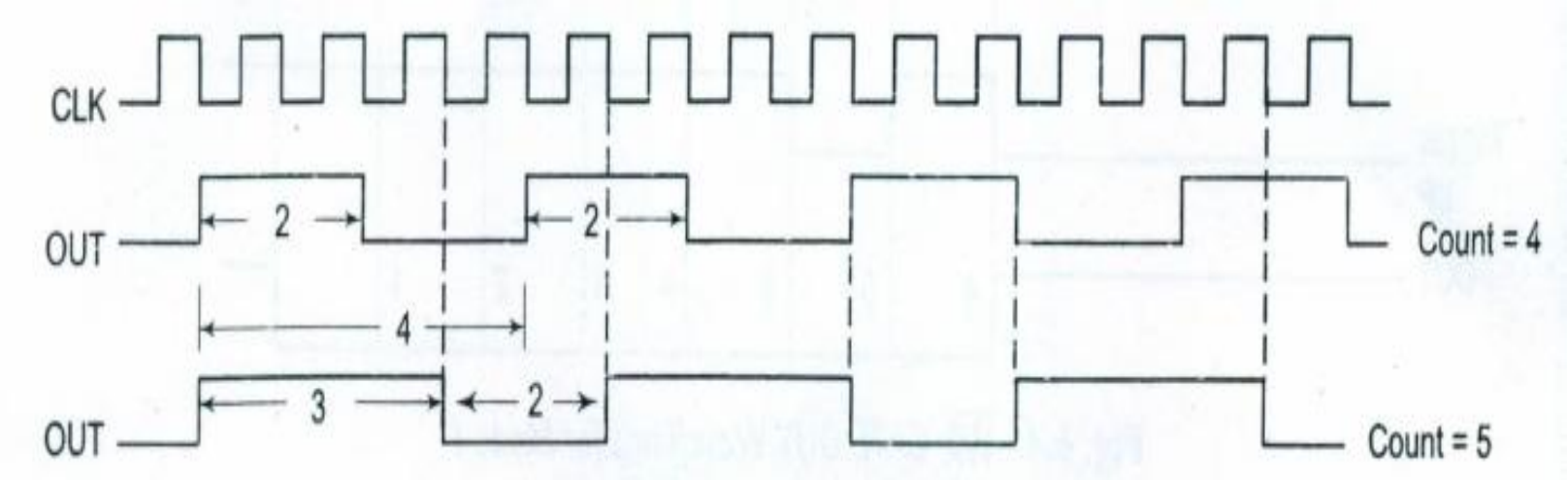
- The output is normally high after initialization.

- If N is loaded as the count value, after N pulses, **the output becomes low for one clock cycle (After N-1 clock cycles).**

- Whenever the count becomes zero another low pulse is generated at the output.

- It is most important mode of 8253.
- **Used to fire up interrupt at constant rate.**
- Used in setting of **system timer** for operating system.
- Also used for **special microcontrollers.**

Mode 3: Square wave rate generator



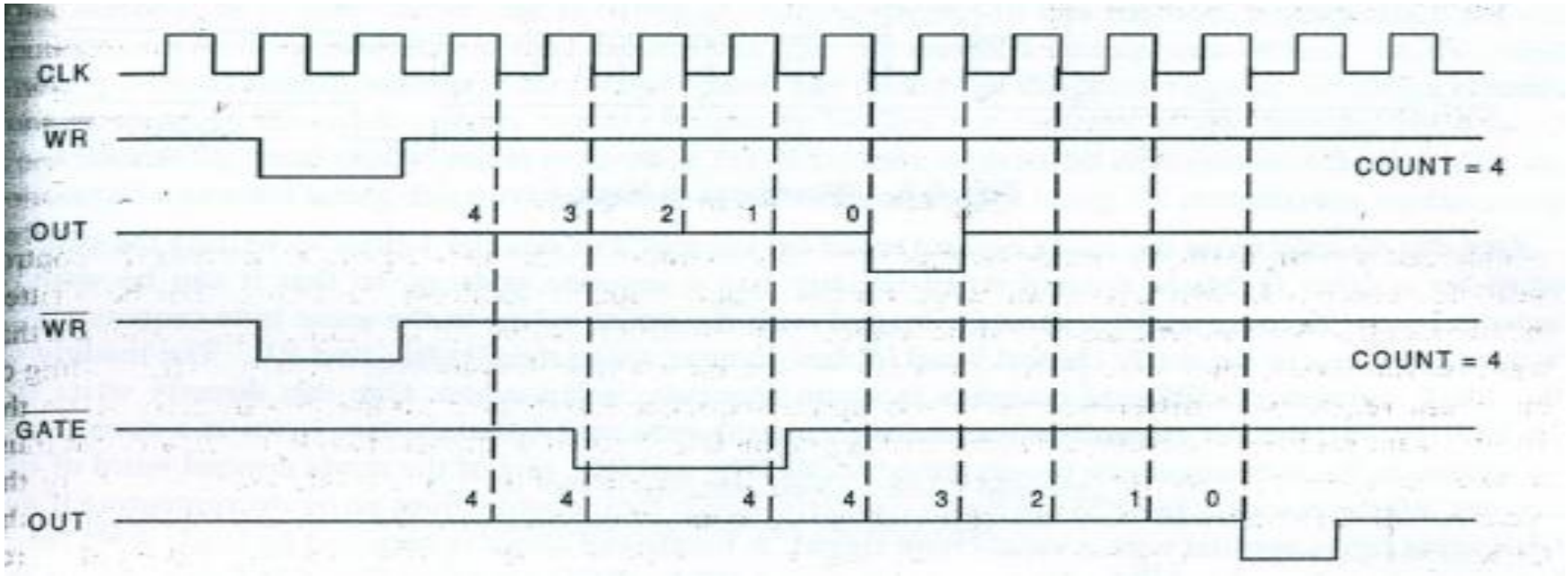
- It is similar to mode 2.

- When, the count N loaded is **EVEN**, half of the count will be high and half of the count will be low.

- When, the count N loaded is **ODD**, the first clock pulse decrements it by 1. Then half of the remaining count will be high and half of the remaining count will be low.

- It is **used to generate square waves.** Also **used by channel 3, which is connected to speaker.**

Mode 4: Software triggered strobe

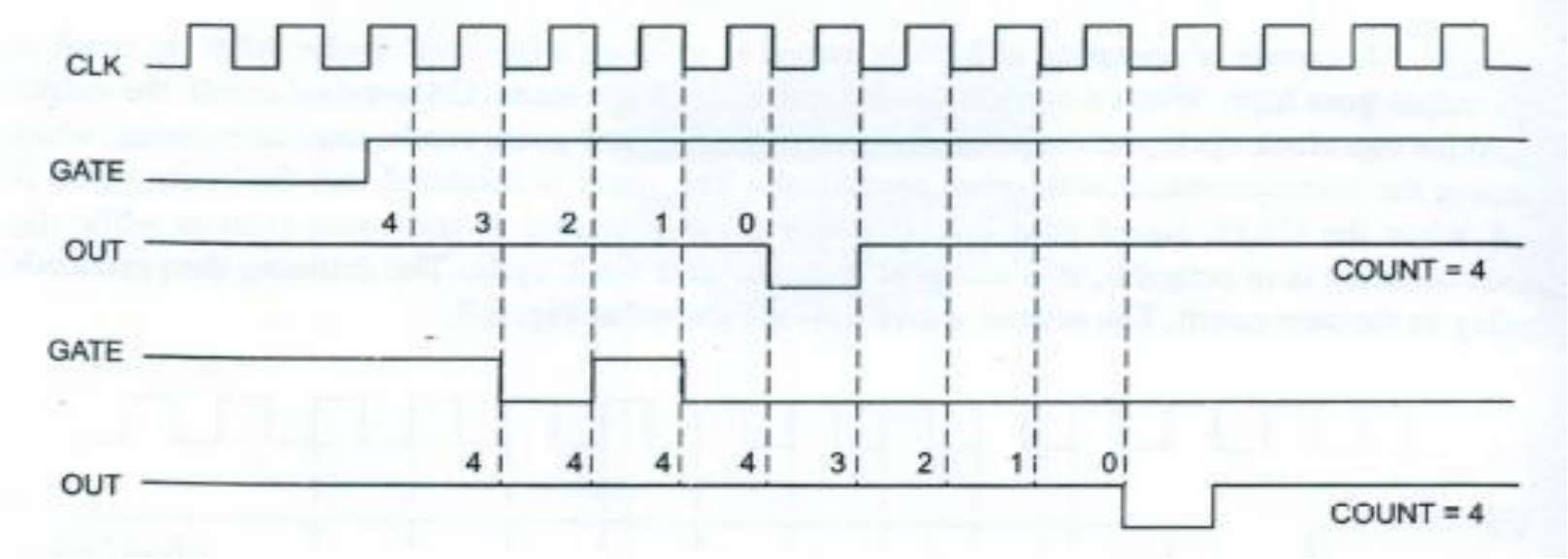


- After the mode is set, the output goes high.
- The **counter automatically begins to decrement** (count down) one clock

pulse after it is loaded with the initial value through software

- When the GATE signal goes low the count is latched. **On the terminal count, the output goes low for one clock cycle, and then again goes high. This low pulse can be used as a strobe.**
- **Used by special microcontrollers. Also used in 8279 to generate IRQ request.**

Mode 5: Hardware triggered strobe



- This **mode generates a strobe in response to an externally generated signal.**

- It is **similar to mode 4 except that the counting is initiated by a signal at the gate input,** i.e., it is hardware triggered instead of software triggered. After it is initialized, the output goes high.

- The counter starts counting after the rising edge of the trigger input (GATE). When the terminal count is reached, the output goes low for one clock cycle.

- **Used by special microcontrollers.**

MODE 0

Dyna-86>A 1000

0000:1000 MOV AL,51

0000:1002 OUT 33,AL

0000:1004 MOV AL,04

0000:1006 OUT 31,AL

0000:1008 INT 3

Dyna-86>G 1000

Break at FFFF:1008

MODE 1

Dyna-86>A 2000

0000:2000 MOV AL,53

0000:2002 OUT 33,AL

0000:2004 MOV AL,04

0000:2006 OUT 31,AL

0000:2008 INT 3

Dyna-86>G 2000

Break at FFFF:2008

MODE 2

Dyna-86>A 3000

0000:3000 MOV AL,55

0000:3002 OUT 33,AL

0000:3004 MOV AL,04

0000:3006 OUT 31,AL

0000:3008 INT 3

Dyna-86>G 3000

Break at FFFF:3008

MODE 3

Dyna-86>A 4000

0000:4000 MOV AL,57

0000:4002 OUT 33,AL

0000:4004 MOV AL,04

0000:4006 OUT 31,AL

0000:4008 INT 3

Dyna-86>G 4000

Break at FFFF:4008

MODE 4

Dyna-86>A 5000

0000:5000 MOV AL,59

0000:5002 OUT 33,AL

0000:5004 MOV AL,04

0000:5006 OUT 31,AL

0000:5008 INT 3

Dyna-86>G 5000

Break at FFFF:5008

MODE 5

Dyna-86>A 6000

0000:6000 MOV AL,5B

0000:6002 OUT 33,AL

0000:6004 MOV AL,04

0000:6006 OUT 31,AL

0000:6008 INT 3

Dyna-86>G 6000

Break at FFFF:6008

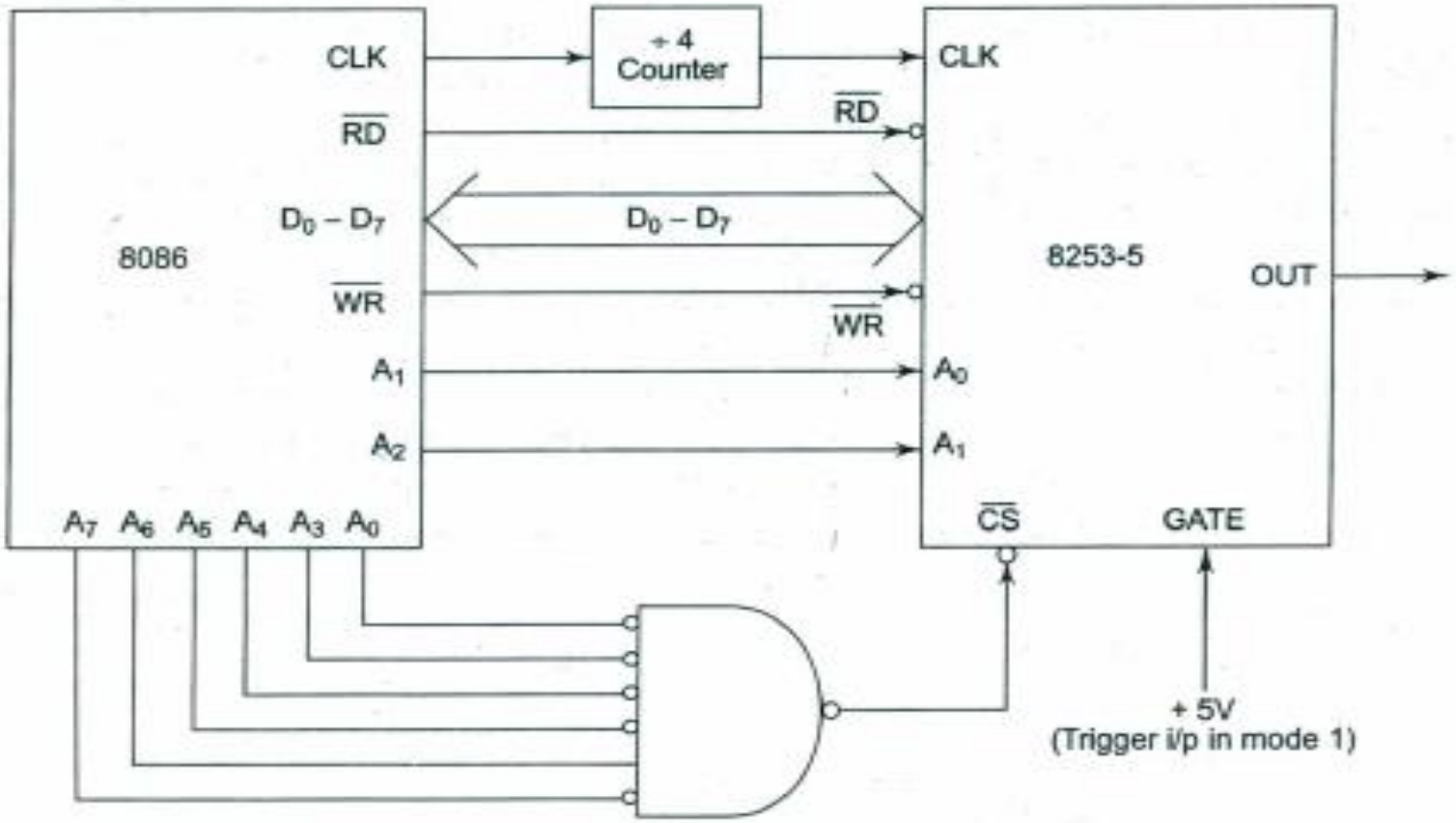


Fig. 6.10 *Interfacing 8253 with 8086 for Problem 6.1*


ok
750 PULSER 1.5
KHZ CLK0 MHZ
CLK0
PULSER KEY0
CLK1
PULSER KEY1
CLK2
VCC GATE0 GND OUT0
RST0
VCC GATE1 GND OUT1
RST1
VCC GATE2 GND OUT2
I/O ADDRESS SELECTION
DYNA-TIMER-STUDY CARD FOR 8253
RES INT U1
CODE STEP U2
REG GO SER
INH EXEC DCR
C RE/IP
D CK/FB
E PIO
F DYNA
8 PR/CS
9 SE/DS
A VR/SS
B BC/ES
4 IB/SP
5 RW/BP
6 OB/SI
7 OW/DI
0 EB/AX
1 EW/BX
2 BK/CX
3 DX

Problem

Design a programmable timer using 8253 and 8086. Interface 8253 at an address 0040H for counter 0 and write the following ALPs. The 8086 and 8253 run at 6 MHz and 1.5 MHz respectively.

(i) To generate a square wave of period 1 ms.
(ii) To interrupt the processor after 10 ms.
(iii) To derive a monoshot pulse with quasistable state duration 5 ms.

Solution

Neglecting the higher order address lines (A_{16}-A_8), the interfacing circuit diagram is shown in Fig. 6.10. The 8253 is interfaced with lower order data bus (D_0- D_7), hence A_0 is used for selecting the even bank. The A_0 and A_1 of the 8253 are connected with A_1 and A_2 of the processor. The counter addresses can be decoded as given below. If A_0 is 1, the 8253 will not be selected at all.

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
0	1	0	0	0	0	0	0	= 40H Counter 0
					0	1	0	= 42H Counter 1
					1	0	0	= 44H Counter 2
					1	1	0	= 46H Control word Reg.

(i) For generating a square wave, 8253 should be used in mode 3.
Let us select counter 0 for this purpose, that will be operated in BCD mode (may even be operated in HEX mode). Now suitable count is to be calculated for generating 1 ms time period.

$f = 1.5$ MHz,

$$\Rightarrow \quad T = \frac{1}{1.5 \times 10^{-6}} = 0.66\ \mu s$$

If N is the number of T states required for 1ms,

$$N = \frac{1 \times 10^{-3}}{0.66 \times 10^{-6}} = 1.5 \times 10^{3}$$

$$= 1500 \text{ states}$$

The control word is decided as below:

SC_1	SC_0	RL_1	RL_0	M_2	M_1	M_0	BCD
0	0	1	1	0	1	1	1

= 37 H

The ALP is given in Program 6.1.

```
CODE        SEGMENT
ASSUME      CS : CODE
START:      MOV AL,37H          ; Initialize 8253,
            OUT 46H,AL          ; counter 0 in mode3.
            MOV AL, 00          ; Write 00 decimal
            OUT 40H, AL         ; in LSB of count reg. and
            MOV AL, 15          ; 15 decimal in MSB as a
            OUT 40 H, AL        ; count.
            MOV AH,4CH
            INT 21H
  CODE      ENDS
            END START
```