UNIT I

If WAIT opcode , check if TS=1 and MP=1 if both are 1, which exception occur

A Exception 4

B Exception 5

C Exception 6

D Exception 7 ……

---------will be generated when the processor attempts to invoke the Page Fault service routine, and detects an exception other than a second Page Fault
A Double Fault ……

B Page Fault

C General Protection Fault

D All

--------is never IOPL-sensitive
A INT 13

B INT 3 ……

C INT 14

D INT 8

--------in the EFLAG register is found to be set at the end of an instruction, a single-step exception occurs.
A TF

B IF

C VM

D All

---------allows several debug control functions such as enabling the breakpoints and setting up other control options for the breakpoints.
A D0-D4

B D6

C D7 ……..

D All

Segmentation unit allows segments of _____ size at maximum.

a) 4Gbytes …….

b) 6Mbytes

c) 4Mbytes

d) 6Gbytes

INT 4 is also called as

A Divide error

B Interrupt on overflow …..

C Array bound check

D Page fault

General protection fault is also known as
A INT 11

B INT 12

C INT 13 ……..

D INT 14

WAIT instruction causes---------interrupt
A General protection fault

B Page fault

C Coprocessor error ……

D Segment not present

Which of the following instruction generate invalid TSS EXCEPTION?
A CALL

B JMP

C IRET

D All …….

A-------bit barrel shifter used to speed shift, rotate, multiply, and divide operations.

A 16

B 32

C 48

D 64 ….

Which of the following is input signal?

A CLK2 ….

B W/R#

C D/C#

D M/IO#

Which of the following is input signal?

A NA#

B READY#

C BS16#

D ALL …..

Which of the following is output signal?

A D/C#

B M/IO#

C LOCK#

D ALL …….

Which of the following is output signal?

A NA#

B READY#

C BS16#

D ADS

How many general purpose registers are available in 80386DX microprocessor

A 10

B 8

C 12

D 16

The instruction unit -------- the instruction opcode

A Fetch

B Decode ……..

C Execute

D All

Segmentation allows the managing of the ------- address space
A Linear

B Logical ……

C Physical

D All

Paging allows the managing of the ------- address space
A Linear

B Logical

C Physical ……

D All

Each segment is divided into one or more ……..K byte pages.

A 2

B 3

C 4 ……

D None

The base architecture include-------accessible segment
A 4

B 5

C6 ….

D7

------- hold the offset of next instruction to be executed
A EIP …….

B ESI

C EDI

D None

VM bit can be set by using ---------- instruction
A CALL

B RET

C IRET …….

D ALL

VM bit is unaffected by --------- instruction
A PUSH

B PUSHA

C POP

D POPF ……

The ------flag is used in conjunction with the debug register breakpoints.
A CF

B IOPL

C RF ……

D None

When ------ is set, it causes any debug fault to be ignored on the next instruction
A RF …….

B NT

C IOPL

D All

------- is set to indicate that the execution of this task is nested within another task.
A RF

B NT ……

C VM

D All

The value of------- in EFLAGS is tested by the IRET instruction to determine whether to do an inter-task return or an intra-task return.
A VM

B IOPL

C DF

D NT

Which of the following is 2 bit field in EFLAGS?
A VM

B NT

C RF

D IOPL ……..

Task switches can always alter the ------field of EFLAGS
A TS

B DF

C NT

D IOPL ……

Bit 11 of EFLAGS is also called as

A OF …..

B DF

C IF

D IOPL

Signed overflow occurs when the operation resulted in carry/borrow into the ------bit (high-order bit) of the result
A Carry

B Sign …
C Overflow

D All

Which of the following flag is used in string operation?
A OF

B CF

C DF ……..

D All

The ------- flag, when set, allows recognition of external interrupts signalled on the INTR pin.
A IF ……

B DF

C IOPL

D None

When ---- is set, the Intel386 DX generates an exception 1 trap after the next instruction is executed.
A IF

B TF …

C IOPL

D RF

The -------Flag is used to simplify the addition and subtraction of packed BCD quantities.
A CF

B PF

C ZF

D AF ……..

---------is a function of only the low-order eight bits
A PF ……

B AF

C OF

D All

Segment registers are ------- bit
A 16 ……

B 32

C 48

D 64

In Real Address Mode, the maximum segment size is
A 4KB

B 4GB

C 64KB ……

D None of these

The selectors in DS, ES,FS indicate the current data segments.
A DS

B ES

C FS

D All …..

The low-order ----- bits of CR0 are also known as the Machine Status Word
A 8

B 16 ….

C 32

D All

The ----- bit is set to enable the on-chip paging unit.
A PG ……..

B PE

C CR0

D All

Bit ----- of CR0 is also called as task switch
A 1

B 2

C 3 …..

D 4

--------is automatically set whenever a task switch operation is performed
A NT

B TS ……..

C PE

D All

If TS is set coprocessor causes -------- exception
A 5

B 6

C 7 …….

D 13

The -------- coprocessor bit is set to cause all coprocessor opcodes to generate a Coprocessor Not Available fault
A TS

B EM ……..

C MP

D All

The WAIT opcode is not affected by the ------bit setting.
A EM ……..

B TS

C MP

D PE

The ------ bit is set to enable the Protected Mode.
A EM

B TS

C MP

D PE ……

-------- holds the 32-bit linear address that caused the last page fault detected.
A CR0

B CR1

C CR2 …..

D CR3

-------contains the physical base address of the page directory table.

A CR0

B CR1

C CR2

D CR3 ……..

A task switch through a TSS which changes the value in

A CR0

B CR1

C CR2

D CR3 …..

UNIT II

------- equals the privilege level of the code segment being executed
A RPL

B CPL …….

C EPL

D DPL

CPL can also be determined by examining the lowest 2 bits of the --------register
A CS …….

B SS

C DS

D All

One instance of the execution of a program

A Task

B Process

C Program

D Both A & B ……

The GDT can contain any type of segment descriptor except
A LDT

B Call gate

C Task gate

D Interrupt …….

LDT may contain only
A Code

B Data

C Stack

D All

IDT may contain only
A Interrupt gate

B Trap gate

C Task gate

D All …

If P=0 then any attempt to access this segment causes ---------
A Exception 13

B Exception 11 ……..

C Exception 4

D Exception 7

When C = 1 Code segment may only be executed when ---------
A CPL<=DPL

B MAX(RPL,CPL)<=DPL

C CPL >= DPL ……

D All

System segments describe information about

A OS table

B Tasks

C Gates

D All ……..

Type 2 descriptor is also called as

A LDT ……..

B Task gate

C TSS

D Call gate

Which of following is system descriptor?

A Code

B Stack

C Data

D TSS

I/O instructions can be unconditionally performed when --------
A CPL <= IOPL …….
B CPL >= IOPL
C CPL = IOPL
D Never check for privilege level

When CPL >IOPL, and the current task is associated with a 286 TSS, attempted I/O instructions cause an ------ fault
A exception 13 …….
B exception 12
C exception 11
D exception 14

“IOPL-sensitive'' instruction

A CLI ……..

B LTR

C LOCK

D CLD

Privilege level transitions can only occur via

A Gates …….

B CALL

C JMP

D RET

--------may also be set or cleared by POPF or IRET instructions.
A NT ……..
B TS
C MP
D PE

Find invalid statement:
When a CALL or INT instruction initiates a task switch
A The new TSS will be marked busy

B The back link field of the new TSS set to the old TSS selector

C The NT bit of the new task is reset by CALL or INT initiated task switches. …….

D An interrupt that does not cause a task switch will clear NT.

The virtual 8086 environment is only entered and exited via -------
A CALL

B RET

C IRET

D Task switch ……

The upper 10 bits of the linear address (A22-A31) are used as an index to select the correct -------
A Page Directory Entry ……..

B Page Table Entry

C Page Frame Entry

D All

Each Page Table is --------K bytes

A 2

B 4 ……..

C 16

D 64

-------will hold the linear address which caused the page fault
A CR0
B CR1
C CR2 …….
D CR3

All Virtual 8086 Mode programs execute at privilege level ---------
A 0

B 1

C 2

D 3 ……..

I/O instructions do not go through the segmentation

A True …….

B False

The ------- I/O address space refers to physical memory rather than linear address
A 4k
B 16k
C 32K
D 64K …….

In Protected Mode, the interrupt vectors are -------- byte quantities

A 2
B 4
C 8 ……..
D None

In Real Mode, the interrupt vectors are -------- byte quantities
A 2
B 4 ……..
C 8
D None

INT 14---------- is also called as

A Page Fault ……

B General Protection Fault

C Segment Not Found

D Coprocessor Not Available

GDTR is ------- register

A 16

B 32

C 48 ….

D 64

IDTR is ------- register

A 16

B 32

C 48 ……..

D 64

LDTR is ------- register

A 16 …..

B 32

C 48

D 64

TR is ------- register

A 16 ….

B 32

C 48

D 64

-------- bit is set before a write operation to the page is carried out

A D …….

B P

C A

D U/S

The ----- register hold 16 bit selector for LDT

A LDTR …….

B IDTR

C GDTR

D TR

Which of the following is/are task specific segment(s)?

A GDTR

B LDTR

C TR

D Both B & C

The Debug Control Register ----is used to set the breakpoints
A DR5

B DR6

C DR7 ……

D DR0-DR3

The Debug Status Register is also called as
A DR5

B DR6 ……

C DR7

D DR0-DR3

……is the data register which contains the data of the Translation Look aside buffer test.
A TR7

B TR6

C Both

D None

The registers can be accessed only when the current privilege level is zero.
A GDTR

B LDTR

C TR

D All

80386 support which type of descriptor table from the following?

a) LDT

b) GDT

c) IDT

d) ALL ……

Virtual Mode Flag bit can be set using ____ instruction or any task switch

operation only in the _____ mode

a) IRET, Virtual

b) POPF, Real

c) IRET, protected ……..

d) POPF, protected

The ___ bit decides whether it is a system descriptor or code/data segment descriptor

a) P

b) S ……

c) D

d) G

The interrupt vector table of 80386 has been allocated _____ space starting from

_____ to _____.

a) 1Kbyte, 00000H, 003FFH ……

b) 2Kbyte, 10000H, 004FFH

c) 3Kbyte, 01000H, 007FFH

d) 4Kbyte, 01000H, 009FFH

UNIT III

If _____input pin of 80386 if activated, allows address pipelining during 80386

bus cycles.

a) BS16

b) NA ……

c) PEREQ

d) ADS

-------- input allows another bus master to request control of the local bus.
A HOLD

B LOCK#

C BOTH A&B

D NONE

After a bus idle state, the processor always uses --------address timing
A Pipelined

B Non-pipelined ……..

C Both

D None

If the cycle is a write, data signals are driven by the Intel386 DX beginning in ---------
A Phase two of T1 …….

B T1

C T2

D Phase 1 of T2

In non-pipelined bus cycle with one wait state READY# is sampled asserted at---------
A T1

B First T2

C Second T2 …….

D Both B & C

Identify the bus state when READY asserted, HOLD negated, Request pending internally

A T1 …….

B T2

C Ti

D Th

Identify the bus state when READY# negated and NA# negated

A T1

B T2 ……

C Ti

D Th

What is the bus state of READY asserted, HOLD negated and no request pending

A T1

B T2

C Ti ……

D Th

Bus state Th goes to ----- ----state when hold negated request pending

A T1 ……

B T2

C Ti

D Remain in Th

When wait states are added and you desire to maintain non-pipelined address timing, it is necessary to negate ------- during each T2 state except the last one
A NA# ….

B READY#

C BS16#

D All

The ------ input is sampled at the end of every phase one, beginning with the next bus state, until the bus cycle is acknowledged
A NA# ….

B READY#

C BS16#

D ADS

-------is/are only required in a bus cycle performing a transition from non-pipelined address into pipelined address timing
A T1

B T2

C T2P

D All ……

The state of ---- distinguishes the first and second interrupt acknowledge cycles.
A BE0-BE1

B BE2-BE3

C A2

D A3

-------are the only signals distinguishing shutdown indication from halt indication
A BE0#,BE1#

B BE1#,BE2#

C BE0#,BE2# ……..

D BE2#,BE3#

Shutdown state drive an address of---------

A 0 ……

B 1

C 2

D 3

Halt state drive an address of---------

A 0

B 1

C 2 ……

D 3

UNIT IV

Which of the following instruction is available only at level 0?

A WAIT

B LDTR ……..

C SLDT

D All

80386 support overall ___ addressing modes to facilitate efficient execution of higher level language programs.

a) 9

b) 10

c) 11 …….

d) 12

The Intel386 DX has a -----byte instruction queue
A 8

B 16 …….

C 32

D 64

The Intel386 DX provides a total of ------- addressing modes for instructions
A 8

B 9

C 10

D 11 …..

The operand is included in the instruction as part of the opcode, that addressing mode is called as

A Resister Operand Mode

B Immediate Operand Mode ……..

C Direct

D All

The effective address is calculated by using
A Displacement

B Base

C Index

D All ….

Scaled index mode is especially useful for accessing
A Array

B Structure

C Both

D None

MOV [ECX], EDX this instruction is based on ------- addressing mode
A Direct

B Resister ……

C Index

D None

MOV ECX, [EAX+24]
What is the addressing mode used for above instruction

A Resister indirect

B Base Mode ……

C Direct

D Relative

Which of the following is base register?
A BX

B BP

C AX

D Both A & B ……

Which of the following is index register?
A SI

B DI

C SP

D Both A & B ……

----------the only instruction forms where the LOCK prefix is legal on the Intel386 DX
A XCHG

B ADD

C AND

D MUL ……

---------is especially useful for implementing semaphores or similar data structures for process synchronization
A XCHG

B ADD

C XLAT

D All

Which of the following operate only on data in the EAX register?

A CBW

B AAA

C CDQ

D POP ……..

--------automatically fill the extra bits of the larger item with the value of the sign bit of the smaller item
A CBW

B CWD

C CDQ

D All …….

Which of the instruction is used for unpacked BCD adjustment?
A DAA

B DAS

C AAA ……

D All

--------instruction is provided to force the RPL bits to the originator's CPL
A CLI

B ARPL ……..

C LTR

D None