Assignment - 6

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Problem statement :-

Write an ALP to read & display the table content pointed by GDTR/LDTR & IDTR.

Objective :-

To understand how to read & display contents of LDTR, GDTR, IDTR.

Outcome :-

Students will study different descriptor tables in system also different registers associated with it.

Theory :-

GDTR :- It is a 48 bits long it stores 32 bit base address of the global descriptor table & 16 bit limit of that table.

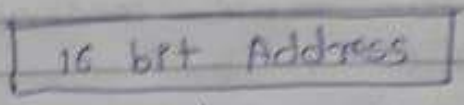
IDTR :- This register also holds 32bit base address of interrupt descriptor table & 16-bit limit of the same.

32 bit Base Address	16 bit limit

GDTR/IDTR Architecture.

LDTR/TR-LDTR is used to store base address of local descriptor table it is 16 bits long.

TR is task register it stores address of TSS descriptor. It is also 16 bits long.



LDTR/TR Architecture

MSW - It is 16 bits long. The machine status word, contains bits to define

1) PG (Paging)
2) ET (Extension Table)
3) TS (Task Switched)
4) EM (Emulate Coprocessor)
5) MP (Math Present)
6) PE (Protection Enable)

others are reserved bits.

Steps

1) Use instructions like
   1) SGDT 2) SIDT 3) SLDT
   4) STR 5) SMSW.

SLDT : Store local descriptor table register the instruction stores the values in the source to the global interrupt descriptor table.

STR : It stores the 16 bit value of task register in given operand.

SMSW : Stores 16 bit MSW in given operand.

Testcase :-

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GDTR    is  ff 52 3020 : 007f
LDTR    is  0000
IDTR    is  ff 57c000 : 0fff
TR      is  0040
MSW     is  0033
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Conclusion :-

Thus we printed the values present in GDTR, IDTR, LDTR, TR, MSW.