1.Barrel shifter is used to speed up which of the following operations?

A)Shift B)Rotate C)Multiply,Divide D)ALL

Ans :- D

2.Multiply and divide logic uses which algorithm?

A)1-Bit per cycle B)2 -Bit per cycle C)8 -Bit per cycle D) 32-Bit per cycle

Ans :- A

3.Each task on 80386DX can have a maximum of _____ segments of up____ size.

A) 16380, 1GB B) 16381, 4GB C) 16381, 1MB D) 16830, 4KB

Ans :- B

4.8086 has _____ bit address lines.

A) 32 B)20 C)16 D)8

Ans :- B

5.The VM bit can be set in _____ mode by _____instruction.

A)Real, INTO B) Protected, IRET C) Protected ,JMP D) None

Ans:- B

6.VM bit is unaffected by_____instruction.

A)PUSHF B)POPA C)POPF D)IRET

Ans:- C

7.Which instruction can alter IOPL field when executed at CPL=0

A)IRET,POPF B)PUSHF,POPE C)IRET, PUSHF D)CALL,POPF

Ans:- A

8.The ____flag when reset doesn't allow recognition of external interrupts signalled on ___ pin

A)IF,INTR B)DF,INTR C)IF,NMI D)None

Ans:- A

9.When TF is ____ exception 1 traps occur only as a functions of breakpoint address loaded into debug register.

A)Set, DRO B)Set DRO-DR 3 C)Reset DRO D)Reset DRO-DR3

Ans:- D

10.The auxiliary flag is used to simplify operations of_____quantities.

A)Packed hexadecimal B)Packed Binary C)Packed BCD D)None

Ans :- C

11.In real mode maximum segment size is fixed at _____

A)2^16 bytes B)2^20 Bytes C) 2^32 Bytes D)2^8 Bytes

Ans:- A

12.The lower order _____ bits of CRO are also known as____ for compatibility with _____protected mode.

A)8,MSW,8086 B)16 LMSW, 80386 C)32, MSW 80386 D)16 MSW 80286

Ans :- D

13.The EM bit in CRO is set to generation _____fault i.e exception _____

A)Coprocessor not available, exception 13

B) Coprocessor available, exception 8

C) Coprocessor not available, exception 7

D) Coprocessor available, exception 7

Ans :- C

14. The WAIT opcode generates a trap when_____

A)MP= 1 TS =1 B)MP=0 TS =0 C)MP=1 TS =0 D)MP=0 TS= 1

Ans:- A

15.For strict 80286 compatibility, PE bit cannot be reset by____ instruction.

A)LMSW B)SMSW C)both A&B D)None

Ans :- A

16.The intel 386 DX page directory table is always ____ KB page aligned.

A)8KB B)4KB C)16KB D) 32KB

Ans:- B

17.DR 7 is used the breakpoint and DR 6 is used to ____the state of breakpoint.

A)Display, Set B)Display, Display C)Set, Display D)Both A&B

Ans:- C

18.TR 7 is the data register which contains the data of _____

A) Translation look aside buffer list B)GDT C)IDT D)None

Ans:- A

19.80386 DV has _____cache.

A)Level 1 B)Level 2 C) Level 3 D) Level 4

Ans :- B

20. TR 6 is

A)Instruction test register B) Command test Register C) A&B D) None

Ans :-

21.Page fault line as address is present in _____

A) CRO B) CRI C) CR2 D) CR 3

Ans:- C

22.Frequency range is _____

A)5-10 MHZ B)6-10 MHZ C)1-2 MHZ D)None

Ans:-B

23.In 80386 _____prefeched instruction are these

A)4 B)8 C)6 D)2

Ans :- C

24.Prefeching depends on_____

A)Barrel Shiftes B) Instruction C)Memory D)Buffer

Ans :- D

25.Fetching is done in_____

A)EU B)CPU C)BIU D)ALL

Ans :- C

26.RPL is detected by : least _____ bits of selector

A)4 B) 2 C) 8 D) 1

Ans:- B

27.Each description table can hold upto _____descriptors of_____bytes

A) 8190, 4 B)8194,8 C) 8192, 8 D) 8100 ,16

Ans :- C

28. The upper ____bits of selector are used as an index to the description table

A)16 B)2 C) 3 D)13

Ans:- D

29. The GDT does not contain_____ descriptions.

A)TSS B) Call Gate C) LDT D) Interrupt &crap

Ans:- C

30. Word count is present in ____and the size of word count is _____.

A)Call Gate ,4 Bits B) LDT ,16 Bits C) Trap Gate ,4 Bits D) TSS, 4 bits

Ans:- A

31.TSS descriptor is present in ____

A)GDT B)LDT C)IDT D) Both A& B

Ans:- A

32.Types used in i 386 _____

A) Type C B)Type E C)Type F D)ALL

Ans:- D.

33.First entry of GDT is_____

A)Offset B)LDT C) NULL D)Descriptor

Ans:- C

34.S= 1 ,E=0 X=0 R/W=1 Which segment does it describe ?????

A)Code, Executable, read only ,Downward

B) Code, Executable, read write ,upward

C) Data , Executable, read only ,upward

D) Code, Executable, read-write ,upward

Ans:- D

35.Total no of descriptor in descriptor table are _____-

a) 13 B) 2^13 C)<=2^13

Ans: c

36. In a maximum size segment, the lowest 12 bits of the segment base should be

a)all 1's b)all 0's c)0 or 1 d)None

Ans)b)

37. If B=1 in a descriptor, then the PUSH ,POP, CALL use:

a)32bit ESP register b) 16 bit SP register c)both a &b d) NONE

ans) a

38. System descriptors contain _____bit linear address & _____bit segment limit.

a)16,8b)32,20c)20,32 d)8,16

ans)b

39.DPL firld is ignored in ____ descriptor.

a)LDT b)GDT c)IDT d)NONE

ans) a

40.. IF bit is reset by:

a)trap gate b)call gate c)TSS d)Interrupt gate

ans)d

41.IOPL sensitive instructions in protected mode are:

a)CLI b) STI c)LOAD STORE d)Both a and b

ans)d

42.the limit of intel 386DX should be grater than

a)002h b)000bh c)0064bh d)ffffh

ans)c

43. After enabling protected mode, the _____instruction id used to load theCS register.

a)jmp b)call c)wait d)iret

ans) a

44. The page directory is ___bytes long and has ___ max entries.

a)8k,512 b)8k,1024 c)4k,1024 d)4k,1024

Ans)c

45.U/S=1,R/W=1 which P.L. are permitted to access?

a)0,1 b)1,2 c)3 d)0,1,2,3

ans)d

46. The paging hardware allows _ bit linear address produced by virtual mode program to be divided upto __pages.

a)32,256 b)16,512 c)32,512 d)20,256

ans) d)

47. Instructions applying to multitasking if attempted to use in real or virtual mode generates

a)exception 6 B)interrupt 13 c)interrupt 8 d)exception 4

ans) a

48. Virtual 8086 mode is entered by executing an ___instruction at CPL=__

a)IRET,2 B) INT,0 C)IRET,0 D)BOTH A & C

ans) c

49. TLB cache holds recent ___entries of page tables.

a)16 b)8 c)20 d)32

ans) d

50. A confirming code segment takes the P.L of the _____instruction due to which the segment was executed.

A)jmp,call b)call,wait c)je, call d)NONE

ANS)a

51. _____provides the fundamental timing for 386DX

a)clk b)clk2 c)both a and b d)none

ans) b

52.BE0# applies to

a)D0-D7 b)D8 –D15 c) D16-D23 d_D24-D31

ans)a

53.BE1# applies to

a)D0-D7 b)D8 –D15 c) D16-D23 d_D24-D31

ans)b

54.BE0# applies to

a)D0-D7 b)D8 –D15 c) D16-D23 d_D24-D31

ans)c

55.BE0# applies to

a)D0-D7 b)D8 –D15 c) D16-D23 d_D24-D31

ans)d

56. When a I/O cycle is in progress, operand being transferred occupies only ___bits of data bus.

a)2 b)8 c)16 d)32

ans)c

57.HALT has address ___

a)0 b)1 c)2 d)3

ans)c

58. SHUTDOWN has address ___

a)0 b)1 c)2 d)3

ans) a

59. the ____bus signals affect HALT and SHUTDOWN operations.

a)BE0#,BE1# b) BE0#,BE3# c) BE0#,BE2# d)ALL

ans)c

60. ___is ignored on the first bus state of all bus cycles.

a)wait b)lock#c)ads#d)ready#

ans)d

61. Ready# must always meet setup and hold times ___&___for correct operation.

a)t19,t20 b)t17,18 c)t20,t21 d)t30,t31

ans)a

62.BS16# must always meet setup and hold times ___&___for correct operation.

a)t19,t20 b)t17,18 c)t20,t21 d)t30,t31

ans)b

63. HOLD must remain ___as long as any other device is a local bus muster.

a)asserted b)negated c)don't care d)NONE

ans)a

64. If both reset and hold are asserted then ___has higher priority

a)hold b)ready c) Equal priority to both d)none

ans)b

65.in hold acknowledge state, _____is the only signal being driven by 386DX while other signals are in high impedance state.

a)hold b)ready c)wait d)hlda

ans)d

66. At the end of the second interrupt acknowledge bus cycle, INTR latches __bit interrupt vector on ___to identify the source of interrupt.

a)8,D0-D7 b)16,D0 –D15 c) 32,D0 –D31 d) ALL

ans)a

67.During reset,, __has high impedance.

a)ads# b)be0# c)w/r# d)D0-D31

ans) d

68. The shortest time of bus activity is:

a)bus cycle b)bus state c)data cycle d)None

ans)b

69.T2 states are repeated indefinitely if _____is not asserted.

a)hlda b)ready# c)bs16# d)none

ans)b

70. When ready# is asserted , data bus pins should be at ___logic state at end of each read cycle.

a)0 b)0 or 1 c)1 d)don't care

ans)b

71. BS16# is asserted implies operation is ___bit

a)16 b)32 c)20 d)both a and c

ans)a

72. _____must be negated to allow recognition of asserted _____in final T2 state.

a) na# ,bs16# b)bs16#,NA# c) NA# ,ready # d) ready#,NA#

ans)a

73. Once a pipelined addresss cycle is in progress, them pipelined timing is maintained in by ___ signal

a) asserting NA#

b)negating NA#

c) asserting READY#

d)negating READY#

ans)a

74. The processor can go in T1P state only from ___state.

a) T2P b)T1 c) T2 d) Ti

ans) a

75. Which of the following transisiton always takes place

a)T1-> T2I b)T1P->T2 c) Ti->T1 d)T1->T2

ans)d

76.)Which instruction does not require LOCK prefix to lock it?

a) call b)wait c)XCHG d) jmp

ans)c

77. Which instruction after execution transfers the control back to the program from where it was called?

a)je b)jmp c) Call d) wait

ans)c)

78. Addressing mode used by wait instruction?

a)implied b) direct c) register d)all of the above

ans)a

79. INT 4 is implicitly also known as

a)iret b) into c) int d) int 13

ans)b

80. Which instruction is associated with the busy pin:

a)call b)jmp c) int d) wait

ans)d

81. DIV instruction takes how many operands.

a)1 b)2 c)3 d)all

ans) a

82. Sign flag sets. Which instruction from the following will cause a program control jump.?

a)js b)jns c)jz d)none

ans)a

83. AAA converts the result of the addition to

a)hexadecimal b) Decimal c) BCD d) Octal

ans) c

84. Test instruction

a)is same as cmp

b)does logical anding

c)tests the operands

d)does logical anding and does not not store the result.

Ans)d

85. Execution of an ALP takes place in the following way:

a)linking, assembling,output

b)linking,output

c)assembling, linking,output

d)none of the above

ans)c

86.To access control registers ___instructions are defined.

a)load b)store c)both a and b d)none

ans)c

87.All intel 386DX instructions operate on ____operands

a) 0 b)0,1 b)0,1,2 d)0,1,2,3

ans)d

88. A packed BCD stores each didgit in

a)one bit b)a nibble c) one byte d)none

ans)b

89. Which of the following is protected mode specific instruction?

a)mov b)add c)lmsw d)none

ans)c

90. HLT instruction uses ____addressing mode.

a)implied b)register c)direct d) ALL

ans) a

91. When STI is used

a)IF=1 b)IF=0 c)IF=don't care d)None

ans)a

92. _____is always undefined following shift operation.

a)IF b)VM c)DF d)AF

ans)d

93.__flags will always be cleared by logical instructions.

a)OF, CF b) AF, CF c) VM, DF d) NT, CF

ans)a

94. The source cannot be a _____when usind LDS instruction

a)register b) operand c) memory location d) None

ans) a

95. ____ instruction is basically related to communication with I/O devices

a)add b) mov c)IN c)sub

ans)c

96.in POPA the first register to popped is :

a)ebp b)esi c)eax d)edx

ans)d

97.in PUSHA the first register to popped is :

a)ebp b)esi c)eax d)edx

ans)c

98. To load/store test register, _____addressing mode is used.

a) Register b) Memory c) direct d)implied

ans) a

99.The value in eax register for exit system call(32 bit) is:

a)0 b)1 c) 2 d)4

ans)b

100. The value in eax register for write system call(32 bit) is:

a)0 b)1 c) 2 d)4

ans)d