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UNIT 3

1. What are the different levels of security in 80386 ?

a. Task level security
b. Page level security
c. Segment level security
d. Both b & c

Answer : d

2. The mechanism that is executed at certain privilege levels, determined by CPL (Current Privilege Level) and I/O privilege level (IOPL) is

a) restricted use of segments
b) restricted accesses to segments
c) privileged instructions or operations
d) none of the mentioned

Answer : c

3. Which is the highest and most secure privilege level in 80386 ?

a. Privilege Level 0
b. Privilege Level 1
c. Privilege Level 1
d. Privilege Level 2

Answer : a

4. What is the privilege level of Kernal in Operating System ?

a. Privilege level 2
b. Privilege level 1
c. Privilege level 3
d. Privilege level 0

Answer : d

5. What fields are checked by Privilege check unit of CPU ?

a. CPL
b. RPL
c. DPL
d. All of the above.

Answer : d

6. IF flag get affected when

a. CPL >= IOPL
b. CPL>=RPL
c. CPL<= IOPL
d. CPL<=RPL

Answer: c

7. CPL of microprocessor is

a. DPL of data segment
b. DPL of stack segment
c. DPL of Current Code segment
d. DPL of previous code segment

Answer : c

8. To change I/O permission, you must be running at privilege level

a. CPL>DPL
b. CPL<DPL
c. CPL<RPL
d. CPL=0

Answer: d

9. Limit field in Code/Data Segment descriptor is of length

a. 8 bits
b. 5 bits
c. 20 bits
d. 16 bits

Answer : c

10. What is the maximum size of segment when Granularity bit is 0.

a. 4 GB b. 1 MB
c. 64 Terabyte d. 64 KB
Answer : b

11. What is the maximum size of segment when Granularity bit is 1.

a. 4 GB b. 1 MB
c. 64 KB d. 64 TB
Answer : a

12. Granularity bit is located at

a. Segment Descriptor b. Segment Register
b. Flag register d. Selector
Answer : a

13. Size of GDT is

a. 4GB b. 4KB
c. 64KB d. 1MB
Answer: c

14. What is the size of each descriptor in GDT.

a. 32 bit b. 64 KB
c. 8 byte d. 1 MB
Answer : c

15. Where is the Conforming bit located.

a. Selector b. Code segment descriptor
c. Data segment descriptor d. TSS
Answer : b

16. The program can reference data only within a segment in which

a. DPL <= CPL b. DPL>=CPL
c. DPL=CPL d. RPL=DPL
Answer: b

17. Call gate descriptor may reside in

a. GDT b. LDT
c. IDT d. Both GDT and LDT
Answer: d

18. Task State Segment contains

a. General purpose registers b. Segment registers
c. Flag registers d. All of the above.
Answer : d

19. Task Register contains

a. Selector to TSS descriptor of currently executing task
b. Base address of GDT c. Limit of GDT
d. All of the above.
Answer: a

20. When T(Trap bit) is set it generates debug exception on following,

a. Macro call b. Push instruction
c. Pop instruction d. Task switching
Answer : d

21. Call gate is

a. segment descriptor b. special system descriptor
c. data segment descriptor d. code segment descriptor
Answer: b

22. Which instructions can use gates to transfer control to lower privilege level

a. JMP b. CALL
c. JNC d. Both JMP and CALL
Answer: b

23. Call Gates can only be accessed if,

a. Gate DPL>= Max(RPL,CPL) b. Gate DPL<= Max(RPL,CPL)
c. Gate DPL=Max(RPL,CPL) d. Gate DPL> Max(RPL,CPL)
Answer: a

24. Privilege rule states that

a. Stack DPL> CPL b. Stack DPL=CPL
c. Stack DPL <CPL d. Stack DPL <= CPL
Answer: b

25. Pointer validation instructions are

a. LAR, LSL b. VERR, VERW
c. INC, DEC d. JMP, CALL
Answer: a

26. Descriptor validation instructions are

a. LAR, LSL b. VERR, VERW
c. INC, DEC d. JMP, CALL
Answer: b

27. Code segments can be

a. readable b. writeable
c. Conforming d. both a and c
Answer: d

28. TSS is accessible to

a. PL 0 b. 80386
c. PL 0,1,2,3 d. All
Answer: b

29. TSS Descriptor is stored in

a. LDT b. IDT
c. GDT d. both LDT and GDT
Answer: c

29. Selector for previous TSS descriptor is provided by

a. TR b. Code segment selector
c. Back link field d. LDTR
Answer: c

30. Task gate refers to

a. Code Segment b. TSS
c. Data Segment d. Task Register
Answer: b

31. Task gates are available in

a. GDT & LDT b. LDT & IDT
c. GDT d. IDT
Answer: b

32. Privilege rule to access TSS via task gate is

a. Max (RPL,CPL)<= task gate DPL
b. Max (RPL,CPL)>=task gate DPL
c. Max (RPL,CPL)= task gate DPL
d. Max (RPL,CPL)<=task gate DPL
Answer: a

33. Privilege rule to access TSS via direct TSS descriptor is

a. Max (RPL,CPL)<= TSS DPL
b. Max (RPL,CPL)>=TSS DPL
c. Max (RPL,CPL)= TSS DPL
d. Max (RPL,CPL)<=TSS DPL
Answer: a

34. Interrupts and exception causing task switch can use task gate available at

a. GDT b. GDT / LDT
c. IDT d. LDT
Answer: c

35. Task can be restricted to cause task switch with task gate available at

a. GDT b. GDT / LDT
c. IDT d. LDT
Answer: d

36. LTR can be executed at

a. CPL=DPL b. CPL=0
c. CPL>DPL d. CPL<DPL
Answer: b

37. STR can be executed at

a. CPL=DPL b. CPL=0
c. CPL>DPL d. Any privilege level
Answer: d

38. which instructions will nest task

a. CALL and JMP b. CALL
c. JMP d. INC
Answer: b
JMP instruction will not nest task

39. New nested task must return to old task with

a. RET b. IRET
c. JMP d. both a and b
Answer: b
RET instruction will not unnest tasks

40. Selector field of task gate must refer to

a. TSS b. TSS descriptors
c. Code segment d. TR
Answer: b

41. Which bit prevents looping in task

a. NT bit b. B bit
c. TS bit d. PE bit
Answer: b

42. Which bit is set when one task nests another task to indicate that it is a child task

a. NT bit b. B bit
c. TS bit d. PE bit
Answer: a

43. Minimum limit of TSS is

a. 64KB b. 8 bytes
c. 4KB d. 103 bytes
Answer: d (Total 104= 0 to 103)

43. Minimum limit of TSS is

a. 64KB b. 8 bytes
c. 4KB d. 67H bytes
Answer: d (67H)= 103 in decimal)

UNIT 4

1. What is the size of an Interrupt Gate descriptor located in IDT.

a. 64 KB b. 8 byte
c. 1 MB d. 32 bit.

Answer : b

2. Task Gate , Interrupt Gate , Trap Gate descriptors all are located in ?

a. IDT (Interrupt Descriptor Table)
b. GDT (Global Descriptor Table)
c. LDT (Local Descriptor Table)
d. Task Register

Answer : a

3. Maskable interrupts are signalled via.

a. INTR pin b. HLD pin
b. NMI pin d. BUSY pin

Answer : a

4. When IF(Interrupt Flag) is disabled following is true.

a. Procedures are disabled b. Multitasking is disabled
c. INTR interrupts are disabled d. Macros are disabled

Answer : c

5. Base address of IDT(Interrupt Descriptor Table) is stored in following.

a. IDTR(Interrupt Descriptor Table Register)
b. LDTR (Local Descriptor Table Register)
c. GDTR (Global Descriptor Table Register)
d. TR (Task Register)

Answer : a

6. The Interrupt handler routine returns with

a. RET instruction
b. IRET instruction
c. CALL instruction
d. JMP instruction

Answer : b

7. Interrupt 0 is used for following exception.

a. Divide Error b. Debug Exception
c. Overflow exception d. None of the above

Answer : a

8. Interrupt 4 represents following exception.

a. Overflow exception b. Bounds Check exception
c. Interrupt exception d. Divide error

Answer : b

9. I/O instructions can be executed when

a. CPL< IOPL b. CPL<= IOPL
c. CPL>IOPL d. CPL>= IOPL

Answer: b

10. which are register I/O instructions

a. IN/OUT b. INS/OUTS
c. INSB/OUTSB d. INC/DEC
Answer: a

11. which are block I/O instructions

a. IN/OUT b. INS/OUTS
c. JMP/CALL d. INC/DEC
Answer: b

12. A task can change IOPL with POPF only with

a. CPL>DPL b. DPL= CPL
c. CPL=0 d. CPL<DPL
Answer: c

13. CLI and STI alter IF flag with POPF only if

a. CPL>IOPL b. DPL= CPL
c. CPL=0 d. CPL<=IOPL
Answer: d

14. The structure allows selective trapping is

a. TSS b. I/O permission bit map
c. Call gate d. Task Gate
Answer: b

15. changes to IF by POPF are

a. DPL sensitive b. IOPL sensitive
c. RPL sensitive d. non of above
Answer: b

16. Interrupt ID 2 is for

a. Debug fault b. NMI
c. Invalid TSS d. Page fault
Answer: b
(Dear students please read all identifiers- This is a sample question can be asked for any identifier)

17. Faults are

a. maskable interrupts b. Non maskable interrupts
c. exceptions d. traps
Answer: c
(exceptions are categorized into faults, traps and aborts)

18. Faults are reported

a. after instruction execution b. before instruction execution
c. during instruction execution d. both b and c
Answer: d

19. Traps are reported

a. Instruction boundary after execution b. before instruction execution
c. during instruction execution d. both b and c
Answer: a

20. Aborts are reported

a. after instruction execution b. before instruction execution
c. during instruction execution d. not permit precise location of occurrence
Answer: d

21. Identifiers for exceptions and NMI are provided by the

a. 8259A PIC b. 80386
c. Operating system d. IDT
Answer: b

22. Identifiers for maskable interrupts are provided by the

a. 8259A PIC b. 80386
c. Operating system d. IDT
Answer: a

23. Debug faults are masked with

a. IF b. RF c. NMI d. TF
Answer: b

24. Interrupts at INTR are masked with

a. IF b. RF c. NMI d. TF
Answer: a

25. NMI are masked with

a. Till IF is 0 b. Till RF is 1 c. Till TF is 0 d. Till IRET is executed
Answer: d

26. Interrupt that vectors through Interrupt gate

a. sets IF b. resets IF
b. sets TF d. Resets TF
Answer: b

27. Interrupt that vectors through Trap gate

a. sets IF b. resets IF
b. sets IOPL d. non of above
Answer: d
(Trap get does not affect IF)

**********Thank YOU**********
**********ALL THE BEST **********