Que-- The Segmentation in 80386 facilitates -------
A) Protection Memory management with Multitasking d.
B) Isolation and memory management
C) Memory management with Multitasking
D) all of above
Answer. D

Que-- Which of the following statement is true?
A) Paging is compulsory and Segmentation is optional
B) Segmentation and paging both are optional.
C) Segmentation and paging both are compulsory.
D) Segmentation is compulsory and paging is optional.
Answer. D

Que-- Segmentation translates ----------. When paging is enabled.
A) logical address to physical address
B) linear address to physical address
C) logical address to linear address
D) logical address to absolute address
Answer. c

Que-- Segmentation translates ---------- When paging is disabled .
A) logical address to physical address
B) linear address to physical address
C) logical address to linear address
D) logical address to absolute address
Answer. A

Que-- An Effective address can be calculated by using ----------
A) Base
B) Index and scale
C) Displacement
D) all of above
Answer. D

Que-- Paging unit translates ----------
A) Logical address to physical address
B) Linear address to physical address
C) Logical address to linear address
D) Logical address to absolute address
Answer. B

Que-- For the 80386 processor segment size is
A) Fixed to 64 KB.
B) Fixed to 4 GB.
C) Not fixed.
D) None of above.
Answer. C

Que-- The 80386 processor can address up to ---------- memory
A) 64 KB.
B) 4 GB.
C) 1 MB
D) none of above.
Answer. B

Que-- There can be ------- descriptor(s) per segment
A) 1
B) 2
C) 0
D) 4
Answer. A

Que-- A descriptor size is ---------- bytes.
A) 2
B) 4
C) 6
D) 8
Answer. D

Que-- Size of GDTR is --------- bits
A) 16
B) 32
C) 48
D) 64
Answer. C

Que-- Size of IDTR is --------- bits
A) 16
B) 32
C) 48
D) 64
Answer. C

Que-- Size of LDTR is --------- bits
A) 16
B) 32
C) 48
D) 64
Answer. A

Que-- Type 2 system descriptor is ----------.
A) an LDT descriptor
B) a TSS descriptor
C) a Call gate Descriptor
D) None of given.
Answer. A

Que-- Which of the statement is false?
A) Global descriptor table can store any type of descriptor.
B) Local descriptor table can store code, data, stack, Call gate, task gate Descriptors.
C) Interrupt Descriptor table can store code and data segment descriptors.
D) None of the above.
Answer. C

Que-- Length of the GDT is ----------.
A) fixed
B) 64 KB
C) between 8 bytes to 64 Kbytes
D) 8KB
Answer. C

Que-- Selector value is copied from ----------
A) segment register
B) descriptor
C) descriptor table register
D) Descriptor cache
Answer. A

Que-- In segmentation process when TI = 1 , the selector's Index part points to the -----
----
A) Target segment descriptor.
B) Interrupt gate descriptor
C) LDT descriptors.
D) None of the above.
Answer. C

Que-- In segmentation process when TI = 1 , then destination segment descriptor is
fetched from ----------
A) GDT
B) LDT
C) IDT
D) None of above
Answer. B

Que-- In segmentation process when TI = 0 , then destination segment descriptor is
fetched from ----------
A) a. GDT
B) b. LDT
C) c. IDT
D) d. None of above
Answer. A

Que-- If paging is off then 32 bit linear address is treated as ----------
A) logical address
B) linear address
C) physical address
D) absolute address
Answer. C

Que-- During segmentation, access to the segment is allowed only if the selector's RPL is ---------- the DPL value conta
descriptor.
A) privilege wise same or greater than
B) numerically same or greater than

C) privilege wise same or less than
D) numerically same or less than
Answer. D

Que-- During execution of an IOPL sensitive instruction, if IOPL is set to 3 then any program ----------.
A) can access I/O devices
B) cannot access I/O devices
C) can access some of the I/O devices.
D) None of the above.
Answer. A

Que-- During execution of an IOPL sensitive instruction, if IOPL is 0 then only code segments having privilege level ---------can devices.
A) 0
B) 1
C) 2
D) 3
Answer. A

Que-- Segment descriptors are created by ----------

A) a. compilers,
B) b. linkers and loaders,
C) c. operating system but not by application programs
D) d. all of the above.
Answer. D

Que-- If Granularity G bit of a descriptor is =1 and limit field consists of a value 2KB then size of the segment is --------?
A) 2KB
B) 4KB
C) 8 KB
D) 8KB
Answer. C

Que-- Flat model of 80386 supports maximum ---------- gigabytes of memory
A) 1 Gb
B) 2 Gb
C) 4 Gb
D) None of these.
Answer. C

Que-- What are the components of an address for 80386
A) Page Number
B) Segment selector
C) Offset
D) Both B and C
Answer. D

Que-- The signed byte integer values range from --------- to --------
A) -32768 to +32767

B) -128 to +127
C) -32767 to +32768
D) -127 to +128
Answer. D

Que--The Unsigned word integer values range from --------- to --------
A) -128 to +127
B) -32768 to +32767
C) -127 to +128
D) 0-255
Answer. B

Que-- The 80386 supports --------- data types.
A) 18
B) 16
C) 17
D) 15
Answer. C

Que-- Following are the data types used by 80386 DX Processor
A) 8,16,32 bit signed and unsigned Integer
B) Character and strings
C) Packed and unpacked BCD i
D) All of above
Answer. D

Que--How many segment registers are available in 80386?
A) 4
B) 6
C) 7
D) 8
Answer. B

Que-- Register Names beginning with E indicates ------- bit register width
A) 8
B) 16
C) 32
D) 64
Answer. C

Que--Amongst given which is the example of conditional flag register?
A) AC
B) IF
C) TF
D) DF
Answer. A

Que-- Amongst given which is the example of conditional flag register?
A) DF
B) IF

C) TF
D) ZF
Answer. D

Que-- Amongst given which is the example of conditional flag register?
A) DF
B) IOPL
C) PF
D) NT
Answer. C

Que-- Amongst given which is the example of control flag register?
A) TF
B) CY
C) PF
D) SF
Answer. A

Que-- Amongst given which is the example of system flag register?
A) DF
B) IOPL
C) CY
D) SF
Answer. B

Que-- Amongst given which is the example of system flag register?
A) DF
B) ZF
C) CF
D) NT
Hide Answer
Answer. D

Que-- ESP Register is used to access ------ segment
A) Extra
B) Stack
C) Code
D) Data
Answer. B

Que-- EBP Register is best suitable to to access ------ segment
A) Extra
B) Stack
C) Code
D) Data
Answer. B

Que-- When carry flag is set?
A) If carry generated out of MSB
B) If carry generated out of D15 bit

C) If carry generated out of D3 bit
D) All of above
Answer. A

Que-- Which of the following is a specid purpose reg. in 80386 ?
A) EIP
B) ESP
C) EFLAGS
D) ALL
Hide Answer
Answer. D

Que-- The prefetch unit permits 80386DX to prefetch upto …….. bytes of instruction code.
A) 6
B) 8
C) 16
D) 20
Hide Answer
Answer. C

Que-- When parity flag is set?
A) If result contains even number of 1's
B) If lower byte contains even number of 1s
C) If lower byte contains odd number of 1s
D) If lower word contains odd number of 1s
Hide Answer
Answer. A

Que-- When auxiliary flag is set?
A) If carry generates out of MSB
B) If carry generates out of D7 bit
C) If carry generates out of D3 bit
D) If carry generates out of D15 bit
Hide Answer
Answer. C

Que-- When overflow flag is set?
A) If carry is generated out of D6 bit in signed number operation
B) If carry is generated out of D14 bit in signed number operation
C) If carry is generated out of D30 bit in signed number operation
D) All of above
Hide Answer
Answer. C

Que-- If direction flag is set then
A) SI is automatically decremented
B) SI is automatically incremented
C) DI is automatically decremented

D) Both (A) and (c)
Answer.

Que-- What is the use of trap flag?
A) To debug the program
B) To execute the instruction at a time
C) To check register or memory contents before complete execution
D) All of above
Answer.

Que-- Which flag is not present in 8086 microprocessor but present in 80386 microprocessor?
A) Nested Task Flag
B) Trap Flag
C) Sign Flag
D) Zero Flag
Answer.

Que-- Which IOPL value has highest priority?
A) 0
B) 1
C) 2
D) 3
Hide Answer
Answer. A

Que-- When zero flag is set?
A) After comparison instruction if source and destination are equal
B) If ALU result is zero
C) Both (A) and (b)
D) It depends on programmer.
Answer.

Que-- Which register cannot be divided into 8 bit data?
A) AX
B) DX I
C) CX
D) SI
Hide Answer
Answer. D

Que-- How many data segments are supported by 80386?
A) 2
B) 3
C) 4
D) 0
Hide Answer
Answer. B

Que-- The IDT is a direct replacement of which table used in 8086 sys.
A) IVT
B) LDT
C) GDT
D) none of this
Hide Answer
Answer. A

Que-- In 80386DX a logical address is also known as------consist of
selector and an offset
A) Physical address
B) Logical address
C) Virtual address
D) None of these
Hide Answer
Answer. C

Que-- For 80386DX a logical address is also known as------consist of
selector and an offset
A) Physical address
B) Logical address
C) Virtual address
D) None of these
Hide Answer
Answer. C

Que-- The 80386 concatenates the two fragments of the limit field to form a ---------- value
A) 20 bit
B) 20 byte
C) 18 bit
D) 18 byte
Hide Answer
Answer. A

Que-- Global descriptor table register(GDTR) is a ------- register located inside the 80386DX
A) 50 bit
B) 48 bytes
C) 50 byte
D) 48 bit
Hide Answer
Answer. D

Que-- he 80386 single-step exception has ----- priority then any external interrupt
A) Low
B) Higher
C) Medium
D) None of these
Hide Answer
Answer. B

Que-- After reset 80386 starts execution in ---------- mode.
A) Real
B) Protected
C) Virtual 8086
D) none of these
Hide Answer
Answer. A

Que-- Which value of RPL in segment selector gives highest privilege level?
A) 0
B) 1
C) 2
D) 3
Hide Answer
Answer. A

Que-- Which value of RPL in segment selector gives lowest privilege level?
A) 0
B) 1
C) 2
D) 3
Hide Answer
Answer. D

Que-- What DPL field of segment descriptor indicates?
A) privilege level of segment
B) privilege level of segment descriptor
C) privilege level of descriptor table
D) all of above
Show Answer

Que-- What segment descriptor contains?
A) Base address of segment
B) Limit of size of segment
C) Access right byte
D) All of these
Hide Answer
Answer. D

Que-- What is the size of segment descriptor?
A) 16 bits
B) 32 bits
C) 48 bits
D) 64 bits
Hide Answer
Answer. D

Que-- What is the size of limit field in segment descriptor of 80386 microprocessor?
A) 8 bits
B) 16 bits

C) 20 bits
D) 32 bits
Answer.

Que-- One GDT contains how many descriptors?
A) 256
B) 2k
C) 4k
D) 8k
Hide Answer
Answer. D

Que-- One IDT contains how many descriptors?
A) 256
B) 2k
C) 4k
D) 8k
Hide Answer
Answer. A

Que-- What is maximum size of GDT?
A) 4 kB
B) 8 kB
C) 32 kB
D) 64 kB
Hide Answer
Answer. D

Que-- How many GDT is/are present in 80386 microprocessor?
A) 1
B) 256
C) 8k
D) Many, one for each task
Hide Answer
Answer. A

Que-- The interrupt vector table of 80386 has been allocated _____ space starting from _____ to _____.
A) 1Kbyte, 00000H, 003FFH
B) 2Kbyte, 10000H, 004FFH
C) 3Kbyte, 01000H, 007FFH
D) 4Kbyte, 01000H, 009FFH
Hide Answer
Answer. A

Que-- The ___ bit decides whether it is a system descriptor or code/data segment descriptor
A) P
B) S
C) D
D) G
Hide Answer

Answer. B

Que-- 80386 support which type of descriptor table from the following?
A) TDS
B) ADS
C) GDT
D) MDS
Hide Answer
Answer. C

Que-- Exactly ----------segments descriptor has to be defined for each segment memory
A) One
B) Two
C) Three
D) Four
Hide Answer
Answer. A

Que-- The Selector is of ---------- bits .
A) 10
B) 16
C) 32
D) 64
Hide Answer
Answer. D

Que-- TI indicates ----------.
A) Task indicator
B) Table indicator
C) Task identifier
D) Table identifier
Hide Answer
Answer. A

Que-- - ----------The extra segment registers in 80386 are
A) DS,FS
B) ES,SS
C) FS,GS
D) GS,CS
Hide Answer
Answer. C

Que-- The 80386DX has a------bit address bus and -------bit data bus.
A) 16,32
B) 16,16
C) 32,32
D) 32,16
Hide Answer
Answer. C

Que-- What is the use of index field present in segment selector?
A) To select GDT
B) To select LDT
C) (A) or (b)
D) To select segment descriptor
Hide Answer
Answer. B

Que-- What is the size of index field in segment selector?
A) 13 bit
B) 14 bit
C) 15 bit
D) 16 bit
Hide Answer
Answer. D

Que-- How many segment selectors are present in 80386?
A) 1
B) 4
C) 6
D) 8
Hide Answer
Answer. A

Que-- Which is non-system segment descriptor?
A) Code
B) Stack
C) Data
D) All of these
Hide Answer
Answer. A

Que-- Which is not non-system segment descriptor?
A) Code
B) Data
C) Call gate
D) Stack
Hide Answer
Answer. D

Que-- Which is not system segment descriptor?
A) Code
B) LDT descriptor
C) Call gate
D) TSS descriptor
Hide Answer
Answer. C

Que-- In segment descriptor of 80386, if D = 0 then the operand size is _____
A) 16 bit

B) 20 bit
C) 24 bit
D) 32 bit
Hide Answer
Answer. A

Que-- In segment descriptor of 80386, if D = 1 then the operand size is _____
A) 16 bit
B) 20 bit
C) 24 bit
D) 32 bit
Hide Answer
Answer. A

Que-- The ___ bit decides whether it is a system descriptor or code/data segment descriptor
A) P
B) S
C) D
D) G
Hide Answer
Answer. B

Que-- The 80386 single-step exception has ----- priority then any external interrupt
A) Low
B) Higher
C) Medium
D) None of these
Hide Answer
Answer. B

Que-- Which of the following is not an interrupt signal?
A) INTR
B) NMI
C) NA#
D) RESET
Hide Answer
Answer. C

Que-- How many IDT is/are present in 80386 microprocessor?
A) 1
B) 256
C) 8k
D) Many, one for each interrupt
Hide Answer
Answer. A

Que-- What is the use of call gate?
A) It acts as interface layer between code segment at different privilege levels
B) To handle interrupts
C) It acts as interface point between user code and a task state

segment
D) To handle exceptions
Hide Answer
Answer. D

Que-- What is the use of trap gate?
A) It acts as interface layer between code segments at different privilege levels
B) To handle interrupts
C) To handle exceptions
D) Both (b) and (c)
Hide Answer
Answer. D

Que-- What is the type number of interrupt gate descriptor of 80386?
A) A
B) B
C) D
D) E
Hide Answer
Answer. D

Que-- The Instruction format of 80386 specifies
A) Instruction , address and operand size prefix
B) Op Code and Displacement
C) base, index, and scale information
D) All of above
Hide Answer
Answer. D

Que-- Maximum length of 80386 Instruction is ----- bytes
A) 8
B) 16
C) 20
D) 12
Hide Answer
Answer. B

Que-- The 80386 DX is .... bit microprocessor.
A) 8
B) 16
C) 24
D) 32
Hide Answer
Answer. D

Que-- What is the size of data bus in 80386 DX microprocessor?
A) 8-bits
B) 16-bits

C) 32- bits
D) 24 bits
Hide Answer
Answer. C

Que-- What is the size of address bus in 80386 DX microprocessor?
A) 8-bits
B) 16-bits
C) 32- bits
D) 64 - bits
Hide Answer
Answer. C

Que-- An Effective address can be calculated by using ----------
A) Base
B) Index and scale
C) Displacement
D) all of above
Hide Answer
Answer. D

Que-- Paging unit translates ----------
A) Logical address to physical address
B) Linear address to physical address
C) Logical address to linear address
D) Logical address to absolute address
Hide Answer
Answer. B

Que-- A descriptor size is ---------- bytes.
A) 2
B) 4
C) 6
D) 8
Hide Answer
Answer. D

Que-- Type 2 system descriptor is ----------.
A) an LDT descriptor
B) a TSS descriptor
C) a Call gate Descriptor
D) None of given.
Hide Answer
Answer. A

Que-- Which of the statement is false?
A) Global descriptor table can store any type of descriptor.
B) Local descriptor table can store code, data, stack, Call gate, task gate Descriptors.
C) Interrupt Descriptor table can store code and data segment descriptors.
D) None of the above.

Hide Answer
Answer. C

Que-- Length of the GDT is ----------.
A) fixed
B) 64 KB
C) between 8 bytes to 64 Kbytes
D) 8KB
Hide Answer
Answer. C

Que-- Selector value is copied from ----------
A) segment register
B) descriptor
C) descriptor table register
D) Descriptor cache
Hide Answer
Answer. A

Que-- In segmentation process when TI = 1 , the selector's Index part points to the ---------
A) Target segment descriptor.
B) Interrupt gate descriptor
C) LDT descriptors.
D) None of the above.
Hide Answer
Answer. C

Que-- In segmentation process when TI = 1 , then destination segment descriptor is fetched from ----------
A) GDT
B) LDT
C) IDT
D) None of above
Hide Answer
Answer. B

Que-- In segmentation process when TI = 0 , then destination segment descriptor is fetched from ----------
A) a. GDT
B) b. LDT
C) c. IDT
D) d. None of above
Hide Answer
Answer. A

Que-- If paging is off then 32 bit linear address is treated as ----------
A) logical address
B) linear address
C) physical address
D) absolute address

Hide Answer
Answer. C

Que-- During segmentation, access to the segment is allowed only if the selector's RPL is ---------- the DPL value conta descriptor.

A) privilege wise same or greater than
B) numerically same or greater than
C) privilege wise same
D) numerically same or less than

Hide Answer
Answer. D

Que-- During execution of an IOPL sensitive instruction, if IOPL is set to 3 then any program ----------.

A) can access I/O devices
B) cannot access I/O devices
C) can access some of the I/O devices.
D) None of the above.

Hide Answer
Answer. A

Que-- During execution of an IOPL sensitive instruction, if IOPL is 0 then only code segments having privilege level ---------can devices.

A) 0
B) 1
C) 2
D) 3

Hide Answer
Answer. A

Que-- Segment descriptors are created by ----------

A) a. compilers,
B) b. linkers and loaders,
C) c. operating system but not by application programs
D) d. all of the above.

Hide Answer
Answer. D

Que-- If Granularity G bit of a descriptor is =1 and limit field consists of a value 2KB then size of the segment is --------?

A) 2KB
B) 4KB
C) 8 KB
D) 8KB

Hide Answer
Answer. C

Que-- Flat model of 80386 supports maximum ---------- gigabytes of memory

A) 1 Gb
B) 2 Gb
C) 4 Gb
D) None of these.

Hide Answer
Answer. C

Que-- What are the components of an address for 80386
A) Page Number
B) Segment selector
C) Offset
D) Both B and C
Hide Answer
Answer. D

Que-- The signed byte integer values range from --------- to --------
A) -32768 to +32767
B) -128 to +127
C) -32767 to +32768
D) -127 to +128
Hide Answer
Answer. D

Que-- The Unsigned word integer values range from --------- to --------
A) -128 to +127
B) -32768 to +32767
C) -127 to +128
D) 0-255
Hide Answer
Answer. B

Que-- The 80386 supports --------- data types.
A) 18
B) 16
C) 17
D) 15
Hide Answer
Answer. C

Que-- Following are the data types used by 80386 DX Processor
A) 8,16,32 bit signed and unsigned Integer
B) Character and strings
C) Packed and unpacked BCD
D) All of above
Hide Answer
Answer. D

Que-- How many segment registers are available in 80386?
A) 4
B) 6
C) 7
D) 8
Hide Answer
Answer. B

Que-- Register Names beginning with E indicates ------- bit register width
A) 8
B) 16
C) 32
D) 64
Hide Answer
Answer. C

Que-- What is operand?
A) Machine code
B) Data
C) Machine code of instruction
D) None of these
Hide Answer
Answer. B

Que-- What is opcode?
A) Machine code
B) Data
C) Machine code of instruction
D) None of these
Hide Answer
Answer. C

Que-- What is the RESET address of 80386 Microprocessor?
A) FFFFFFF0H
B) FFFFFFFFH
C) FFFFF000H
D) FFFFFF00H
Hide Answer
Answer. A

Que-- Which instruction is used to swap the content of two operand?
A) XCHG
B) TEST
C) AND
D) OR
Hide Answer
Answer. A

Que-- In Data Movement Instruction which data transfer is not possible.
A) Memory to Memory
B) Memory to Register
C) Immediate to Immediate
D) Both A and C
Hide Answer
Answer. D

Que-- In 80386 microprocessor for 32-bit operand and instructions, which registers can be used as base register?
A) ESX, EBP

B) ESI, EDI
C) Both A and B
D) All 32-bit general purpose registers.
Hide Answer
Answer. D

Que-- What is PUSHFD instruction?
A) instruction pushes all 16 bits of the EFLAGS register onto the stack.
B) instruction pushes all 32 bits of the EFLAGS register onto the stack.
C) Push All Registers Segment register saves the contents of the segment registers on the stack
D) None of these
Hide Answer
Answer. B

Que-- Which order it following to push the Register into the Stack?
A) EAX, EDX, ECX, EBX, Old ESP, EBP, ESI, and EDI.
B) EAX, EBX, EDX, ECX, Old ESP, EBP, ESI, and EDI.
C) EAX, ECX, EDX, EBX, Old ESP, EBP, ESI, and EDI.
D) None of these
Hide Answer
Answer. C

Que-- What is PUSHA instruction?
A) Push All Registers saves the contents of the eight general registers on the stack
B) Push ESP Registers saves the contents of the registers on the stack
C) Push All Registers Segment register saves the contents of the segment registers on the stack
D) None of these
Hide Answer
Answer. A

Que-- For real mode of 80386, calculate physical address of the operand present in the following

MOV AX, [BX] [DX * 2]
Given : AX = 2000H, DX = 3000H, BX = 1000H, CS = 2000H, DS=3000h

A) 28000H
B) 37000H
C) 18000H
D) 0A000H
Hide Answer
Answer. B

Que-- Which instruction is used to convert the word into the double word?
A) CWDE
B) CBW
C) CDQ
D) CWD
Hide Answer

Answer. D

Que-- Which instruction is used to move with sign extension?
A) MOV
B) MOVZX
C) MOVSX
D) None of these
Hide Answer
Answer. C

Que-- Which instruction is used to move with Zero extension?
A) MOV
B) MOVZX
C) MOVSX
D) None of these
Hide Answer
Answer. B

Que-- Which of the following is an illegal 80386 instruction
A) MOV 50h, EBX
B) INC EBP
C) AND bx, bx
D) ADD ax, 25h
Hide Answer
Answer. A

Que-- What is the use of ADC instruction?
A) ADC sums the operands, adds one if CF is set, and replaces the destination operand with the result
B) ADC sums the operands, and replaces the destination operand with the result
C) ADC sums the operands, adds zero if CF is set, and replaces the destination operand with the result
D) None of these
Hide Answer
Answer. A

Que-- What is the use of INC instruction?
A) INC adds one to the destination operand.
B) INC adds one to the source operand.
C) INC adds two to the destination operand.
D) None of these
Hide Answer
Answer. A

Que-- What is the use of DEC instruction?
A) DEC Subtract one from the destination operand.
B) DEC Subtract one from the source operand.
C) DEC Subtract two from the destination operand.
D) None of these
Hide Answer
Answer. A

Que-- What is the use of CMP instruction?
A) CMP, adds the source operand from the destination operand, but does not alter the source and destination operands
B) CMP, subtracts the source operand from the destination operand, and stores the result in the destination operands
C) CMP subtracts the source operand from the destination operand, but does not alter the source and destination operands
D) all of these
Hide Answer
Answer. C

Que-- What is the use of SBB instruction?
A) SBB subtracts the source operand from the destination operand, add 1 if CF is set, and returns the result to the destination operand.
B) SBB subtracts the source operand from the destination operand, subtracts 1 if CF is set, and returns the result to the destination oper
C) SBB subtracts the source operand from the destination operand, add 1 if CF is set, and returns the result to the Source operand.
D) all of these
Hide Answer
Answer. B

Que-- Which instruction is used to Load GDT register?
A) LLDT
B) LGDT
C) LGT
D) None of these
Hide Answer
Answer. B
Show Answer
Show Answer

Que-- Which instruction is used to Load LDT register?
A) LIDT
B) LGDT
C) LLDT
D) None of these
Hide Answer
Answer. C

Que-- Which instruction is used to Store IDT register?
A) SLDT
B) SGDT
C) SIDT
D) None of these
Hide Answer
Answer. C

Que-- Which instruction is used to Store LDT register?
A) SIDT
B) SGDT
C) SLDT
D) None of these
Hide Answer
Answer. C

Que-- Which instruction is used to Store GDT register?
A) SLDT
B) SGDT
C) LGT
D) None of these
Hide Answer
Answer. B

Que-- What is the meaning of that instruction

MOV TR n, REG / MOV REG, TRn
A) Moves to/from debug reg.
B) Moves to/from control reg.
C) Moves to/from Test reg.
D) D all of these
Hide Answer
Answer. C

Que-- What is the meaning of that instruction MOV DR n, REG / MOV REG, DRn
A) Moves to/from debug reg.
B) Moves to/from control reg.
C) Moves to/from Test reg.
D) all of these
Hide Answer
Answer. A

Que-- What is the meaning of that instruction MOV CR n, REG / MOV REG, CRn
A) Moves to/from reg.
B) Moves to/from control reg.
C) Moves to/from Test reg.
D) all of these
Hide Answer
Answer. B

Que-- Which instruction is used to Load MSW?
A) LMSW
B) LCR0
C) SMSW
D) all of these
Hide Answer
Answer. A

Que-- Which instruction is used to Load IDT register?
A) LLDT
B) LGDT
C) LIDT
D) None of these
Hide Answer
Answer. C

Que-- Which instruction is used to Store MSW.
A) SMSW
B) LCR0
C) LMSW
D) all of these
Hide Answer
Answer. A

Que-- What is ARPL?
A) Adjust Requested Privilege Level
B) Adjust Requested Program Level
C) Adjust Requested Privilege Low
D) None of these
Hide Answer
Answer. A

Que-- RET instruction is used in association with ____ instruction.
A) JMP
B) CALL
C) ACALL
D) All of these
Hide Answer
Answer. B

Que-- What is IRET?
A) Return from procedure
B) Return to procedure
C) Return from Interrupt routine
D) All of these
Hide Answer
Answer. C

Que-- What is JLE?
A) Jump less or equal
B) Jump less or not equal
C) Jump if Equal
D) None of these
Hide Answer
Answer. A

Que-- What is JNGE?
A) Jump if not greater or equal
B) Jump if not greater not equal
C) Jump if not equal
D) All of these
Hide Answer
Answer. A

Que-- What is JNO?
A) Jump if not Overflow

B) Jump if Oveflow
C) Jump if not greater if equal
D) None of these
Hide Answer
Answer. A

Que-- A conditional jump instruction
A) always cause a transfer of control
B) always involves the use of the status register
C) always modifies the program counter
D) always involves testing the Zero flag
Hide Answer
Answer. B

Que-- The call instruction stores the return address for a subprogram
A) on the stack
B) in the memory address register
C) in the CS:IP
D) does not involve using the return address
Hide Answer
Answer. A

Que-- An assembly language directive is
A) the same as an instruction
B) used to define space for variables
C) used to start a program
D) Used to give Command to Assembler
Hide Answer
Answer. D

Que-- The call instruction modifies
A) The flags register
B) The stack pointer
C) The BP register
D) none of the these
Hide Answer
Answer. B

Que-- What is the output of the following code?
CLC
MOV BH,79h
RCL BH,1
A) CF=0, OF= 1,BH= 01100101
B) CF=1, OF=1, BH=01100110
C) CF=1, OF =0,BH= 01001101
D) CF=0, OF=0, BH=1111 0010
Hide Answer
Answer. D

Que-- An interrupt instruction
A) causes an unconditional transfer of control
B) causes a conditional transfer of control
C) modifies the status register
D) is an I/O instruction
Hide Answer
Answer. A

Que-- A data movement instruction will
A) modify the status register
B) modify the stack pointer
C) modify the program counter
D) transfer data from one location to another
Hide Answer
Answer. D

Que-- A hardware interrupt is
A) Internal interrupt
B) External interrupt
C) I/O interrupt
D) clock interrupt
Hide Answer
Answer. B

Que-- The call instruction is used to
A) access subprograms
B) access memory
C) perform I/O
D) access the stack
Hide Answer
Answer. A

Que-- An interrupt instruction
A) is an I/O instruction
B) modifies the status register
C) causes a conditional transfer of control
D) causes an unconditional transfer of control
Hide Answer
Answer. D

Que-- A data movement instruction will
A) modify the status register
B) modify the stack pointer
C) transfer data from one location to another
D) modify the program counter
Hide Answer
Answer. C

Que-- _____ instruction never transfer control to non confirming segement whose DPL ≠ CPL
A) LFS

Que-- What is the output of the following code?

```
MOV AL, 00110100B
MOV BL, 00111000B
ADD AL, BL
```

A) AL = 6CH
B) AX=0102H
C) AL=C6H
D) None of these

Hide Answer

Answer. A

Que-- What is the output of the following code?

```
MOV AL, 49H ; 49H is BCD number
MOV BH,72H ; 72H is BCD number
SUB AL, BH
```

A) AL=D7, CF=1.
B) AL=7D, CF=1.
C) AL=77, CF=1
D) none of them

Hide Answer

Answer. A

Que-- What is the output of the following code?

```
MOV AL,0011 0101B
MOV BL, 39H
SUB AL, BL
```

A) AL= 00000100, CF=0
B) BL=00000100, CF=0
C) AL=11111100 CF=1
D) BL=00000100, CF=1

Hide Answer

Answer. C

Que-- What is the output of the following code?

```
MOV BX,2376h
MOV CL,2
ROL BX, CL
```

A) 0101110011010011, CF=0
B) 1101001101011100, CF=0
C) 0110100010011101, CF=1
D) 1000 1101 1101 1000, CF=0

Hide Answer

Answer. D

Que-- What is the output of the following code? PUSHAL

A) Decrement SP by 2 & push a word to stack
B) Increment SP by 2 & push a word to stack
C) Decrement SP by 2 & push a AL to stack
D) None of these

Hide Answer

B) LES
C) JMP
D) LGS

Hide Answer

Answer. C

Answer. D

Que-- An assembly language program is translated to machine code by
A) An assembler
B) An interpreter
C) A compiler
D) A linker
Hide Answer
Answer. A

Que-- The errors that can be pointed out by the assembler are
A) Syntax errors
B) Semantic errors
C) Logical errors
D) None of the above
Hide Answer
Answer. A

Que-- The actual method of enabling Protected Mode is
A) load CR1 with the PE bit set, via the MOV CR0, R/M instruction
B) load CR0 with the PE bit set, via the MOV CR0, R/M instruction
C) load CR2 with the PE bit set, via the MOV CR0, R/M instruction
D) All of these
Hide Answer
Answer. B

Que-- Load the base address and limit of the GDT to GDTR register, using which instruction
A) LIDT
B) LGDT
C) SGDT
D) SIDT
Hide Answer
Answer. B

Que-- How many null Descriptor entries are present in a GDT?
A) 0
B) 1
C) 2
D) 3
Hide Answer
Answer. B

Que-- How many interrupt type is defined by IDT ?
A) 257
B) 256
C) 258
D) 260
Hide Answer
Answer. B

Que-- Which bit in GDT descriptor decide it's a Byte Granular or Page Granular
A) D bit
B) G bit
C) PG bit
D) None of thses
Hide Answer
Answer. B

Que-- DPL field in every descriptor is how many bit.
A) 1 bit
B) 2 bit
C) 3 bit
D) 4 bit
Hide Answer
Answer. B

Que-- The actual method of enabling Real Mode is _____
A) load CR0 with the PE bit Reset, via the MOV CR0, R/M instruction
B) load CR0 with the PE bit set, via the MOV CR0, R/M instruction
C) load CR2 with the PE bit set, via the MOV CR0, R/M instruction
D) All of these
Hide Answer
Answer. A

Que-- Which interrupt is used in a NASM for programming?
A) INT 80H
B) SYSCALL
C) Both A and B
D) None of thses
Hide Answer
Answer. C

Que-- What is .BSS stands for?
A) Block Started By Symbol
B) Block Started Symbol
C) Both A and B
D) None of thses
Hide Answer
Answer. C

Que-- When executing 32-bit code, the Intel386 DX uses either ____ or ____ it displacements, and any register can be used as base or index registers.
A) 8, 16
B) 16, 16
C) 8, 32
D) 16, 32
Hide Answer
Answer. C

Que-- 64 bit _____ increases the speed of all shift, rotate, multiply and divide operations

A) barrle shifter
B) register
C) microprocessor
D) logical shifter

Hide Answer

Answer. A

Que-- The instructions _____ and _____ are used to modify and read the visible portion of the task register.

A) LTR,STR
B) LDTR,SDTR
C) IDT,IDTR
D) GDTR,IDTR

Hide Answer

Answer. A

Que-- Given that the BL register contains ASCII value of 'B', which of the following instructions will change BL so that it contains ASCII value of 'b'

A) and bl, 0010 0000
B) or bl, 0010 0000
C) or bl, 1101 1111
D) and bl, 1101 1111

Hide Answer

Answer. B

Que-- Which of the following is an illegal instruction?

A) MOV AX, 3000
B) INC AL,1
C) AND BX,BX
D) ADD AX,30

Hide Answer

Answer. B

Que-- AAD instruction converts two unpacked _____ digits an AH and AL to the equivalent binary number in AL.

A) BCD
B) binary
C) hex
D) None of the above

Hide Answer

Answer. A

Que-- IMUL perform _____ multiplication

A) signed
B) unsigned
C) both (A) and (b)
D) None of the above

Hide Answer

Answer. A

Que-- NEG instruction takes _____ complement of the destination number and places it back to the destination

A) 2's
B) 1's
C) 9's
D) 10's

Hide Answer

Answer. A

Que-- In DAA instruction sum is adjusted to packed BCD format in _____ register

A) AL
B) AX
C) EAX
D) None of the above

Hide Answer

Answer. A

Que-- In 80386 microprocessor for 32-bit operand and instructions, which registers can be used as base register?

A) ESX,EBP
B) ESI,EDI
C) both (A) and (b)
D) All general purpose registers except ESP

Hide Answer

Answer. D

Que-- The _____ pair gives the address of the next instruction to be executed in the program sequence.

A) CS:IP
B) SS:BP
C) DS:SI
D) GS:DI

Hide Answer

Answer. A

Que-- Which of the following is an illegal 80386 instruction?

A) mov AX, [BX]
B) INC [BX]
C) ADD BX,[BX]
D) ADD AX,[CX]

Hide Answer

Answer. D

Que-- A conditional jump instruction

A) always cause a transfer of control
B) always involves the use of the status register
C) always modifies the program counter
D) always involves testing the zero flag

Hide Answer

Answer. B

Que-- In SAHF instruction _____ flaf is affected
A) VM
B) ZF
C) IOPL
D) all of above
Hide Answer
Answer. B

Que-- The instruction INC I where I is a memory variable involves ___
A) a memory read operation
B) memory read and memory write operation
C) only in arithmetic instruction
D) a memory read ,memory write and arithmetic operation
Hide Answer
Answer. D

Que-- A hardware interrupt is _____
A) also called an internal interrupt
B) also called an external interrupt
C) an i/o interrupt
D) a clock interrupt
Show Answer

Que-- An assembly language program is typically
A) non portable
B) shorter than an equivalent HLL program
C) harder to read than a machine code program
D) slower to execute than a compiled HLL program
Hide Answer
Answer. A

Que-- Which of the following is not an TASM directive
A) .stack
B) db
C) .model
D) call
Hide Answer
Answer. D

Que-- The call instruction is used to
A) access subprograms
B) access memory
C) perform i/o
D) None
Hide Answer
Answer. A

Que-- The processor control instruction are used for controlling various _____function through programs.
A) CPU
B) memory

Question-The TLB holds the recent_____entries of page tables.
A. 16
B. 32
C. 64
D. None of these

C) i/o
D) memory
Hide Answer
Answer. A

Que-- The instruction JG operates with
A) unsigned number
B) 2's complement form
C) floating point umbers
D) AASCII code
Hide Answer
Answer. B

Que-- The instruction JA operates with
A) unsigned number
B) 2's complement form
C) floating point umbers
D) AASCII code
Hide Answer
Answer. A

Que-- The call instruction stores the return address for a subprogram
A) on the stack
B) In the memory address register
C) in the CS:IP
D) does not involve using the return address
Hide Answer
Answer. A

Que-- Given that dl contains 'x' which of the following will cause 'x' to be displayed:
A) mov ah, 1h, int 21h
B) mov ah, 2h, int 21
C) mov ah, 2h, int 21h
D) mov ah, 0h, int 21
Hide Answer
Answer. C

Que-- Which of the following will terminate a program and return to MS-DOS?
A) mov ax,4c00h; int 21h
B) mov ax,4c00h; int 20h
C) mov dx,4c00h; int 21h
D) mov ax,09h; int 21h
Hide Answer
Answer. A

Que-- Virtual Mode Flag bit can be set using ____ instruction or any task switch operation only in the _____ mode
A) IRET, Virtual
B) POPF, Real

C) IRET, protected
D) POPF, protected
Hide Answer
Answer. C

Que-- The interrupt vector table of 80386 has been allocated _____ space starting from _____ to _____.
A) 1Kbyte, 00000H, 003FFH
B) 2Kbyte, 10000H, 004FFH
C) 3Kbyte, 01000H, 007FFH
D) 4Kbyte, 01000H, 009FFH
Hide Answer
Answer. A

Que-- The instructions _____ and _____ are used to modify and read the visible portion of the task register.
A) LTR,STR
B) LDTR,SDTR
C) IDT,IDTR
D) GDTR,IDTR
Hide Answer
Answer. A

Que-- A data movement instruction will
A) modify the status register
B) modify the stack pointer
C) transfer data from one location to another
D) modify the program counter
Hide Answer
Answer. C

Que-- The call instruction stores the return address for a subprogram
A) on the stack
B) In the memory address register
C) in the CS:IP
D) does not involve using the return address
Hide Answer
Answer. A

Que-- Virtual Mode Flag bit can be set using ____ instruction or any task switch operation only in the _____ mode
A) IRET, Virtual
B) POPF, Real
C) IRET, protected
D) POPF, protected
Hide Answer
Answer. C

Que-- The interrupt vector table of 80386 has been allocated _____ space starting from _____ to _____.

A) 1Kbyte, 00000H, 003FFH
B) 2Kbyte, 10000H, 004FFH
C) 3Kbyte, 01000H, 007FFH
D) 4Kbyte, 01000H, 009FFH
Hide Answer
Answer. A

Que-- What is the effect of the following instructions?
mov ah, 2h
int 21h
A) read a character into al
B) read a character into dl
C) display the character in al
D) display the character in dl
Hide Answer
Answer. D

Que-- Given that al contains the ASCII code of an uppercase letter, it can be converted to lowercase by
A) add al,32
B) or al, 1101 1111
C) and al, 0010 0000
D) sub al, 32
Hide Answer
Answer. A

Que-- What is the output of the following code?
MOV AL, -28
MOV BL,59
IMUL BL
AX=? , MSB=?
A) AX= F98CH, MSB=1
B) AX= 1652, MSB=1.
C) BX F9C8H, MSB=1
D) BX= 1652, MSB=1
Hide Answer
Answer. A

Que-- IF CX =1234H and BX=75FDH what is the value stored in CX after the execution of the following instruction:TEST CX,BX
A) 1234H
B) 77FDH
C) 75FDH
D) 1032H
Hide Answer
Answer. A

Que-- What is the output of the following code?

MOV AL,88H ;88H is BCD number

MOV CL,49 ; 49H is BCD number
ADD AL, CL
DAA

A) D7, CF=1
B) 37, CF=1
C) 73, CF=1
D) 7D, CF=1

Hide Answer

Answer. B

Que-- What is the output of the following code?

MOV AL, 49H ; 49H is BCD number
MOV BH,72H ; 72H is BCD number
SUB AL, BH
DAS

A) AL=D7, CF=1.
B) AL=7D, CF=1.
C) AL=77, CF=1
D) none of them

Hide Answer

Answer. C

Que-- What is the output of the following code?

CLC
MOV BH,179
RCL BH, 1

A) CF=0, OF= 1, BH= 01100101
B) CF=1, OF=1, BH=01100110
C) CF=1, OF =0, BH= 01001101
D) CF=0, OF=0, BH=00101100

Hide Answer

Answer. B

Que-- What is the output of the following code?

MOV SI,10010011 10101101B
CLC
MOV BH,179
RCL BH, 1

A) CF=0, OF= 1, BH= 01100101
B) CF=1, OF=1, BH=01100110
C) CF=1, OF =0, BH= 01001101
D) CF=0, OF=0, BH=00101100

Hide Answer

Answer. B

Que-- What is the output of the following code?

MOV SI,10010011 10101101B
CLC
SHR SI, 1

A) 37805, CF=1, OF=1

B) 18902, CF=1, OF=1
C) 19820, CF=1, OF=1
D) 53708, CF=1, OF=1
Hide Answer
Answer. B

Que-- What is the output of the following code?
MOV BX,23763
MOV CL,8
ROL BX, CL
A) 0101110011010011, CF=0
B) 1101001101011100, CF=0
C) 0110100010011101, CF=1
D) 1011100110001100, CF=1
Hide Answer
Answer. B

Que-- In 80386 microprocessor for 32-bit operand and instructions, which registers can be used as base register?
A) ESX,EBP
B) ESI,EDI
C) both (A) and (b)
D) All general purpose registers except ESP
Hide Answer
Answer. D

Que-- In 80386 microprocessor, for 32-bit operand and instructions which registers can be used as index registers?
A) ESX,EBP
B) ESI,EDI
C) both (A) and (b)
D) All general purpose registers except ESP
Hide Answer
Answer. D

Que-- For real mode of 80386, calculate physical address of the operand present in the following instruction
MOV AX, [BX][DX*2]
Given : AX = 2000H, DX = 3000H, DS = 1000H, CS = 2000H
A) 28000H
B) 09000H
C) 18000H
D) 0A000H
Hide Answer
Answer. C

Que-- Which of the following is an illegal instruction?
A) MOV AX, 3000
B) INC Al,1

C) AND bx,bx
D) ADD ax,30
Hide Answer
Answer. B

Que-- Given that the BL register contains ASCII value of 'B', which of the following instructions will change BL so that it contains ASCII value of 'b'
A) or bl, 0010 0000
B) and bl, 0010 0000
C) or bl, 1101 1111
D) and bl, 1101 1111
Hide Answer
Answer. A

Que-- Given that the BL register contains ASCII value of 'b', which of the following instructions will change BL so that it contains ASCII value of 'B'
A) or bl, 0010 0000
B) and bl, 0010 0000
C) or bl, 1101 1111
D) and bl, 1101 1111
Hide Answer
Answer. D

Que-- Which of the following is an illegal instruction?
A) MOV Ax, 30000
B) iNc Al
C) AND bx, bx
D) add ax, 30
Hide Answer
Answer. A

Que-- Which of the following is an illegal 80386 instruction
A) mov 20, bx
B) iNc Al
C) aNd bx, bx
D) add ax, 30
Hide Answer
Answer. A

Que-- Which of the following is an illegal 80386 instruction?
A) mov ax, [bx]
B) iNc [bx]
C) aDd bx, [bx]
D) add ax, [cx]
Hide Answer
Answer. D

Que-- The net effect of calling the following subprogram in terms of program behavior is to
MOV AX,8000H

MOV BX,AX
PUSH AX
POP BX
ADD BX,10
POP AX

A) leave ax unchanged
B) add 10 to ax
C) cause the program to behave in an unpredictable manner
D) do nothing
Hide Answer
Answer. B

Que-- A conditional jump instruction
A) always cause a transfer of control
B) always involves the use of the status register
C) always modifies the program counter
D) always involves testing the Zero flag
Hide Answer
Answer. B

Que-- An interrupt instruction
A) causes an unconditional transfer of control
B) causes a conditional transfer of control
C) modifies the status register
D) is an I/O instruction
Hide Answer
Answer. A

Que-- When a program is translated by the TASM assembler, the machine code is stored in a file with the extension
A) .lis
B) .obj
C) .exe
D) .out
Hide Answer
Answer. B

Que-- The output of the linker (LINK command) is stored in a file with the extension
A) .lis
B) .obj
C) .exe
D) .LNK
Hide Answer
Answer. B

Que-- The effect of the following instructions
Push ax
Add ax,4
Pop bx

Mov cx,ax
Push bx
Pop ax
On the ax register is

A) leave it with its original value
B) add 4 to it
C) clear it
D) double it

Hide Answer
Answer. A

Que-- The call instruction stores the return address for a subprogram

A) on the stack
B) in the memory address register
C) in the CS:IP
D) does not involve using the return address

Hide Answer
Answer. A

Que-- Given that dl contains 'x' which of the following will cause 'x' to be displayed:

A) mov ah, 1h, int 21h
B) mov ah, 2h, int 21
C) mov ah, 2h, int 21h
D) mov ah, 0h, int 21h

Hide Answer
Answer. C

Que-- Given that al contains the ASCII code of an uppercase letter, it can be converted to lowercase by

A) add al,30
B) sub al, 30
C) or al, 0010 0000
D) and al, 0010 0000

Hide Answer
Answer. C

Que-- Which of the following will read a character into al?

A) mov ah, 1h, int 21
B) mov ah, 2h, int 21
C) mov ah, 2h, int 20H
D) mov ah, 1h, int 21h

Hide Answer
Answer. D

Que-- Which of the following will display a string whose address is in the DX register?

A) mov ah, 0h ; int 21h
B) mov ah, 2h; int 21h
C) mov ah, 9h ; int 21
D) mov ah, 9h; int 21h

Hide Answer
Answer. D

Que-- Which of the following will terminate a program and return to MS-DOS?
A) mov ax,4c00h; int 21h
B) mov ax,4c00h; int 20h
C) mov dx,4c00h; int 21h
D) mov ax, 9h ; int 21h
Hide Answer
Answer. A

Que-- The CMP instruction modifies the
A) IP or CS: IP
B) destination register
C) flag register
D) segment register
Hide Answer
Answer. C

Que-- Conditional instructions typically inspect the
A) IP or CS: IP
B) destination register
C) flag register
D) accumulator
Hide Answer
Answer. C

Que-- The call instruction modifies
A) the flags register
B) IP or CS: IP
C) BP register
D) none of the these
Hide Answer
Answer. B

Que-- The call instruction modifies
A) the flags register
B) stack pointer
C) BP register
D) none of the these
Hide Answer
Answer. B

Que-- The call instruction modifies
A) IP or CS: IP and SP register
B) flags register
C) BP register
D) none of the previous
Hide Answer
Answer. A

Que-- The ret instruction modifies the
A) IP or CS: IP and SP register

B) flags register
C) BP register
D) none of the previous
Hide Answer
Answer. A

Que-- The conditional branch instruction JNS performs the operations when if __
A) ZF =0
B) SF=0
C) SF=1
D) CF=0
Hide Answer
Answer. B

Que-- What is the output of the following code?
MOV AL, 88H is BCD number
MOV CL, 49; 49H is BCD number
ADD AL,CL
DAA
A) D7,CF=1
B) 37, CF=1
C) ((C 73, CF=1
D) 7D, CF=1
Hide Answer
Answer. B

Que-- What is the output of the following code?
MOV AL, 49H; 49H is BCD number
MOV BH, 72H; 72H is BCD number
SUB AL,BH
DAS
A) AL=D7,CF=1
B) AL=7D, CF=1
C) AL=77, CF=1
D) none of them
Hide Answer
Answer. C

Que-- What is the output of the following code?
MOV AL, 00110100B
MOV BL, 00111000B
ADD AL, BL
AAA
A) AL = 6CH
B) AX=0102H
C) AX=0012 H
D) AL=C6H
Hide Answer
Answer. B

Que-- What is the output of the following code?

```
MOV AL,00110101B
MOV BL, 39H
SUB AL, BL
AAS
```

A) AL= 00000100, CF=1
B) BL=00000100, CF=0
C) AL=11111100 CF=1
D) BL=00000100, CF=1

Hide Answer

Answer. A

Que-- What is the output of the following code?

```
CLC
MOV BH,179
RCL BH,1
```

A) CF=0, OF= 1, BH= 01100101
B) CF=1, OF=1, BH=01100110
C) CF=1, OF =0, BH= 01001101
D) CF=0, OF=0, BH=00101100

Hide Answer

Answer. B

Que-- What is the output of the following code?

```
MOV SI,10010011 10101101B
CLC
SHR SI,1
```

A) 37805, CF=1, OF=1
B) 18902, CF=1, OF=1
C) 19820, CF=1, OF=1
D) 53708, CF=1, OF=1

Hide Answer

Answer. B

Que-- What is the output of the following code?

```
MOV BX,23763
MOV CL,8
ROL BX, CL
```

A) 0101110011010011, CF=0
B) 1101001101011100, CF=0
C) 0110100010011101, CF=1
D) 1011100110001100, CF=1

Hide Answer

Answer. B

Que-- What is the output of the following code?

```
PUSH AL
```

A) Decrement SP by 2 & push a word to stack

B) Increment SP by 2 & push a word to stack
C) Decrement SP by 2 & push a AL to stack
D) Illegal
Hide Answer
Answer. D

Que-- What is the output of the following code?

```
MOV AX, 37D7H
MOV BH, 151
DIV BH
```

A) AL = 65H, AH= 94 decimal
B) AL= 5EH, AH= 101 decimal
C) AH= E5H, AL= 5EH
D) AL= 56H, AH= 5EH
Hide Answer
Answer. B

Que-- The negative numbers in the binary system can be represented by
A) Sign magnitude
B) 1's complement
C) 2's complement
D) All of the above
Hide Answer
Answer. C

Que-- Pseudo instructions are
A) Machine instructions
B) Logical instruction
C) Micro instruction
D) instructions to assembler
Hide Answer
Answer. A

Que-- The errors that can be pointed out by the assembler are
A) Syntax errors
B) Semantic errors
C) Logical errors
D) none of the above
Hide Answer
Answer. A

Que-- Which of the following, when used in the data section of a MASM program, reserves 40 bytes of RAM (memory)?
A) BYTE 20 DUP (2)
B) WORD 40 DUP (1)
C) BYTE 20 DUP (20)
D) WORD 20 DUP (2)
Hide Answer

Answer. D

Que-- IF CX =1234H and BX=75FDH what is the value stored in CX after the execution of the following instruction:

TEST CX, BX

A) 1234H
B) 77FDH
C) 75FDH
D) 1032H

Hide Answer
Answer. A

Que-- What does the INTn instruction push onto the stack rthe CALL instruction does not?

A) Segment Address
B) Flags
C) Offset Address
D) None of above

Hide Answer
Answer. B

Que-- ASCII stands for

A) American standard code for information interchange
B) All-purpose scientific code for information interchange
C) American security code for information interchange
D) American Scientific code for information interchange

Hide Answer
Answer. A

Que-- Which is not an operand?

A) Variable
B) Register
C) Memory location
D) Assembler

Hide Answer
Answer. D

Hide Answer
Answer. B

Question-If RW3-RW0 =11, in DR7 then it means the operation is

A. Data read
B. Data write
C. Reserved for future use
D. Both A and B

Question-This ____flag is used to hold privilege level
A. NT
B. IOPL
C. RF
D. None of these
Hide Answer
Answer. B

Question-____register reserved for other processor
A. CR1
B. CR0
C. CR2
D. All of the above
Hide Answer
Answer. A

Question-Number of control register available in 80386___
A. 2
B. 3
C. 4
D. 5
Hide Answer
Answer. C

Question-These registers are reserved by INTEL.
A. DR3
B. DR4
C. DR5
D. Both B and C
Hide Answer
Answer. D

Question-The debugging register holds _____
A. 16 bit linear breakpoint address
B. 32 bit linear breakpoint address
C. 32 bit interrupt service routine
D. None of these

Hide Answer
Answer. B

Question-____is known as debug status register.
A. DR1
B. DR3
C. DR4
D. DR6
Hide Answer
Answer. D

Question-If RW bit in debug register is 01, then the operation is__
A. Instruction access
B. Data read
C. Data write
D. Both B and C
Hide Answer
Answer. C
Show Answer

Question-This bit is not available in DR7 register
A. GE
B. LE
C. BS
D. None of these
Hide Answer
Answer. C

Question-BD bit is available in ___register
A. DR3
B. DR4
C. DR6
D. DR7
Hide Answer
Answer. C

Question-These registers are used to test translation look aside buffer (TLB)
A. TR2 & TR3
B. TR5 & TR6
C. TR6 & TR7
D. All the above

Hide Answer
Answer. C

Question-___register holds linear address of the TLB
A. TR7
B. TR6
C. Both A and B
D. None of the above
Hide Answer
Answer. B
Show Answer

Question-___register holds physical address of the TLB
A. TR7
B. TR6
C. Both A and B
D. None of the above

Hide Answer
Answer. A

Question-This bit indicates, the entry in TLB is not dirty.
A. D#
B. D
C. D+
D. None of the above
Hide Answer
Answer. A

Question-This bit is not available in test register
A. V
B. D#
C. W
D. None of the above

Hide Answer
Answer. D

Question-This instruction not belongs to system instructions
A. Input /Output
B. Data movement
C. Interrupt control
D. None of the above
Hide Answer
Answer. B

Question-LAR used to _____
A. Load segment register
B. Load access rights byte
C. Load access register
D. None of the above
Hide Answer
Answer. B

Question-LAR instruction affects ____flag
A. DF
B. ZF

C. CF
D. All the above
Hide Answer
Answer. B

Question-This/these instruction cannot be executed in real mode
A. VERR
B. VERW
C. LSL
D. All of the above
Hide Answer
Answer. D

Question-This instruction load source into local descriptor table register
A. LLDT
B. LAR
C. LSL
D. None of the above
Hide Answer
Answer. A

Question-This instruction load value in global descriptor table
A. LGDT
B. SLDT
C. GLDT
D. None of the above
Hide Answer
Answer. A
Show Answer
Show Answer

Question-SGDT does_____
A. Load global value in global descriptor table
B. Store global descriptor table register to destination
C. Store global descriptor table register to source
D. All of the above
Hide Answer
Answer. B

Question-CLTS used to clear TS flag in the ____register
A. CR2
B. DR1
C. CR0
D. CR6
Hide Answer
Answer. C

Question-CLTS executes at privilege level ___
A. 0
B. 1

C. 2
D. 3
Hide Answer
Answer. A

Question-ESC instructions affect ____ flag
A. ZF
B. CF
C. No flags affected.
D. TF
Hide Answer
Answer. C

Question-This instruction is used to pass instruction to coprocessor
A. ESC
B. WAIT
C. READY
D. None of the above
Hide Answer
Answer. A

Question-The instruction works with ports of 80386?
A. IN
B. OUT
C. Both A and B
D. None of the above
Hide Answer
Answer. C

Question-Input instruction works on the data of size?
A. Byte
B. Word
C. Double word
D. All of the above
Hide Answer
Answer. D

Question-The port access instructions, is in the form of?
A. Fixed port only
B. Variable port only
C. Both A and B
D. None of the above
Hide Answer
Answer. C

Question-The flags affected after the execution of IN and OUT instruction?
A. CF
B. ZF
C. TF
D. No flags affected

Hide Answer
Answer. D

Question-The instruction which not belong to string?
A. INS
B. INSB
C. INSW
D. None of the above
Hide Answer
Answer. D

Question-The instruction which works on string of word?
A. OUT
B. OUTS
C. OUTSW
D. All the above
Hide Answer
Answer. C

Question-The instruction which does not belong to interrupt control?
A. CLI
B. STI
C. LIDT
D. None of the above
Hide Answer
Answer. D

Question-The flag is used control direction of the string processing?
A. CLI
B. STI
C. Both A and B
D. None of the above
Hide Answer
Answer. C

Question-The number of clock cycles required for STI instruction?
A. 1
B. 2
C. 3
D. 4
Hide Answer
Answer. C

Question-CLI instruction affects _____flag?
A. Interrupt
B. Carry Flag
C. Zero flag
D. None of the above
Hide Answer
Answer. A

Question-SIDT requires____ number of machine cycles?
A. 7
B. 8
C. 9
D. 11
Hide Answer
Answer. C
Show Answer

Question-The operands for the SIDT instruction?
A. SIDT source, destination
B. SIDT source
C. SIDT destination
D. All of the above
Hide Answer
Answer. C

Question-LIDT instruction format?
A. LIDT destination
B. LIDT source, destination
C. LIDT source
D. None of the above
Hide Answer
Answer. C

Question-The instruction MSW, related to_____
A. Interrupt enable flag
B. Machine status word
C. Machine control word
D. None of the above
Hide Answer
Answer. B

Question-The instruction used to store machine status word?
A. SMSW
B. SLMSW
C. LMSW
D. All the above
Hide Answer
Answer. A

Question-The number of clock cycles required for SMSW instruction?
A. 1
B. 2
C. 3
D. 4
Hide Answer
Answer. B

Question-When 80386 processor is reset, its default mode is_____.
A. Real
B. Protected
C. Can be real or protected
D. Virtual mode
Hide Answer
Answer. A

Question-_____bit can be used to switch the processor into protected mode.
A. PF
B. PE
C. PE#
D. None of the above
Hide Answer
Answer. B

Question-Multitasking feature available in _____mode
A. real
B. Protected
C. Both A and B
D. None of the above
Hide Answer
Answer. B

Question-The size of GDTR register is___bit
A. 72
B. 48
C. 32
D. 16
Hide Answer
Answer. B

Question-The size of LDTR is___bit
A. 8
B. 16
C. 32
D. 72
Hide Answer
Answer. B

Question-The register used to select TSS _____
A. TS
B. TR
C. TT
D. None of the above
Hide Answer
Answer. B

Question-The register not available to test translation look aside buffer is_____
A. TR5

B. TR6
C. TR7
D. None of the above
Hide Answer
Answer. A

Question-This instruction does not belong to privileged instruction set.
A. ARPL
B. LTR
C. SGDT
D. None of the above
Hide Answer
Answer. D

Question-The register which contains the data to be written into or read out of the addressed location is called
A. Memory address Register
B. Memory data register
C. Program computer
D. Index register
Hide Answer
Answer. B

Question-Protected mode is named as protected because it supports
A. Memory Management
B. Virtual Memory
C. Protection Mechanism
D. None of Above
Hide Answer
Answer. C

Question-The size of interrupt descriptor table register (IDTR) is
A. 18 bits
B. 48 bits
C. 16 bits
D. None of above
Hide Answer
Answer. B

Question-The task register supported by protected mode has a size
A. 18 bits
B. 48 bits
C. 16 bits
D. None of above
Hide Answer
Answer. C

Question-The segment selector of protected mode contains following bits in its structure
A. Index, RP, TI
B. Index, TI, GDT
C. Both A and B
D. None of above
Hide Answer
Answer. A

Question-The index field of segment selector is used to select
A. Base address of descriptor from descriptor table
B. Descriptor from descriptor table
C. Privilege Levels
D. None of above
Hide Answer
Answer. A

Question-The segment selector is used as Index or pointer which of the following
A. Descriptor table
B. General Purpose register
C. Debug registers
D. Global table
Hide Answer
Answer. A

Question-The linear address consist of following fields
A. Directory, Page, Base
B. Directory, Page, Offset
C. Both A and B
D. None of above
Hide Answer
Answer. B

Question-The descriptor in the descriptor table contains
A. Base address, Segment limit, Access right byte
B. Base address, segment limit, offset
C. Base address, Access right byte, Effective address
D. None of above
Hide Answer
Answer. A

Question-TI bit of segment selector is used to indicate
A. Descriptor tables
B. Descriptor registers
C. Pages
D. None of above
Hide Answer
Answer. A
Show Answer

Question-TI' bit set to '0' of segment selector indicates
A. Local Descriptor Table
B. Global Descriptor Table
C. Interrupt Descriptor table
D. None of above
Hide Answer
Answer. B

Question-Segment descriptor contains how many bits of base linear address of the segment
A. 32 bit
B. 48 bit
C. 16 bit
D. None of above
Hide Answer
Answer. A

Question-Which bit of segment descriptor indicates the presence of segment in memory
A. Present bit (p)
B. CPL
C. SPL
D. None of above
Hide Answer
Answer. A

Question-If G=0, it indicates memory limit upto
A. 1 MB
B. 4 GB
C. 1 GB
D. 2 GB
Hide Answer
Answer. B

Question-This unit perform task of converting logical to physical address.
A. Execution unit
B. Bus interface unit
C. Memory management
D. All the above
Hide Answer
Answer. C

Question-The 80386 processor works in address space____
A. Virtual
B. Linear
C. Physical
D. All the above
Hide Answer
Answer. D

Question-The logical address consists of ___
A. Segment selector

B. Offset
C. Both A and B
D. None of the above
Hide Answer
Answer. C

Question-Instruction used to check for illegal memory reference, while generating
A. LSP
B. LSL
C. SLL
D. None of above
Hide Answer
Answer. B

Question-If ____mechanism is not enabled, then linear address is similar to physical
A. Segmentation
B. Paging
C. Both A and B
D. None of above
Hide Answer
Answer. B

Question-___ 13 bit fields points to GDT or LDT tables.
A. T1
B. RPL
C. Index
D. All the above
Hide Answer
Answer. C

Question-The process of translation of linear to physical address, known as___
A. Segmentation
B. Paging translation
C. A or B
D. None of above
Hide Answer
Answer. B

Question-The size of offset in 32 bit linear address?
A. 10 bits
B. 11 bits
C. 12 bits
D. 13 bits
Hide Answer
Answer. C

Question-All information related to segments is stored in segment descriptor of
A. 6 byte
B. 8 byte

C. 7 byte
D. None of above
Hide Answer
Answer. B

Question-The instruction used to load base and limit of descriptor tables____
A. LGDT
B. LLDT
C. Both A and B
D. None of the above
Hide Answer
Answer. C
Show Answer

Question-The logical address consists of_____and _____
A. Selector and index
B. Selector and offset
C. Offset and limit
D. None of the above
Hide Answer
Answer. B

Question-The size of limit fields in segment descriptor____
A. 12 bits
B. 16 bits
C. 18 bits
D. 20 bits
Hide Answer
Answer. D

Question-The size of access right fields in segment descriptor____
A. 12 bits
B. 16 bits
C. 18 bits
D. 20 bits
Hide Answer
Answer. A

Question-The segment selector specified in _____register
A. Base
B. Segment
C. Index
D. Any of the above
Hide Answer
Answer. B

Question-The data structure needed for segment translation____
A. Segment selectors
B. Segment registers

C. Descriptor
D. All the above
Hide Answer
Answer. D

Question-During the conversion of linear to physical address, linear base address
A. Segment register
B. Segment descriptor
C. Base register
D. None of above
Hide Answer
Answer. B

Question-This field is not present in segment selector register.
A. RPL
B. T1
C. R1
D. None of above
Hide Answer
Answer. C

Question-RPL=00 in segment selector, means
A. Highest privilege level
B. lowest privilege level
C. All of the above
D. None of the above
Hide Answer
Answer. A

Question-The bit field which is not available in Access right byte of segment
A. P
B. DPL
C. S
D. None of the above
Hide Answer
Answer. D

Question-Which bit is not available in base address of base address of segment?
A. G
B. D
C. AVL
D. A
Hide Answer
Answer. D

Question-If TYPE = 001, then it decribes____in Access right bytes
A. Data segment, read only
B. Data segment , write/read
C. Stack segment, read/write
D. Code segment, execution only

Hide Answer
Answer. B

Question-If TYPE = 100, then it decribes____in Access right bytes
A. Data segment, read only
B. Data segment , write/read
C. Stack segment, read/write
D. Code segment, execute only
Hide Answer
Answer. D

Question-If TYPE = 110, then it decribes____in Access right bytes
A. Data segment, read only
B. Data segment , write/read
C. Code segment, execute only conforming
D. Code segment, execute only
Hide Answer
Answer. C

Question-If S bit 0 in segment descriptor then it
A. Specifies system segment descriptor
B. Specifies non system segment descriptor
C. Both A and B
D. None of the above
Hide Answer
Answer. A

Question-If D bit 1 in segment descriptor, then it
A. Assumed operands of size 16 bit
B. Assumed operands of size 32 bit
C. Assumed operands of size 48 bit
D. None of the above
Hide Answer
Answer. B

Question-If G bit 1, in segment descriptor, then
A. Unit of limit field is 1 byte
B. Unit of limit field is 1024 byte
C. Unit of limit field is 4096 byte
D. None of the above
Hide Answer
Answer. C

Question-If G bit 0, in segment descriptor, then
A. Unit of limit field is 1 byte
B. Unit of limit field is 1024 byte
C. Unit of limit field is 4096 byte
D. None of the above
Hide Answer
Answer. A

Question-This bit is reserved by Intel in segment descriptor.
A. D
B. X
C. F
D. P
Hide Answer
Answer. B

Question-How many different types of segment descriptors?
A. 1
B. 2
C. 3
D. 4
Hide Answer
Answer. B

Question-Which is not the type of non system segment descriptor?
A. Code
B. Stack
C. LDT
D. Data
Hide Answer
Answer. C

Question-If E=0 in access right byte of segment descriptor, then it describes
A. Data segment
B. Code segment
C. Stack segment
D. None of the above
Hide Answer
Answer. A

Question-If E=1 in access right byte of segment descriptor, then it describes
A. Data segment
B. Code segment
C. Stack segment
D. None of the above
Hide Answer
Answer. B

Question-Which bit sets the descriptor privilege level?
A. DL
B. DPL
C. DLP
D. None of the above
Hide Answer
Answer. B

Question-Which bit is not available in Access right byte of segment descriptor?
A. E

B. C
C. R
D. None of the above
Hide Answer
Answer. D

Question-When the segment growth exceeds beyond the limit, then_____generated
A. Exception 9
B. Exception 13
C. Error
D. None of the above

Hide Answer
Answer. B

Question-If W=0 in access right byte of data segment, means
A. Data may not read
B. Data may not written
C. Data may be written
D. None of the above

Hide Answer
Answer. B

Question-The growth of this section expands in downwards direction
A. Code
B. Data
C. Stack
D. All of the above
Hide Answer
Answer. C

Question-Which bit is not available in access right of data segments?
A. A
B. S
C. R
D. DPL
Hide Answer
Answer. C

Question-If type = 5 of non segment descriptor then it means type is
A. Read only
B. Read /write
C. Read only, expand down, accessed
D. Execute only
Hide Answer
Answer. C

Question-If type = 2 of non segment descriptor then type is
A. Read only

B. Read /write
C. Read only, expand down, accessed
D. Execute only
Hide Answer
Answer. B

Question-Which is not the type of gate descriptors?
A. Call gate descriptor
B. Task gate descriptor
C. Trap gate descriptor
D. System gate descriptor
Hide Answer
Answer. D

Question-Which is not true regarding GDT?
A. Many segments can be active at same time
B. One can have other GDT in memory, but only one active at A time,
C. One must have only one GDT, whenever process running in protected mode
D. None of the above
Hide Answer
Answer. A

Question-The number of LDT we can define at a time _____
A. 8191
B. 8192
C. 1
D. None of the above
Hide Answer
Answer. B

Question-Which field is not available in LDT descriptor?
A. Segment limit
B. P
C. Base address
D. None of the above
Hide Answer
Answer. D

Question-Which descriptor used for interrupt and exception handling?
A. Interrupt gates
B. Trap gates
C. Task gates
D. All the above
Hide Answer
Answer. B

Question-What is the size of gate descriptor?
A. 16 bits

B. 32 bits
C. 48 bits
D. 64 bits
Answer. B

Question-Which parameter specifies the number of parameters that are to be copied From callers stack to the parallel procedure's stack in descriptors
A. Character count
B. Word count
C. Register count
D. None of above
Hide Answer
Answer. B

Question-Which descriptor used to store task switching state of the processor?
A. TSS
B. Trap Gate
C. LDT
D. GDT
Hide Answer
Answer. A

Question-TSS descriptor does appear in____
A. LDT
B. GDT
C. IDT
D. None of the above
Hide Answer
Answer. B

Question-If B=0, in TSS descriptor means
A. Task is not busy
B. Task is busy
C. Both A and B
D. None of the above
Hide Answer
Answer. A

Question-This field is not available in TSS descriptor.
A. B
B. P
C. DPL
D. A
Hide Answer
Answer. D

Question-What is the size of descriptor?
A. 2 byte
B. 4 byte

C. 8 byte
D. 48 bits
Answer. C

Question-How much is the size of descriptor tables?
A. 65551 bytes
B. 65536 bytes
C. 4 GB
D. None of the above
Answer. B

Question-In a IDT, how many numbers of gate descriptor are available?
A. 512
B. 256
C. 64
D. 1024
Hide Answer
Answer. B

Question-Each task can have its own___
A. GDT
B. LDT
C. Both A and B
D. None of the above
Hide Answer
Answer. B

Question-Each register store the _____address of the base of the descriptor table
A. 32 bit linear
B. 32 bit physical
C. 16 bit linear
D. None of the above
Hide Answer
Answer. A

Question-GDTR is ____bit register of 80386 processor.
A. 16 bit
B. 32 bit
C. 48 bit
D. 64 bit
Hide Answer
Answer. C

Question-The lower 16 bit of GDTR decides_____
A. Base of segment
B. Limit of GDT
C. OFFSET
D. None of the above
Hide Answer
Answer. B

Question-The upper 4 bytes of GDTR is known as_____
A. Segment size
B. Segment limit
C. Segment attributes
D. Segment base
Hide Answer
Answer. D

Question-Segment descriptor does not provide
A. The size of a global memory segment
B. The starting point of a global memory segment
C. The access rights of a global memory segment
D. None of the above
Hide Answer
Answer. D

Question-The size of IDT should not be set to support more than 256, because
A. It is not accessible
B. It does not support
C. 80386 supports only 256 interrupts
D. None of the above
Answer. C

Question-The default value that 80386 loads into IDTR defines a base address of_____and limit of _____
A. 0 & 03FH
B. 1 & 03FFH
C. 0 & 03FFH
D. 1 & F3FH
Answer. C

Question-LDTR is a ____bit register of 80386 processor
A. 20
B. 16
C. 32
D. 48
Answer. B

Question-LDT is also called as_____
A. Private table
B. Public table
C. Shared table
D. None of the above
Hide Answer
Answer. A

Question-Which instruction is not used to load LDTR, GDTR?
A. SLDT
B. LGDT
C. LLDT
D. None of the above

Answer. A

Question-Which instruction is not used to store values in descriptor table?
A. LIDT
B. SIDT
C. SGDT
D. SLDT
Hide Answer
Answer. A

Question-LDT is a
A. System Descriptor
B. Non-system Descriptor
C. Both A and B
D. None of above
Hide Answer
Answer. A

Question- Task state segment (TSS) is of type
A. System Descriptor
B. Non-system Descriptor
C. Both A and B
D. None of above
Hide Answer
Answer. A

Question- Which bit of code segment descriptor indicates that the segment is present in memory
A. Executable (E)
B. AVL
C. Segment Descriptor
D. Present Bit

Hide Answer
Answer. D

Question-The segment descriptor bit (S) = 1 of code/data segment descriptor indicates
A. Code or data segment descriptor
B. System/Gate segment descriptor
C. GDT
D. None of Above
Hide Answer
Answer. A

Question-LDT descriptor is present only in
A. GDTR
B. IDT
C. Data segment Descriptor
D. None of Above

Hide Answer
Answer. A

Question-Which gate descriptor is used to change privilege levels
A. Call gate
B. Task gate
C. Trap Gate
D. Interrupt Gate
Hide Answer
Answer. A

Question-The arrangement in which segment descriptors are grouped and placed one locations is called
A. Descriptor Table
B. TSS Descriptor
C. Segment
D. Interrupt vector table
Hide Answer
Answer. A

Question-Each descriptor takes how many bytes to store information of segment
A. 4 bytes
B. 8 bytes
C. 3 bytes
D. 2 bytes
Hide Answer
Answer. B

QUESTION- GDT can store any type of descriptor except
A. TSS
B. call gate
C. interrupt gate
D. task gate
Hide Answer
Answer. C

Question-The IDT is a direct replacement of which table used in 8086 system
A. IVT
B. LDT
C. GDT
D. None of Above
Hide Answer
Answer. A

Question-LDTR is used as an index or selector to which descriptor table
A. LDT
B. GDT
C. IDT
D. Task gate
Hide Answer

Answer. B

Question-Which instruction is used to load the values of corresponding selector in GDTR
A. LGDT
B. LLDT
C. LIDT
D. None of Above
Hide Answer
Answer. A

Question-Which instruction is used to copy the contents of IDT into destination operand
A. SGDT
B. SLDT
C. SIDT
D. None of above
Hide Answer
Answer. C

Question-Which instruction is used to copy the contents of GDT into destination operand
A. SGDT
B. SLDT
C. SIDT
D. None of above
Hide Answer
Answer. A

Question-How many page table entries a TLB can store
A. 32
B. 16
C. 8
D. None of above
Hide Answer
Answer. A

Question-The check used to check whether any problem is attempting to use segment which is not allowed is called as
A. Type checking
B. Limit checking
C. Validity checking
D. None of above
Hide Answer
Answer. A

Question-The check to determine whether a programmer is defining address out of segment limit is called as
A. Type checking
B. Limit checking
C. Validity checking
D. None of above

Answer. B

Question-How many privilege levels are provided by Pentiums protection model
A. 0
B. 1
C. 2
D. 3
Hide Answer
Answer. D

Question-kernel is assigned to which privilege level
A. Level 0
B. Level 1
C. Level 2
D. Level 3
Hide Answer
Answer. A

Question-For loading task register which instruction is used
A. HLT
B. LTR
C. LMSW
D. MOVX
Hide Answer
Answer. B

Question-The technique which allows system to create a virtual environment for their programs is called
A. Paging
B. Demand paging
C. Segmentation
D. None of above
Hide Answer
Answer. B

Question-In virtual to physical address translation, page table address is stored in which register
A. GDTR
B. LDTR
C. page table base register
D. None of above
Hide Answer
Answer. C

Question-The physical address generated by virtual to physical address translation process contains
A. Virtual page number, offset
B. Physical page number, offset
C. page table address
D. None of Above

Answer. B

Question-Read mode address generation produces physical/linear address of size
A. 20 bit
B. 30 bit
C. 16 bit
D. None of Above
Hide Answer
Answer. A

Question-Segment descriptor has how many categories
A. 2
B. 3
C. 1
D. None of Above
Hide Answer
Answer. A

Question-When first entry of GDT is reserved by Pentium processor to all zero's is known as
A. Segment descriptor
B. Null Descriptor
C. Descriptor Table
D. None of above
Hide Answer
Answer. B

Question-The structure describing segment is called as
A. Segment descriptor
B. Segment Selector
C. Segment Table
D. None of above
Hide Answer
Answer. A

Question-The process of converting logical address into a linear address is called as
A. Segmentation
B. Paging
C. All of the above
D. None of above
Hide Answer
Answer. A

Question-The task register supported by protected mode has a size
A. 48 bits
B. 16 bits
C. 8 bits
D. 24 bits

Hide Answer
Answer. B

Question-What DPL field of segment descriptor indicates?
A. privilege level of segment
B. privilege level of segment descriptor
C. privilege level of descriptor table
D. All the above
Hide Answer
Answer. A

Question-For conforming code segment, code executes when
A. CPL = DPL
B. CPL > DPL
C. CPL < DPL
D. A or B
Hide Answer
Answer. D

Question-One GDT contains how many descriptors?
A. 256
B. 2k
C. 4k
D. 8k
Hide Answer
Answer. D

Question-What is maximum size of GDT?
A. 4 kb
B. 8 kb
C. 32 kb
D. 64 kb
Hide Answer
Answer. D

Question-How many GDT is/are present in 80386 microprocessor?
A. 1
B. 256
C. Many, one for each task
D. 4k
Hide Answer
Answer. A

Question-Paging is the ---------- phase of address translation
A. First
B. Second
C. Third
D. Fourth
Hide Answer
Answer. B

Question-Paging converts the linear address to ----------
A. Linear address
B. Logical address
C. Physical address
D. None of the above
Hide Answer
Answer. C

Question-How paging is turned on in 80386
A. PG=1
B. PG=0
C. None of these
D. All of these
Hide Answer
Answer. A

Question-The second translation process is called as ----------
A. Segment translation
B. Page translation
C. All of the above
D. None of the above
Hide Answer
Answer. B

Question-Which components are present in 80386 paging mechanism
A. Page Directory
B. Page table
C. Page frame
D. All of the above
Hide Answer
Answer. D

Question-What is the page frame size in 80386?
A. 1 KB
B. 2 KB
C. 3 KB
D. 4 KB
Hide Answer
Answer. D

Question-What does A means in Page Directory Entry
A. Accumulator
B. Accessed Bit
C. Advance bit
D. None of the above
Hide Answer
Answer. B

Question-What is full form for PDBR?
A. Page directory base register
B. Page directory base reserved
C. Plain domain base register
D. None of the above
Answer. A

Question-PG bit is present in -------
A. CR0
B. CR1
C. CR2
D. CR3
Hide Answer
Answer. A

Question-Paging can be speed up using --------
A. Translation look aside buffer
B. Tables
C. Memory
D. None of the above
Hide Answer
Answer. A

Question-Translation look aside buffer uses which algorithm
A. LRU
B. FIFO
C. Optimal
D. None of these
Hide Answer
Answer. A

Question-PDE stands for --------
A. Page directory Entry
B. Page directory Enable
C. All of the above
D. None of the above
Hide Answer
Answer. A

Question-PTE stands for --------
A. Page table entry
B. Page table enable
C. All of the above
D. None of the above
Hide Answer
Answer. A

Question-The registers that are used to store four program controllable break point
A. DR5-DR7
B. DR0-DR1

C. DR6-DR7
D. DR0-DR3
Hide Answer
Answer. D

Question-The register DR6 hold
A. break point status
B. break point control information
C. break point status and break point control information
D. None of the mentioned
Hide Answer
Answer. A

Question-The bits of CR3, that are always zero are
A. higher 4 bits
B. lower 8 bits
C. higher 10 bits
D. higher 12 bits
Hide Answer
Answer. D

Question-The bit that is undefined for page directory entries is
A. A-bit
B. P-bit
C. D-bit
D. None of the above
Hide Answer
Answer. C

Question- The storage of 32 recently accessed page table entries to optimize the time,
A. page table
B. page descriptor base register
C. page table cache
D. None of the above
Hide Answer
Answer. C

Question- The 32-bit control register, that is used to hold global machine status, independent of the executed task is
A. CR0
B. CR2
C. CR3
D. All of the above
Hide Answer
Answer. D

QUESTION- The register DR6 hold
A. break point control information
B. break point address

C. break point status and break point control information
D. None of the mentioned
Hide Answer
Answer. D

Question- The registers that are not available for programmers are
A. data and address registers
B. instruction pointers
C. segment descriptor registers
D. flag registers
Hide Answer
Answer. C

Question- Which of the following is not a component of paging unit?
A. Page directory
B. Page table
C. Page base register
D. Page
Hide Answer
Answer. C

Question- The bit that is used for providing protection is
A. User/Supervisor bit
B. Read bit
C. Write bit
D. All of the above
Hide Answer
Answer. D

Question- The page table cache is also known as
A. page table storage
B. storage buffer
C. translation look aside buffer
D. None of the above

Hide Answer
Answer. C

Question-This is/are optional in 80386 processor
A. Segmentation
B. Paging
C. Both A and B
D. None of the above
Hide Answer
Answer. B

Question-In order, to enable paging, we must initialize registers___
A. CR0 & CR1
B. CR1 & CR3

C. CR0 & CR3
D. None of the above

Question-_____ address and _____ are added to generate linear address.
A. Effective, Segment Base
B. offset, instruction register
C. Effective, Instruction register
D. None of these
Answer. A

Question-Page size in 80386 is _____
A. 1 Kbytes
B. 2 Kbytes
C. 4 kbytes
D. 8 kbytes
Hide Answer
Answer. C

Question-Each page directory must contain ____number of descriptors
A. 512
B. 216
C. 1024
D. 1
Hide Answer
Answer. C

Question-Which is not attributes of pages in physical memory?
A. Absent status
B. R/W#
C. A
D. D
Hide Answer
Answer. A

Question-The most efficient use of memory ,with less fragmentation is___
A. Paging
B. Segmentation
C. Flat memory model
D. None of the above
Hide Answer
Answer. B

Question-If page fault generates then____address is stored in____register.
A. physical, CR2
B. physical, CR3
C. linear, CR2
D. linear, CR3
Hide Answer
Answer. C

Question-The _____of current page directory is stored in the CR3 Register
A. Logical address
B. Physical address
C. Linear address
D. All of the above
Hide Answer
Answer. B

Question-If U/S# bit is 0,means
A. Pages are accessible from all privileges levels
B. Pages are accessible from PL 3
C. Pages are accessible from PL 0,1,2
D. None of the above
Hide Answer
Answer. C

Question-If R/W# is 0, then
A. Write privileges are allowed
B. Read privileges are allowed
C. Code fetch operation allowed
D. Both B and C
Hide Answer
Answer. D

Question-The bit positions from 12-31 in page table entry are____
A. Page address
B. Linear address of page
C. Page frame address
D. Both A and B
Hide Answer
Answer. C