Total No. of Questions—8] [Total No. of Printed Pages—3

Seat No.	

[5459]-184

S.E. (Computer) (I Semester) EXAMINATION, 2018

COMPUTER ORGANIZATION AND ARCHITECTURE

(2015 PATTERN)

Time : Two Hours **Maximum Marks : 50**

N.B. :— (*i*) Neat diagrams must be drawn wherever necessary.

(*ii*) Figures to the right side indicate full marks.

(*iii*) Use of calculator is allowed.

(*iv*) Assume suitable data if necessary.

1. (*a*) List the elements of Bus Design. Explain any *two* elements of Bus Design. [6]

(*b*) Using Booth's algorithm multiplies the following : [6]

Multiplicand = + 22

Multiplier = – 5 [6]

Or

2. (*a*) Draw and explain data flow of floating point addition. [6]

(*b*) Explain Direct cache mapping technique with its advantages and disadvantages. [6]

3. (*a*) What are data transfer modes of DMA ? Explain any *two* in detail. [6]

P.T.O.

(*b*) Discuss the following I/O mechanisms for transferring data with a neat flowchart : [6]

(*i*) Programmed I/O

(*ii*) Interrupt driven I/O

Or

4. (*a*) What is Machine Instruction ? Explain types of Machine Instructions. [6]

(*b*) Explain the following addressing modes along with suitable example : [6]

(*i*) Direct addressing

(*ii*) Indirect addressing

(*iii*) Displacement addressing mode

5. (*a*) Draw and explain the functional block diagram of 8086. [7]

(*b*) Explain the use of the following registers of 8086 CPU : [6]

(*i*) General purpose registers

(*ii*) Segment Register

(*iii*) Pointer and Index register

(*iv*) Flag Register

Or

6. (*a*) Draw and explain instruction cycle state diagram. [7]

(*b*) Compare superscalar and superpipelined approaches in superscalar processor. [6]

7. (*a*) Explain the following instruction execution phases with suitable example : [7]

(*i*) Fetch the instruction

(*ii*) Fetch the operand

(*iii*) Execute the instruction

(*b*) Draw and explain Microprogrammed Control Unit. [6]

Or

8. (*a*) Explain in detail the following microinstruction sequencing techniques : [6]

(*i*) Single Address Fields

(*ii*) Variable Address Fields

(*b*) Name the different design methods for hardwired control units. Explain in detail with any *one* design method. [7]

Q.1	a)	Elements of bus Design = 2 Marks 1. Types of bus 2. Physical dedication 3. Method of Arbitration 4. Timing 5. Bus Width 6. Data Transfer Type Explanation of any two elements 2 * 2 = 4 Marks	[6]
	b)	Result = -110(111110010010)	[6]
		OR	
Q.2	a)	Flowchart = 3Marks Explanation = 3Marks	[6]
	b)	Direct mapping technique Explanation =2 Marks Advantages = 2 Marks Disadvantages= 2 Marks	[6]
Q.3	a)	Listing of Modes: 2 Marks Single Transfer Mode Block Transfer Mode Demand or Burst Transfer Mode Explanation of mode 2*2=4 Marks	[6]
	b)	Programmed I/O = 3 Marks Interrupt driven I/O = 3 Marks	[6]
		OR	
Q.4	a)	Machine Instruction = 2 Marks Types of machine Instruction 1. Based on operations (Explanation of All)= 2 Marks • Data Processing • Data Storage • Data Movement • Control 2. Based on number of addresses (Explanation of All)= 2 Marks • Three Address Instruction • Two Address Instruction • One Address Instruction	[6]
	b)	I. Direct addressing = 2 Marks II. Indirect addressing = 2 Marks III. Displacement addressing mode= 2Marks	[6]
Q.5	a)	Diagram = 3 Marks Explanation = 34Marks	[7]
	b)	$1\frac{1}{2}$ *4 =6 Marks	[6]

P.T.

OR

Q.6	a)	Diagram =3 Marks Explanation = 4 Marks	[7]
	b)	Each point of Differentiation = 2 Marks 2*3=6 Marks	[6]
Q.7	a)	Instruction fetch = 2 Marks Operand Fetch= 2 Marks Execution of instruction steps= 3 Marks	[7]
	b)	Diagram =3 Marks Explanation = 3 Marks	[6]

OR

Q. 8	a)	Single Address Fields = 3 Marks Variable address Fields = 3 Marks	[6]
	b)	Listing of Methods= 2 Marks Explanation of any one method= 5 Marks	[7]

- State table
- Delay element
- Program counter
- PLA ✓ ✓ ✓