(MCQs) on “Privilege”

1. By using privilege mechanism the protection from unauthorised accesses is done to
a) operating system
b) interrupt handlers
c) system softwares
d) all of the mentioned
View Answer

Answer: d
Explanation: The operating system, interrupt handlers and other system softwares can be protected from unauthorised accesses in virtual address space of each task using the privilege mechanism.

2. The task privilege level at the instant of execution is called
a) Descriptor privilege level (DPL)
b) Current privilege level (CPL)
c) Effective privilege level (EPL)
d) None of the mentioned
View Answer

Answer: b
Explanation: Any one of the four privilege levels may be used to execute a task. The task privilege level at that instant is called the Current Privilege Level (CPL).

3. Once the CPL is selected, it can be changed by
a) hold
b) transferring control using system descriptors
c) transferring control using gate descriptors
d) transferring control using interrupt descriptors
View Answer

Answer: c
Explanation: Once the CPL is selected, it cannot be changed during the execution normally in a single code segment. It can only be changed by transferring the control, using gate descriptors, to a new segment.

4. The data segments defined in GDT (global descriptor table) and the LDT (local descriptor table) can be accessed by a task with
a) privilege level 0
b) privilege level 1
c) privilege level 2
d) privilege level 3
View Answer

Answer: a
Explanation: A task executing at level 0, the most privilege level, can access all the data segments

defined in GDT and the LDT of the task.

5. A task with privilege level 0, doesnot refer to all the lower level privilege descriptors in
a) GDT (global descriptor table)
b) LDT (local descriptor table)
c) IDT (interrupt descriptor table)
d) None of the mentioned
View Answer

Answer: b
Explanation: The task with privilege level 0, refers to all the lower level privilege descriptors which applies to all the descriptors except the LDT descriptors.

6. The selector RPL that uses a less trusted privilege than the current privilege level for further use is known as
a) Least task privilege level
b) Descriptor privilege level
c) Effective privilege level
d) None of the mentioned
View Answer

Answer: c
Explanation: A selector RPL uses a less trusted privilege than the current privilege level for further use. This is known as the Effective Privilege Level of the task.

7. The effective privilege level is
a) maximum numeric of RPL and CPL
b) minimum privilege of RPL and CPL
c) numeric minimum and privilege maximum of RPL and CPL
d) none of the mentioned
View Answer

Answer: c
Explanation: The effective privilege level is minimum in numeric and maximum in privilege of RPL and CPL.

8. The task requesting an access to a descriptor is allowed to access after checking the
a) type of descriptor
b) privilege level
c) type of descriptor and privilege level
d) corresponding segment
View Answer

Answer: c
Explanation: The task requesting an access to a descriptor is allowed to access to it and to the corresponding segment, only after checking type of the descriptor and privilege level(CPL, RPL, DPL).

9. A CALL instruction can reference only a code segment descriptor with

a) DPL less privilege than CPL
b) DPL equal privilege to CPL
c) DPL greater privilege than CPL
d) All of the mentioned
View Answer

Answer: b
Explanation: A CALL or JUMP instruction can reference only a code segment descriptor with DPL equal to CPL of the task or a segment with a DPL of equal or greater privilege than CPL.

10. The RPL of a selector that referred to the code descriptor must have
a) less privilege than CPL
b) greater privilege than CPL
c) equal privilege than CPL
d) any privilege regarding CPL
View Answer

Answer: c
Explanation: The RPL of a selector that referred to the code descriptor must have the same privilege as CPL.

11. The instruction that refers to only code segment descriptors with DPL equal to or less than the task CPL is
a) CALL
b) IRET
c) ESC
d) RET and IRET
View Answer

Answer: d
Explanation: The RET and IRET instructions are to refer to only code segment descriptors with DPL equal to or less than the task CPL.

12. When a JUMP instruction references a Task State Segment(TSS) descriptor, then DPL must be
a) equally privileged as CPL
b) greater or equally privileged than CPL
c) less or equally privileged than CPL
d) less privileged than CPL
View Answer

Answer: c
Explanation: When a CALL or JUMP instruction references a Task State Segment(TSS) descriptor, then DPL must be less or equally privileged than CPL.

13. The data segment access refers to
a) loading DS
b) loading ES
c) loading SS

d) all of the mentioned
View Answer

Answer: d
Explanation: Loading DS, ES or SS for referring to a new descriptor comes under the data segment access.

14. An exception is generated when
a) privilege test is negative
b) an improper segment is referenced
c) referenced segment is not present in physical memory
d) all of the mentioned
View Answer

Answer: d
Explanation: If the privilege test is negative or an improper segment is referenced then an exception 13 is generated. If the referenced segment is not present in physical memory, an exception 11 is generated

MCQs on – Protection

This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on “Protection”.

1. The mechanism to provide protection, that is accomplished with the help of read/write privileges is
a) restricted use of segments
b) restricted accesses to segments
c) privileged instructions
d) privileged operations
View Answer

Answer: a
Explanation: The restricted use of segments is accomplished with the help of read/write privileges.

2. The Local descriptor table (LDT) and Global descriptor table (GDT) are present in
a) privileged instruction check
b) operation reference check
c) segment load check
d) none of the mentioned
View Answer

Answer: c
Explanation: In restricted use of segments i.e. segment load check, the segment usages are restricted by classifying the corresponding descriptors, under LDT and GDT.

3. The mechanism that is accomplished using descriptor usages limitations, and rules of privilege check is
a) privileged instruction check
b) operation reference check
c) segment load check
d) none of the mentioned
View Answer

Answer: b
Explanation: Restricted accesses to segment, also called, operation reference check, is accomplished using descriptor usages limitations, and rules of privilege check.

4. The mechanism that is executed at certain privilege levels, determined by CPL (Current Privilege Level) and I/O privilege level (IOPL) is
a) restricted use of segments
b) restricted accesses to segments
c) privileged instructions or operations
d) none of the mentioned
View Answer

Answer: c
Explanation: The privileged instructions or operations, also called, privileged instruction check, is executed at certain privilege levels, determined by CPL and I/O privilege level(IOPL), as defined by the flag register.

5. If CPL is not of the required privilege level, then the instructions that get affected is
a) IRET
b) POPF
c) IRET and POPF
d) None of the mentioned
View Answer

Answer: c
Explanation: The IRET and POPF instructions do not perform any of their functions, if CPL is not of the required privilege level.

6. If CPL is greater than zero, then the instruction that remains unaffected is
a) IRET
b) POPF
c) IF
d) IRET and POPF
View Answer

Answer: c
Explanation: IF remains unaffected, if CPL is greater than zero. No exception is generated for this condition.

7. The condition, “CPL not equals to zero” satisfies, when executing the instruction

a) LIDT
b) LGDT
c) LTR
d) All of the mentioned
View Answer

Answer: d
Explanation: The condition, “CPL not equals to zero” satisfies, when executing the instructions, LIDT, LGDT, LTR, LMSW, CTS and HLT.

8. While executing the instruction IN/OUT, the condition of CPL is
a) CPL = 0
b) CPL < IOPL
c) CPL > IOPL
d) All of the mentioned
View Answer

Answer: c
Explanation: The condition CPL>IOPL exists, when executing the instructions, INs, IN, OUTS, OUT, STI, CLI and LOCK.

9. The instruction at which the exception is generated, but the processor extension registers contain the address of failing instruction is
a) LTR
b) INS
c) CTS
d) ESC
View Answer

Answer: d
Explanation: At the ESC instruction, the exception is generated, but the processor extension registers contain the address of failing instruction.

10. The exception that has no error code on stack is
a) double exception detected
b) processor extension segment overrun
c) invalid task state segment
d) stack segment overrun
View Answer

Answer: b
Explanation: The processor extension segment overrun has no error code on stack.

11. Which of the following is protected mode exception?
a) double exception detected
b) invalid task state segment
c) stack segment overrun
d) all of the mentioned

View Answer

Answer: d
Explanation: Double exception detected, invalid task state segment, stack segment overrun, processor extension segment overrun, are the protected mode exceptions