Total No. of Questions—8] [Total No. of Printed Pages—2

Seat No.	

[5559]-184

S.E. (Computer) (I Sem.) EXAMINATION, 2019

COMPUTER ORGANIZATION AND ARCHITECTURE

(2015 PATTERN)

Time : Two Hours **Maximum Marks : 50**

Instructions to the candidates:

1) *Neat diagrams must be drawn wherever necessary.*
2) *Figures to the right side indicate full marks.*
3) *Use of Calculator is allowed.*
4) *Assume Suitable data if necessary*

Q.1 a) Draw and explain flow chart of non restoring.division algorithm [6]

b) Write short note on [6]
1.PROM
2.EPROM

OR

Q.2 a) Draw and explain hardware implementation of Booth's Algorithm [6]

b) Draw and explain memory hierarchy [6]

Q.3 a) Write short note on Infini Band and Infini band Architecture [6]

b) Explain following addressing modes with one example each [6]
a. auto increment
b. auto decrement
c. immediate

OR

Q.4 a) Draw and explain I/O channels with diagram. [6]

b) What is opcode and operand ? How machine instruction is represented in X86? [6]

P.T.O.

Q.5	a)	Discuss in detail 1. Instruction level and machine level parallelism 2. Instruction Issue Policy	[6]
	b)	Enlist and explain Use visible registers and control and status registers	[7]
		OR	
Q.6	a)	Draw and explain Instruction cycle state diagram	[7]
	b)	Enlist features of 8086 microprocessor.	[6]
Q.7	a)	Write a Control Sequence for Conditional Branch Instruction?	[7]
	b)	Explain How to Fetching a word from Memory and how to store a Word into Memory ?	[6]
		OR	
Q. 8	a)	Explain in detail State Table Design Method for Hardwired Control?	[7]
	b)	Explain Vertical Microinstruction format	[6]

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Marking Scheme

Q.1	a)	Flow chart= 4 Marks Explanation = 2 Marks	[6]
	b)	PROM= 3 Marks EPROM=3 Marks	[6]
		OR	
Q.2	a)	Diagram = 3 Marks Explanation = 3 Marks	[6]
	b)	Diagram = 3 Marks Explanation = 3 Marks	[6]
Q.3	a)	InfiniBand = 3 Marks Infiniband Architecture = 3 Marks	[6]
	b)	auto increment = 2 Marks auto decrement = 2 Marks immediate= 2 Marks	[6]
		OR	
Q.4	a)	Diagram = 3 Marks Explanation = 3 Marks	[6]
	b)	Opcode= 2 Marks Operand= 2 Marks Machine Instruction representation = 2Marks	[6]
Q.5	a)	1. Instruction level and machine level parallelism 2. Instruction Issue Policy	[6]
	b)	**User visible registers: 4 Marks** General Purpose registers Data Registers Address Registers Control and status registers: 3 Marks	[7]
		OR	
Q.6	a)	Diagram= 4 Marks Explanation = 3 Marks	[7]
	b)	Each feature : 1 Mark 6 features: 6 Marks	[6]

Q.7 a) Control Sequence for Conditional Branch Instruction = 7 Marks [7]

b) Fetching a word from Memory= 3 Marks
store a Word into Memory = 3 Marks [6]

OR

Q. 8 a) State Table Design Method for Hardwired Control = ~~6 Marks~~ Diagram = 3 explanation = 4 [7]

b) Diagram= 3 Marks
Explanation = 3 Marks [6]