Protection and Multitasking -- 1 marks Questions

For a single task in protected mode, the 80386 can address-------Vitual memory the virtual memory of Virtual memory

A) 32 GB
B) 64 MB
C) 32 TB
D) 64 TB

Answer- D

Question- The mechanism to provide protection, that is accomplished with the help of read/write privileges is with the help of read/write
A) restricted use of segments
B) restricted accesses to segments
C) privileged instructions
D) privileged operations

Answer- A

Question- The mechanism that is accomplished using descriptor usages limitations, and rules of privilege check is
A) privileged instruction check
B) operation reference check
C) segment load check
D) none of the mentioned

Answer- B

Question- The mechanism that is executed at certain privilege levels, determined by CPL (Current Privilege Level) and I/O privilege level (IOPL) is
A) restricted use of segments
B) restricted accesses to segments
C) privileged instructions or operations
D) none of the mentioned

Answer- C

Question- The paging unit is enabled only in
A) virtual mode
B) addressing mode
C) protected mode
D) none of the mentioned

Answer- C

Question- The bit that is used for providing protection is
A) User/Supervisor bit
B) Read bit
C) Write bit
D) all of the mentioned

Answer- D

Question- To enter in protected mode,_____ bit should be at logic 1.
A) PG

B) ET

C) PE

D) NT

Question- In 80386, privilege levels are defined by _____

A) DPL
B) CPL

C) RPL

D) All of above

Question- How many privilege levels are available in 80386
A) 1
B) 2
C) 3
D) 4

Answer- D

Question- Which is highest privilege level in 80386
A) 1
B) 3
C) 2
D) 0

Answer- D

Question- Which is LOWEST privilege level in 80386
A) 1
B) 0
C) 3
D) 2

Answer- C

Question- The unit that provides a four level protection mechanism, for system's code and data against application program is

A) central processing unit

B) segmentation unit

C) bus interface unit

D) none of the mentioned

Answer- B

Question- In protected mode of 80386, the VM flag is set by using

A) IRET instruction

B) task switch operation
C) IRET instruction or task switch operation
D) none of the mentioned

Answer- C

Question- By using privilege mechanism the protection from unauthorised accesses is done to

A) operating system

B) interrupt handlers
C) system softwares
D) all of the mentioned

Question- The task privilege level at the instant of execution is called

A) Descriptor privilege level (DPL)

B) Current privilege level (CPL)
C) Effective privilege level (EPL)

D) none of the mentioned

Question- Once the CPL is selected, it can be changed by

A) HOLD

B) transferring control using system descriptors

C) transferring control using gate descriptors

D) transferring control using interrupt descriptors

Question- The data segments defined in GDT (global descriptor table) and the LDT (local descriptor table) can be accessed by a task with

A) privilege level 0

B) privilege level 1
C) privilege level 2
D) privilege level 3
Answer- A

Question- A task with privilege level 0, does not refer to all the lower level privilege descriptors in

A) GDT (global descriptor table)
B) LDT (local descriptor table)
C) IDT (interrupt descriptor table)

D) none of the mentioned

Question- The selector RPL that uses a less trusted privilege than the current privilege level for further use is known as

A) Least task privilege level
B) descriptor privilege level
C) effective privilege level
D) none of the mentioned

Question- The effective privilege level is

A) maximum numeric of RPL and CPL

B) minimum privilege of RPL and CPL

C) numeric minimum and privilege maximum of RPL and CPL

D) none of the mentioned

Question- The task requesting an access to a descriptor is allowed to access after checking the

A) type of descriptor
B) privilege level

C) type of descriptor and privilege level
D) corresponding segment

Question- A CALL instruction can reference only a code segment descriptor with

A) DPL less privilege than CPL

B) DPL equal privilege to CPL

C) DPL greater privilege than CPL

D) all of the mentioned

Question- The RPL of a selector that referred to the code descriptor must have

A) less privilege than CPL
B) greater privilege than CPL

C) equal privilege than CPL

D) any privilege regarding CPL

Question- The instruction that refers to only code segment descriptors with DPL equal to or less than the task CPL is
A) CALL

B) IRET
C) ESC
D) RET and IRET

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B) interrupt handlers

C) system softwares

D) all of the mentioned

Question- The mechanism to provide protection, that is accomplished with the help of read/write privileges is
A) restricted use of segments
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C) privileged instructions

D) privileged operations

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A) restricted use of segments
B) restricted accesses to segments
C) privileged instructions or operations

D) none of the mentioned

Question- If CPL is not of the required privilege level, then the instructions that get affected is
A) IRET
B) POPF
C) IRET and POPF

D) none of the mentioned

Question- If CPL is greater than zero, then the instruction that remains unaffected is

A) IRET
B) POPF
C) IRET and POPF

D) none of the mentioned

Question- The condition, "CPL not equals to zero" satisfies, when executing the instruction
A) LIDT

B) LGDT

C) LTR

D) all of the mentioned

Question- While executing the instruction IN/OUT, the condition of CPL is

A) CPL = 0

B) CPL < IOPL
C) CPL > IOPL

D) all of the mentioned

Question- The instruction that reads the segment limit into the register, if privilege rules and descriptor type allow is

A) VERW

B) APRL

C) LSL

D) LAR

Question- The instruction that adjusts the RPL (Requested Privilege Level) of the selector, to the numeric maximum of current selector RPL value is

A) LAR
B) VERR
C) LSL

D) APRL

Question- The selector RPL that uses a less trusted privilege than the current privilege level for further use is known as

A) Least task privilege level
B) descriptor privilege level
C) effective privilege level
D) none of the mentioned

Question- Amongst the given which is not a privilege instruction?
A) CLTS
B) TEST
C) HLT
D) LLDT

Answer- B

Question- Amongst the given which is a privilege instruction?
A) LMSW
B) TEST
C) AND

D) STD

Answer- A

Question- Amongst the given which is a privilege instruction?
A) AAA
B) OR
C) CLD
D) MOV CR3, EAX

Answer- D

Question- What is the significance of setting R/W field of PDE in protected mode?
A) (a) Write privileges are allowed from PL3 code
B) (b) Write privileges are allowed from PL2 code
C) (c) Write privileges are allowed from PL1 code
D) (d) Write privileges are allowed from PL0 code

Answer- A

Question- What is the significance of setting R/W field of PTE in protected mode?
A) (a) Write privileges are allowed from PL3 code
B) (b) Write privileges are allowed from PL2 code
C) (c) Write privileges are allowed from PL1 code
D) (d) Write privileges are allowed from PL0 code

Answer- A

Question- What privilege level must be assigned to Kernel?
A) PL0
B) PL1
C) PL2
D) PL3
Answer- Question- For instruction HLT to be executed what must be the value of CPL?
A) 0
B) 1
C) 2
D) 3

Answer- A

Question-The on chip protection hardware performs which checks of the following ?
Type and Limit check
A) Restriction of Procedure Entry points

B) Restriction of addressable DOMAIN
C) Restriction on Certain Instruction Execution
D) All of above

Answer- D

Question- System services are implemented at Privilege level -----
A) 0
B) 1
C) 2
D) 3

Answer- B

Question- Custom routines to support special purpose system operations like Device Drivers are executed at Privilege level ----
A) 0
B) 1
C) 2
D) 3

Answer- C

Question- Conforming Code Segments conforms the privilege level of -----
A) Caller – calling code
B) Callee – called code
C) Both A and B
D) None of above
Answer- Question- Destination Selector field of a call gate is ------- bits long
A) 8
B) 16
C) 32
D) 48

Answer- B

Question- The task state segment descriptor for the designated task is checked for its ----- and --------
A) Limit and Base
B) base and address
C) limit and presence
D) base and presence

Answer- C

Question- The Task Register(TR) specify the ----- executing task by pointing to the task State Segment(TSS)

A) Normal
B) Currently
C) (Multiple
D) (Single

Answer- B

Question- What is the minimum size of TSS in 80386?

A) 64 bytes
B) 104 byte
C) 4 KB
D) 64 KB

Answer- B

Question- Multitasking is activated in ----------mode of the Processor 80386?

A) Real
B) Protected
C) Virtual
D) V86

Answer- A

Question- How task switching can be obtained in 80386?

A) The current task JMPs or CALLs a TSS descriptor
B) The current task JMPs or CALLs a task gate
C) An interrupt or exception selects a task gate
D) All of above

Answer- D

Question- To return from a task, ____ instruction is used.

A) RET
B) IRET
C) JMP
D) CALL

Answer- B

Question- .....holds task environment

A) TSS Descriptor

B) TSS

C) None of these
D) TR

Question- TSS is not accessible to
A) Program at PL0
B) User program
C) Both a & b
D) None of these

Answer- C

Question- To support multitasking .....is used
A) TSS
B) TR
C) Task Gate descriptor
D) All of these

Answer- D

Question- For task switching following is used
A) Interrupts
B) Exceptions
C) A & B
D) None of these

Answer- C

Question- In TSS descriptor if bit B=1 then
A) Task is busy
B) Operand is 16-bit
C) Operand is 32-bit
D) Operand is byte

Answer- A

Question- Size of Task state segment is
A) 80 bytes
B) 104 bytes
C) 128 bytes
D) 256 bytes

Answer- B

Question- Maximum size of TSS is
A) 64 KB
B) 1MB
C) 4GB
D) 64 TB

Answer- C

Question- Task register holds
A) Base
B) Limit
C) Both a & b
D) None of these

Answer- D

Question- .....points to TSS to specify currently executing task
A) TR
B) TP
C) TSSD
D) None of these

Answer- A

Question- Which field in TSS holds the 16-bit offset of the beginning of I/O permission bit map
A) Bit map offset
B) Back link
C) CR 3
D) EIP

Answer- A

Question- To keep track of previous task 80386 uses
A) Flags
B) EIP
C) Back link
D) None of these

Answer- C

Question- Which of following are static set fields of TSS?
A) Selector of LDT
B) PDBR

C) T-bit
D) All of these

Answer- D

Question- Which of following are static set fields of TSS?
A) I/O map Offset
B) Pointers to stack
C) A & B
D) none of these

Answer- C

Question- Privilege level of stack and code segment must be
A) Same
B) Greater than
C) Less than
D) Greater or equal

Answer- A

Question- Which of following are dynamic set fields of TSS?
A) General purpose register
B) Segment register
C) Instruction pointer
D) All of these

Answer- D

Question- Each isolated task can have
A) Separate LDT and page directory
B) Different logical to linear mapping
C) Different linear to physical mapping
D) All of these

Answer- D

Question- Each task have following mapping
A) logical to linear mapping
B) linear to physical mapping
C) Sequential
D) Both A & B

Answer- D

Question- Each task can have
A) Separate LDT and page directory
B) Different logical to linear mapping
C) Different linear to physical mapping
D) All of these

Answer- D

Question- Which bit shows the current task is child task
A) NT
B) G
C) TS
D) B

Answer- A

Question- 1. What is the long form of TSS in multitasking?
A) Test Switch Segment
B) Task switch segment
C) Task selector segment
D) Test state segment

Answer- B

Question- What is the size IOPL field?
A) (a) 1-bit
B) (b) 2-bit
C) (c) 8-bit
D) (d) 4-bit

Answer- B

Question- The parent task and child tasks are indicated by which fields of the TSS?
A) (a) Back link field and NT field
B) (b) NT field and Back link field
C) (c) ESP and Back link field
D) (d) NT field and ESP

Answer- A

Question- Which instruction is used to nest the tasks?
A) (a) JMP
B) (b) CALL
C) (c) RET
D) (d)JBE

Answer- B

Question- TSS descriptor appears in which descriptor table?
A) (a) GDT and LDT
B) (b) GDT
C) (c) LDT
D) (d) IDT

Answer- B

Question- Which portion of the task register is visible?
A) (a) Selector
B) (b) Segment descriptor
C) (c)Selector and base address
D) (d) Selector and segment limit
Answer- A

Answer- A

Question- Which descriptor table base address is present in task state segment?
A) GDT
B) IDT
C) LDT
D) None of these

Answer B

Question- What is the meaning of 'T' field in task state segment?
A) Trap flag
B) Task switch trap
C) Task register
D) Test register

Answer- B

Question- Amongst given which is a privilege instruction?
A) LOOP
B) XLAT
C) TEST
D) LTR

Answer- D

Question- What must be the CPL at the time of execution of LTR instruction?
A) 0
B) 1
C) 2
D) 3

Answer- A

Question- Which of the following instruction is used in protected mode only?
A) AAA
B) LTR
C) STD
D) CLD

Answer- B

Question- Amongst given which is not a privilege instruction?
A) STR
B) HLT
C) OUT
D) LTR

Answer- B

Question- What condition is needed to change the IOPL of any task?
A) (a) If code is at PL3
B) (b) If code is at PL2
C) (c) If code is at PL1
D) (d) If code is at PL0

Answer- D

Question- What condition is needed to change the IOPL of any task?
A) (a) If code is at PL3
B) (b) If code is at PL2
C) (c) If code is at PL1
D) (d) If code is at PL0

Answer- D

Question- Type field of Busy TSS Descriptor indicates value - ----------
A) S=0 and Type = 1001
B) S=1 and Type = 1100
C) S=0 and Type = 0100

D) None of above

Answer- A

Question- Type field of Available TSS Descriptor indicates value - ----------
A) S=0 and Type = 1001
B) S=1 and Type = 1100
C) S=0 and Type = 1011
D) None of above

Question- Type field of task Gate Descriptor indicates value - ----------
A) S=0 and Type = 0101
B) S=1 and Type = 1100
C) S=0 and Type = 0100
D) None of above

Answer- A

Protection and Multitasking MCQ's (2 Marks Questions)

Question- Which instruction is used to read the visible portion of the task register into memory or general-purpose register?
A) LTR
B) STR
C) STD
D) CLD

Qestion- . Which instruction is used to load the new TSS selector to the task register?
A) STR
B) STD
C) CLD
D) LTR

Answer- D

Question- . What is the size of segment limit in task state segment descriptor?
A) (a)8 bit

B) (b) 16 bit
C) (c) 20 bit
D) (d) 32 bit

Answer- C

Question- Which control register is present in task state segment?
A) CR0
B) CR1
C) CR2
D) CR3

Answer- D

Question- 4. Which portion of the task register is invisible?
A) (a) Selector
B) (b) Segment descriptor
C) (c)Selector and base address
D) (d) Base address and segment limit

Answer- D

Question- What condition is needed to permit the current task to switch to the new task?
A) (a) Task Gate DPL >= max(CPL, RPL)
B) (b) Task Gate DPL <= max(CPL, RPL)
C) (c) Task Gate RPL >= max(CPL, DPL)
D) (d) Task Gate CPL >= max(DPL, RPL)

Answer- A

Question- 3. What is the condition necessary to execute I/O privilege instructions?
A) (a) CPL <= IOPL
B) (b) CPL => IOPL
C) (c) DPL <= IOPL
D) (d) RPL => IOPL

Answer- A

Question- 2. In multitasking where I/O permission bitmap is located?
A) At the bottom of the Task gate descriptor
B) At the bottom of the TSS
C) On the top of the TSS
D) On the top of Task gate descriptor

Answer- C

Question- Task switching is done when
A) A long jump or call instruction contains a selector which refers to a TSS descriptor
B) Selector in long jump or call instruction refer to a task gate
C) Interrupt selector refers to a task gate
D) All of these

Answer- D

Question- During task switching without task gate which of the checks are performed
A) instruction check
B) Limit check
C) Busy task check
D) All of these

Answer- B

Question- Task switching is done by
A) Direct method
B) Indirect method
C) Both A & B
D) None of these

Answer- C

Question- In the direct method Task switching is done by
A) Jumping to task gate
B) Calling to task gate
C) Both A & B
D) Both A or B

Answer- C

Question- The DPL of the new TSS descriptor is not used for privilege checking ,when .....is used for task switch
A) Task gate
B) Trap gate
C) Call gate
D) Interrupt gate

Answer- A

Question- During task switching without task gate which of the checks are performed
A) Privilege check

B) Limit check
C) Present check
D) All of these

Answer- D

Question- Which of the following statements are false?
A) Task switches cannot be recursive
B) Tasks are not re-entrant
C) Currently running task is always a busy task
D) None of these

Answer- D

Question- When task gate is used, the DPL of target .....is not used for privilege checking
A) TSS descriptor
B) TR
C) TSS
D) Stack
Answer- A

Answer- A

Question- Processor selects task gate descriptor only when the maximum of selectors .....and the .....of procedure is less than or equal to the .....of the descriptor
A) DPL,RPL,CPL
B) CPL,DPL,RPL
C) RPL,CPL,DPL
D) CPL,RPL,DPL

Answer- C

Question- Processor selects task gate descriptor only when the maximum of selectors RPL and the CPL of procedure are..... to the DPL of the descriptor
A) less than or equal
B) Greater than or equal
C) Same
D) Less than

Answer A

Question- Bit T in TSS is used for
A) Enabling task switch trap

B) disabling task switch trap
C) Both A & B
D) None of these

Answer- C

Question- TSS descriptor present in
A) GDT
B) LDT
C) A or B
D) A
Answer-
Question- Which of following are dynamic set fields of TSS?
A) Flag register
B) Back link
C) Instruction pointer
D) All of these

Answer- D

Question- To perform context save 80386 needs minimum storage of
A) 80 bytes
B) 104 bytes
C) 128 bytes
D) 256 bytes

Answer- B

Question- Nested task switching is done by ____
A) using FAR CALL instruction
B) Exception
C) fault or trap
D) all of above

Answer- D

Question- What is the size of visible part present in TR of 80386?
A) 16 bit
B) 20 bit
C) 24 bit
D) 32 bit

Answer- A

Question- WC field of call gate is used to push ------- on destination privilege level stack .
A) Old stack SS:ESP and old CS:EIP

B) New stack SS:ESP and old CS:EIP
C) Both SS:ESP and old CS:EIP
D) None of above

Answer- A

Question- Destination offset field of a call gate is ------- bits long
A) 8
B) 16
C) 32
D) 48

Answer- C

Question- Type field of Call gate indicates value - ----------
A) S=0 and Type = 1100
B) S=1 and Type = 1100
C) S=0 and Type = 0100
D) None of above

Answer- A

Question- Privilege requirements to use a call gate are ---------- (numerically)
A) CPL ≤ DPL of the Code & C bit=0
B) DPL of the target code segment ≤ CPL & C bit=0
C) Target DPL ≤ max (RPL,CPL) & C bit=0
D) All of above

Answer- D

Question- Call gate is used to access --------
A) Code at same Privilege level
B) Code at higher privilege level
C) Code at lower Privilege
D) None of above

Answer- B

Question- For Conforming Code Segments to be used Rule is
A) CPL =DPL & C bit = 1
B) CPL numerically > DPL & C bit = 1
C) CPL numerically < DPL & C bit = 1
D) None of above

Answer- B

Question- Inter privilege level transfer can be done using
A) Task gate Descriptor
B) Call Gate Descriptor
C) Conforming Code segment Descriptor
D) B AND C

Answer- D

Question- What condition must be satisfied for successful control transfer using Call Gate mechanism?
A) (a) Target DPL= >Max(RPL, CPL) <= Gate DPL
B) (b) Target DPL<= Max(RPL, CPL) => Gate DPL
C) (c) Target DPL=> Max(RPL, CPL) => Gate DPL
D) (d) Target DPL<= Max(RPL, CPL) <= Gate DPL

Answer- D