

本次实验采用Verilog自动评测机制。

评测页面: <http://10.249.12.98:6620/>

用户名: 学号@stu.hit.edu.cn

密码: hitszcs2021 (由于现在尚未将重置密码的功能改造完毕, 所以请大家尽量不要修改过于复杂的密码, 否则可能无法重置)

登录之后, 看到以下页面:

Signed in successfully.

Courses

Current

计算机组成原理 (2021
年春)

Lab1: Report Submission (PDF Only)

Test: RTL Submission

Lab1: RTL Submission

[COURSE PAGE](#) [GRADEBOOK](#)

点击“计算机组成原理”。弹出初次修改用户信息的界面, 在Nickname填写和First name一致即可。其余无需理会。

Editing student fake's Enrollment in 计算机组成原理

Email

fake@stu.hit.edu.cn

First name

student

Last name

fake

Nickname

student

Anonymizing nickname to display on the public scoreboards

在“Assignment”下找到实验0：

Assignments —

实验0：熟悉提交流程

Test: RTL Submission

打开"RTL Submission", 此后在Handouts中下载代码模板：

Test: RTL Submission

Options

[View handin history](#)

[View writeup](#)

[Download handout](#)

🕒 Due: June 1st 2021, 12:00 pm CST

📅 Last day to handin: June 1st 2021, 12:00 pm CST

Drag a file here to hand in. Click to select a file.

Files do not submit automatically.

☐ I affirm that I have complied with this course's academic integrity policy as defined in the syllabus.

SUBMIT

(unlimited submissions left)

Handouts

📄 Code Template: top.v

样例代码如下：

```
2 // DON'T CHANGE THE MODULE AND PORT DEFINITION !!!!
1 module top(input [1:0] a, input [1:0] b, input fcn, output [1:0] c);
3     assign c = fcn ? a&b : a|b;
1 endmodule
```

修改完毕代码后，将文件上传并提交：

🕒 Due: June 1st 2021, 12:00 pm CST

📅 Last day to handin: June 1st 2021, 12:00 pm CST

📄 top.v

Last modified: May 5th 2021, 10:59 pm

Lines of code: 5

File size: 163 bytes

✕

✓ I affirm that I have complied with this course's academic integrity policy as defined in the syllabus.

SUBMIT

(unlimited submissions left)

稍后刷新测评页面，即可得到测评成绩：

