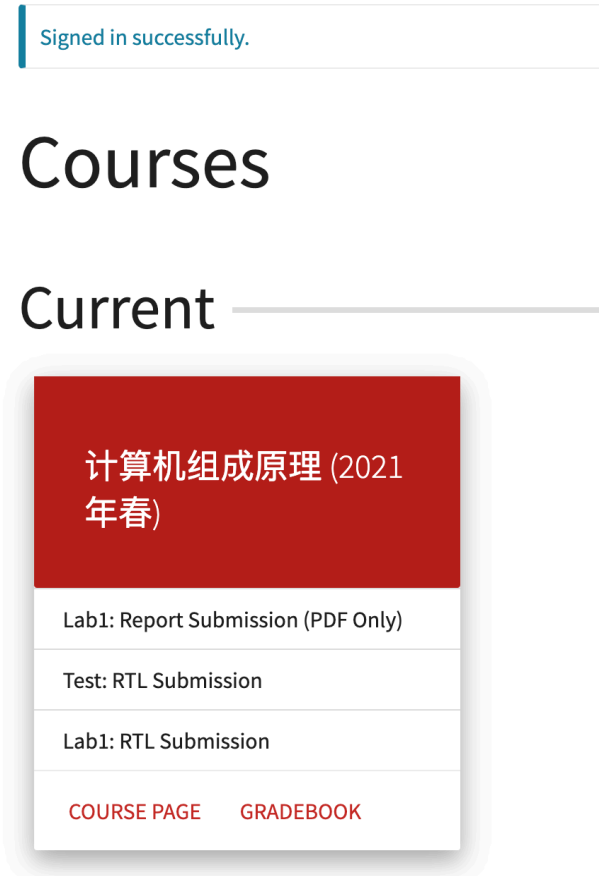
本次实验采用Verilog自动评测机制。

评测页面：http://10.249.12.98:6620/

用户名：学号@stu.hit.edu.cn

密码：hitszcs2021（**由于现在尚未将重置密码的功能改造完毕，所以请大家尽量不要修改过于复杂的密码，否则可能无法重置**）

登录之后，看到以下页面：



点击"计算机组成原理"。弹出初次修改用户信息的界面，在Nickname填写和First name一致即可。其余无需理会。

Editing student fake's Enrollment in 计算机组成原理

Email
fake@stu.hit.edu.cn

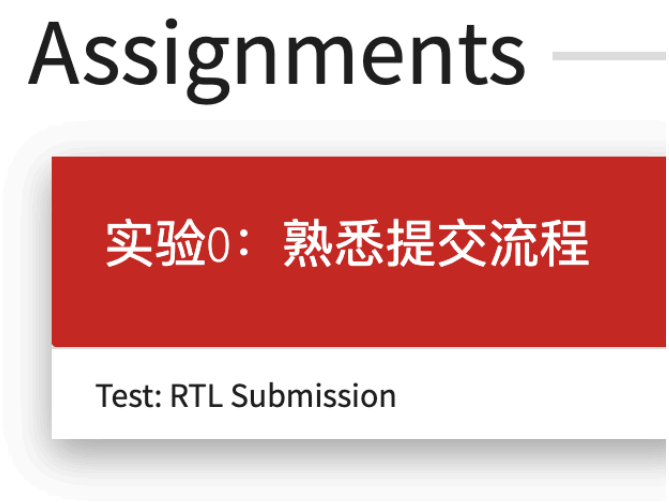
First name
student

Last name
fake

Nickname
student

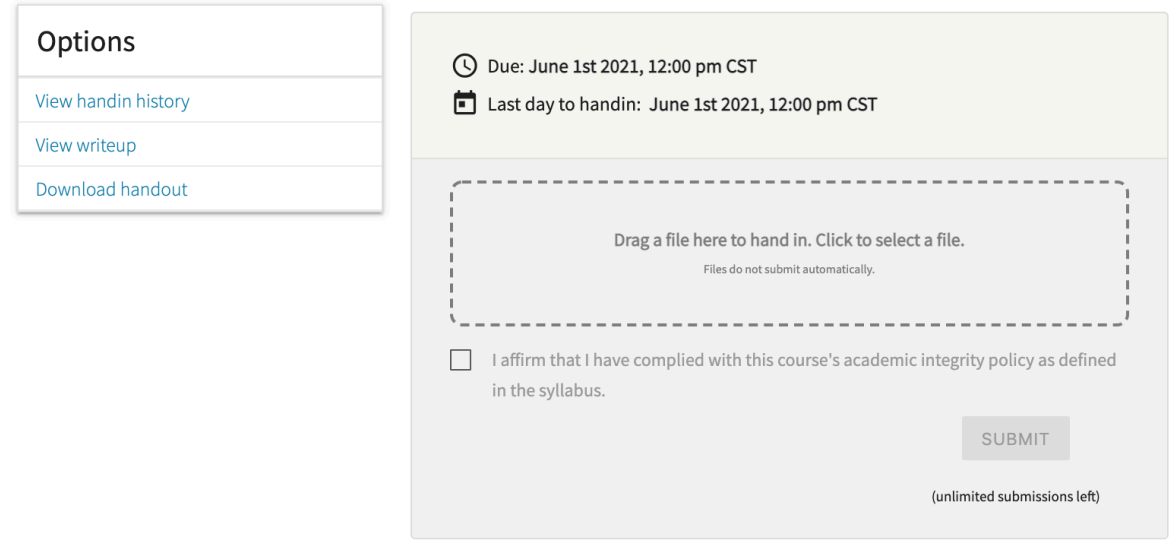
Anonymizing nickname to display on the public scoreboards

在“Assignment”下找到实验0：

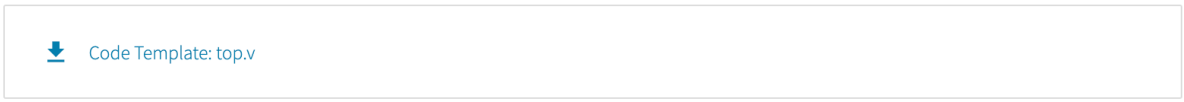


打开"RTL Submission"，此后在Handouts中下载代码模板：

Test: RTL Submission



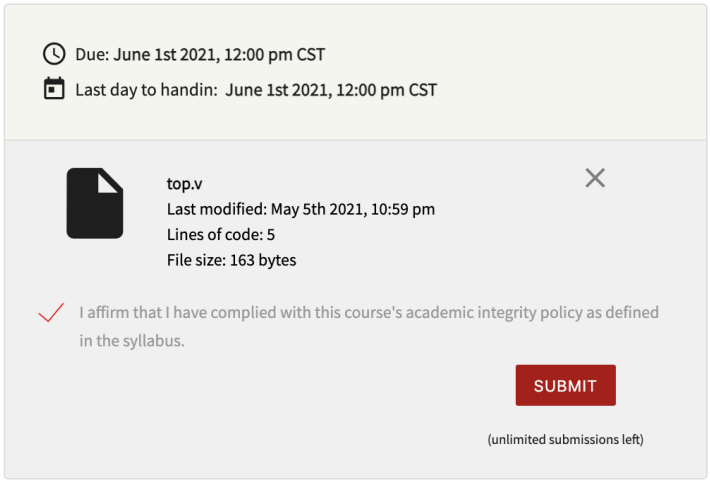
Handouts



样例代码如下：

```
// DON'T CHANGE THE MODULE AND PORT DEFINITION !!!!
module top(input [1:0] a, input [1:0] b, input fcn, output [1:0] c);
    assign c = fcn ? a&b : a|b;
endmodule
```

修改完毕代码后，将文件上传并提交：



稍后刷新测评页面，即可得到测评成绩：

Ver	File	Submission Date	And Gate (50.0)	Or Gate (50.0)	Late Days Used	Total Score
1	fake@stu.hit.edu.cn_1_handin.v	2021-05-05 22:59:21 +0800	50.0	50.0	Submitted 0 days late	100.0

Page loaded in 0.020786945 seconds