SONY

A multi-GNSS receiver

CXD5603GF

Description

The CXD5603GF is a multi-GNSS receiver with a high sensitivity and fast acquisition engine.

The CXD5603GF can operate from a single supply rail from 0.7 V to 1.8 V. Higher supply voltages up to 5.5 V are also possible using a companion PMIC (CXA3846GF). The CXA3846GF has two high efficiency DC-DC converters and very low power RTC (Real Time Clock) and CRYSTAL oscillators.

The CXD5603GF also has integrated digital noise filters and spectrum analyzer, enabling developers to measure against noise and observe the received spectrum in the final product.

A Digitally Controlled Xtal Oscillator (DCXO) is supported.

Features

- A multi-GNSS receiver for GPS, GLONASS, SBAS, QZSS, BeiDou and Galileo
- Ultra-low power consumption
- Embedded noise filters and spectrum analyzer for development
- DCXO ready

Contents

Package

XFBGA-49Pin (WLCSP)

Structure

Silicon-Gate CMOS IC

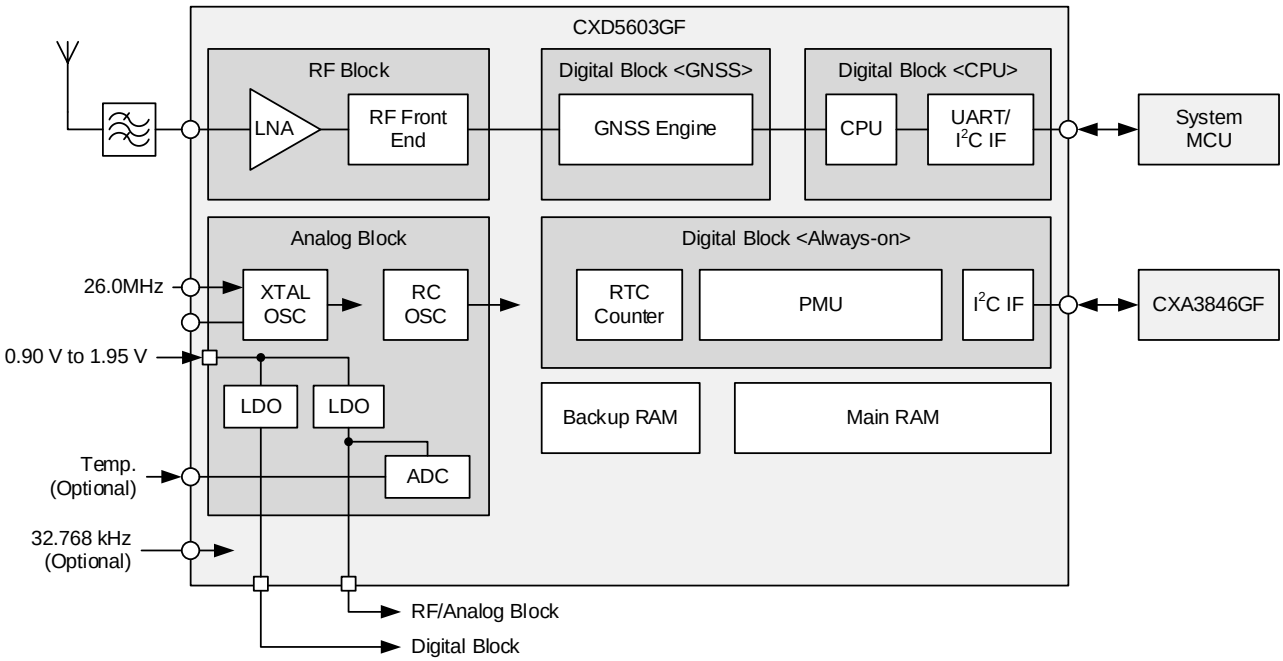
Absolute Maximum Ratings

Item	Min.	Max.	Unit
I/O supply voltage	-0.3	2.5	V
Supply voltage	-0.3	1.4	V
Digital input voltage (except Failsafe Mode)	-0.3	IO supply voltage + 0.3	V
Digital input voltage (Failsafe Mode)	-0.3	2.2	V
Analog input voltage	-0.3	IO supply voltage + 0.3	V
Storage temperature	-65	150	˚C

Recommended Operating Conditions

Item		Min.	Typ.	Max.	Unit
I/O supply voltage(VDD_IO0, VDD_IO1, VDD_IO_ANA)		1.65	1.80	1.95	V
Supply voltage	VDD_CORE (for digital block)	0.65	0.70	0.75	V
	VDDA_LNA, VDDA_LO, VDDA_ANA, VDDA_XOSC and LDO0_OUT(for analog blocks)	0.65	0.70	0.75	V
	LDO_IN	0.90	—	1.95	V
Noise level @1kHz to 3MHz	VDD_IO_ANA	—	—	10	mVpp
	LDO_IN	—	—	20	mVpp
	VDDA_LNA, VDDA_LO, VDDA_ANA, VDDA_XOSC and LDO0_OUT	—	—	50	µVpp
Operating temperature		-25	25	85	˚C

Block Diagram



Pin Description

List

Pin#	Pin Name	Type	I/O	IO Power Supply	Reset State	Description
A1	RF_IN	Analog	Input	VDD_IO_ANA	—	GNSS RF signal input
A2	VDDA_LNA	Power	—	—	—	Analog block (LNA) power
A3	VSSA_ANA	GND	—	—	—	Analog blocks GND
A4	VDD_IO_ANA	Power	—	—	—	Analog IO power
A5	P02 / UART0_CTS	Digital	In/Out	VDD_IO0	Hi-Z	UART CTS (Host IF) / interrupt to Host IF (I^2C)
A6	P03 / UART0_RTS	Digital	In/Out	VDD_IO0	Hi-Z	UART RTS (Host IF)
A7	VDD_IO0	Power	—	—	—	VDD_IO0 domain IO power
B1	VSSA_LNA	GND	—	—	—	Analog block (LNA) GND
B2	VSSA_LO	GND	—	—	—	Analog block (Local OSC) GND
B3	VDDA_LO	Power	—	—	—	Analog block (Local OSC) Power
B4	VSSA_AIN	GND	—	—	—	Analog IO GND
B5	TEST0	Digital	Input	VDD_IO1	Hi-Z	Tied to GND
B6	P00 / UART0_TXD / I2C0_SCL	Digital	In/Out	VDD_IO0	Hi-Z	UART TX (Host IF) / I^2C SCL (Host IF / Slave)
B7	P01 / UART0_RXD / I2C0_SDA	Digital	In/Out	VDD_IO0	Hi-Z	UART RX (Host IF) / I^2C SDA (Host IF / Slave)
C1	TSENS_IN	Analog	Input	VDD_IO_ANA	—	Input from crystal thermistor

Pin#	Pin Name	Type	I/O	IO Power Supply	Reset State	Description
C2	VSSA_XOSC	GND	—	—	—	Analog blocks (Crystal OSC) GND
C3	VDDA_ANA	Power	—	—	—	Analog blocks power
C4	P07 / PMIC_INT	Digital	In/Out	VDD_IO1	Hi-Z	TCXO enabler / Interrupt input from CXA3846GF
C5	P05 / GPS_EXTLD	Digital	In/Out	VDD_IO0	Hi-Z	Timing signal input (from 3G, LTE Modem)
C6	VSS	GND	—	—	—	Digital block VSS
C7	P04 / CLK_EXTREF_IN / 1PPS_OUT	Digital	In/Out	VDD_IO0	Hi-Z	Reference clock (clock bias known) input / 1PPS out
D1	XOSC_OUT	Analog	In/Out	VDD_IO_ANA	—	Crystal OSC
D2	XOSC_IN	Analog	In/Out	VDD_IO_ANA	—	Crystal OSC / Clock input from TCXO
D3	VDDA_XOSC	Power	—	—	—	Analog blocks (Crystal OSC) power
D4	P17 / RTC_IRQ_OUT	Digital	In/Out	VDD_IO1	Hi-Z	External LNA enabler / Interrupt output to CXA3846GF
D5	SYSTEM0	Digital	Input	VDD_IO1	Hi-Z	BOOT MODE
D6	SYSTEM1	Digital	Input	VDD_IO1	Hi-Z	BOOT MODE
D7	VDD_IO1	Power	—	—	—	VDD_IO1 domain IO power
E1	LDO0_OUT	Analog	In/Out	VDD_IO_ANA	—	LDO output for analog blocks
E2	VSSA_RCOSC	GND	—	—	—	Analog blocks GND
E3	P15 / I2C1_SDA	Digital	In/Out	VDD_IO1	Hi-Z	I^2C SDA (CXA3846GF IF / Master)
E4	P14 / I2C1_SCL	Digital	In/Out	VDD_IO1	Hi-Z	I^2C SCL (CXA3846GF IF / Master)
E5	VSS	GND	—	—	—	Digital block VSS
E6	P06 / BOOT_REC	Digital	In/Out	VDD_IO1	Pull-down	BOOT Recovery (Normally tied to GND)
E7	VSS	GND	—	—	—	Digital block VSS
F1	LDO_IN	Analog	Input	VDD_IO_ANA	—	LDO0 / LDO1 input
F2	LDO_EN	Analog	Input	VDD_IO_ANA	—	LDO0 / LDO1 enabler
F3	P11 / SPI1_IO1	Digital	In/Out	VDD_IO1	Hi-Z	FLASH memory interface (SPI IO1 / Master)
F4	P12 / SPI1_IO2	Digital	In/Out	VDD_IO1	Hi-Z	FLASH memory interface (SPI IO2 / Master)
F5	P16 / SEN_IRQ_IN	Digital	In/Out	VDD_IO1	Hi-Z	Interrupt input
F6	RST_X	Digital	Input	VDD_IO1	Hi-Z	Reset input
F7	RTC_CLK_IN	Digital	Input	VDD_IO1	Hi-Z	RTC clock input
G1	P13 / SPI1_IO3	Digital	In/Out	VDD_IO1	Hi-Z	FLASH memory interface (SPI IO3 / Master)
G2	P10 / SPI1_IO0	Digital	In/Out	VDD_IO1	Hi-Z	FLASH memory interface (SPI IO0 / Master)
G3	P09 / SPI1_SCK	Digital	In/Out	VDD_IO1	Hi-Z	FLASH memory interface (SPI CLK / Master)

Pin#	Pin Name	Type	I/O	IO Power Supply	Reset State	Description
G4	P08 / SPI1_CS_X	Digital	In/Out	VDD_IO1	Hi-Z	FLASH memory interface (SPI CS / Master)
G5	LDO1_OUT	Analog	Output	VDD_IO_ANA	—	LDO output for digital block
G6	VDD_CORE	Power	—	—	—	Digital block power
G7	VDD_CORE	Power	—	—	—	Digital block power

Failsafe Mode

Digital pins are in failsafe mode when the interface supply (VDD_IO0 or VDD_IO1) is grounded(less than 50 mV and Hi-Z is NOT acceptable), while the core supply (VDD_CORE) may or may not be available. If the pins are in failsafe mode and connected to 1.95 V, protection circuits prevent any unwanted leak current from the pins.

Unused Pin Terminations

XOSC_OUT

The XOSC_OUT should be open if the crystal oscillator is not used.

LDO1_OUT

The LDO1_OUT should be open if the LDO1 is not used. However LDO0_OUT should be tied to analog 0.7 V even if the LDO0 is not used.

Description of Functions

Support Satellite Systems

- GPS (L1 C/A)
- GLONASS (L1OF)
- QZSS (L1 C/A)
- SBAS (L1 C/A)
- BeiDou (B1)[1]
- Galileo (E1 CBOC)[1]

Position Accuracy[2,3]

Item	GPS	GPS & GLONASS	Unit
2DRMS	2.5	2.5	m

Time-To-First-Fix (TTFF)[2, 3]

Item	GPS	GPS & GLONASS	Unit

[1] Planned for the future. Please contact your local sales representative for details.
[2] Signal strength is -130 dBm

Item	GPS	GPS & GLONASS	Unit
Cold Start	35	35	s
Hot Start	2	2	s

Sensitivity[3]

Item	GPS	GPS & GLONASS	Unit
Cold Start	-147	-147	dBm
Hot Start	-160	-160	dBm
Tracking	-165	-165	dBm

Noise Filter

An embedded noise filter for GNSS signals. It is automatically enabled at the optimum settings for the input noise.

RF Performance

Item	Min.	Typ.	Max.	Unit	Remark
Total NF	—	3	—	dB	

Internal LDO

Embedded LDOs are provided for each internal power supply block. They should be used if supply voltage is provided by some source other than the CXA3846GF in order to reduce noise on the supply lines.

LDO0 and LDO1 have same spec as follows.

Item	Min.	Typ.	Max.	Unit	Remark
Input voltage	0.90	—	1.95	V	Even if the LDOs are not used, LDO_IN must be this input voltage level.
Output voltage	0.65	0.70	0.75	V	

The LDO0 is for analog powers and the LDO1 is for digital block powers.

If the LDOs are not used, the LDO_EN pin must be tied to GND and LDO_IN pin must be tied to VDD_IO_ANA.

Power-on reset

An internal power-on reset circuit enables autonomous startup without external reset control by the system. To avoid malfunction in boot-up, power-off state must be more than 100 ms.

Internal clock oscillators

Crystal oscillator

This oscillator handles19.2 MHz crystal and creates a clock for the PLL. It also has a buffer mode for the TCXO signal input and the frequency is 26.0 MHz.

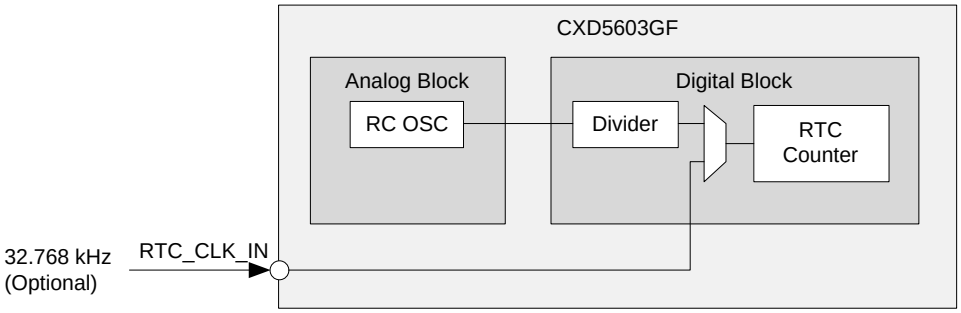
[3] Test circuit is shown at p.18.

RC oscillator

A clock from this oscillator is used for the power management unit and RTC counter (if there is no external RTC clock).

RTC clock

RTC counter maintains GNSS time and is used for the system wakeup/sleep timer function. Its clock sources are the RC oscillator or the RTC_CLK_IN pin with 32.768 kHz.



Because the clock from the RC oscillator is calibrated for the RTC counter but it may have frequency drift by temperature during sleep states (the calibration is done at S0: Exec[4] and S1: Idle states[4]), the sleep time also may be drifted.

Interfaces

Host MCU interface

The following are provided as interfaces to the host MCU.

- UART: up to 2.00 Mbps
- I^2C[5]: Standard mode(100 kbps), Fast mode(400 kbps) and Fast mode plus(1 Mbps)

The interface selection is set by the SYSTEM0 and SYSTEM1 pins.

SYSTEM1	SYSTEM0	Selected interface
0	0	I^2C
0	1	UART
1	0	Reserved
1	1	Reserved

CXA3846GF interface

This is an I^2C interface with normal mode and fast mode. It is provided as an interface for the CXA3846GF.

FLASH memory interface

SPI1 is for an external FLASH memory. The max clock frequency is 39 MHz

1PPS output

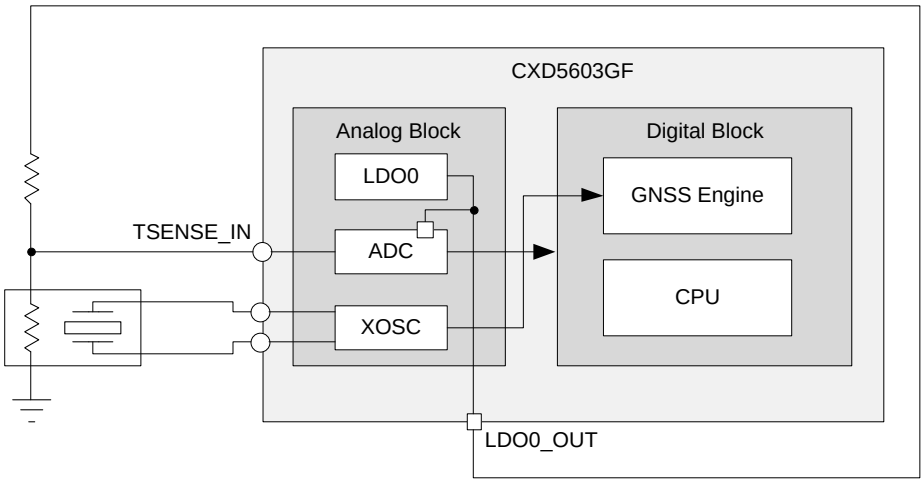
A 1PPS (pulse per second) signal is synchronized in the GPS time. P04/CLK_EXTREF_IN/1PPS_OUT can be used for

[4] Please see “Description of Operation” at p.10
[5] Planned for the future. Please contact your local sales representative for details.

1PPS outputs.

ADC (Analog to Digital Converter)

An ADC is used for temperature measurements with a thermistor in a crystal oscillator for DCXO implementations.



Recovery pin

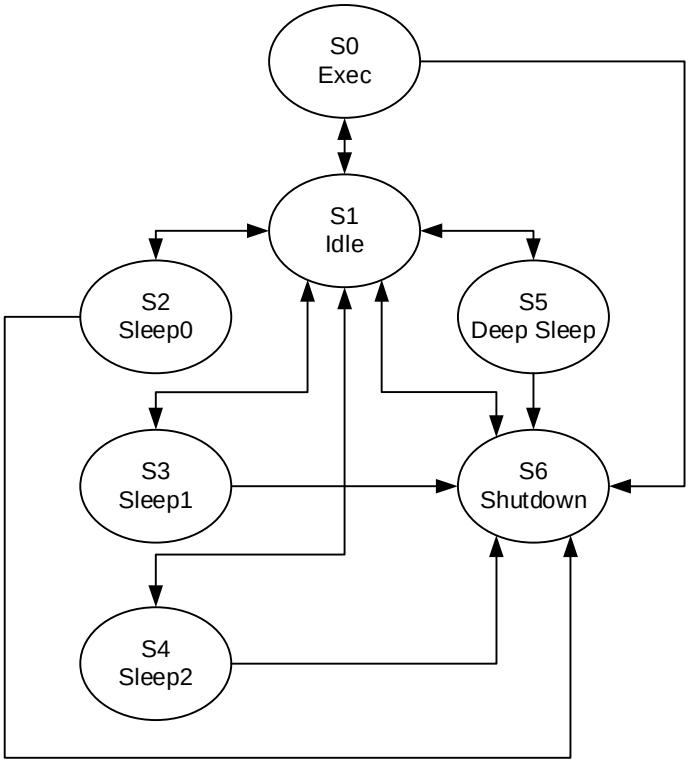
When P06/BOOT_REC pin is high at power-on sequence[6], the CXD5603GF doesn't read a firmware on the FLASH memory to over-write it. Please refer to the "CXD5603GF User's Manual" for details.

Description of Operation

State Transition

There are some states in the CXD5603GF and the CXA3846GF operations as shown in the following diagram. If the CXA3846GF is not used, the system doesn't go to "S5" or "S6".

[6] See AC characteristics - Power-on / Power-off, p.17



State	CXD5603GF					CXA3846GF		
	GNSS	CPU	Always-on block	Backup RAM	Main RAM	CE Pin	RTC Counter	Registers
S0: Exec	Operation	Operation	Operation	Hold	Hold	H	Operation	Hold
S1: Idle	Standby	Operation	Operation	Hold	Hold	H	Operation	Hold
S2: Sleep0	Power-off	Power-off	Operation	Hold	Hold	H	Operation	Hold
S3: Sleep1	Power-off	Power-off	Operation	Hold	Power-off	H	Operation	Hold
S4: Sleep2	Power-off	Power-off	Operation	Power-off	Power-off	H	Operation	Hold
S5: Deep Sleep	Power-off	Power-off	Power-off	Power-off	Power-off	H	Operation	Hold
S6: Shutdown	Power-off	Power-off	Power-off	Power-off	Power-off	L	Off	Off

State Description

S0: Exec

GNSS positioning can be performed.

S1: Idle

This is a command waiting state. The system can accept commands but power consumption is managed to be low.

S2: Sleep0

The CXD5603GF holds program code, data and satellite date but other logic circuit is powered off. The CXD5603GF can wake up from this state without loading the data from an external FLASH memory or the system MCU.

S3: Sleep1

Because the CXD5603GF holds satellite data only in this state, it must load program data from an external FLASH memory or the system MCU for wake-up but it can get a position with hot start.

S4: Sleep2

In this state, the CXD5603GF is powered off except an internal PMU and always-on block.

S5: Deep Sleep

In this state, the CXD5603GF is powered off but the CXA3846GF holds its RTC counter and backup registers.

S6: Shutdown

The CE pin of the CXA3846GF is low in this state. All functions are off but the leakage current is very low.

Please refer to the “CXD5603GF User’s Manual” for details.

Electrical Characteristics

DC Characteristics

Digital IO

Item		Symbol	Min.	Typ.	Max.	Unit
Input voltage	H level	V_{IH}	0.65 × IO supply voltage	—	IO supply voltage + 0.3	V
	L level	V_{IL}	-0.3	—	0.35 × IO supply voltage	V
Output voltage	H level	V_{OH}	0.8 × IO supply voltage	—	—	V
	L level	V_{OL}	—	—	0.2 × IO supply voltage	V
Drivability	H level @V_{OH}(Min.)	I_{OH}	2	—	—	mA
	L level @V_{OL} (Max.)	I_{OL}	2	—	—	mA
Pull-up resistance		R_{PU}	30	—	70	kΩ
Capacitance		C_{BL}	—	—	5	pF

Analog IO

- LDO_EN

Item		Symbol	Min.	Typ.	Max.	Unit
Input voltage	H level	V_{IH}	0.8 × IO supply voltage	—	IO supply voltage + 0.3	V
	L level	V_{IL}	-0.3	—	0.3	V

- Except above

Item	Symbol	Min.	Typ.	Max.	Unit
Input voltage	V_I	—	—	Recommended operating supply voltage	V
Output voltage	V_O	—	—	Recommended operating supply voltage	V

Current consumption / Core[7]

Item	State	Symbol	Min.	Typ.	Max.	Unit	Remark
Max load	—	MAX	—	—	55	mA	
Satellite acquisition	S0: Exec	GNS_{ACQ}	—	16	—	mA	
Satellite tracking		GNS_{TRK}	—	8	—	mA	8-ch tracking
Idle	S1: Idle	IDLE	—	4	—	mA	Waiting for command
Sleep0	S2: Sleep0	SLP_0	—	0.24	—	mA	
Sleep1	S3: Sleep1	SLP_1	—	0.20	—	mA	
Sleep2	S4: Sleep2	SLP_2	—	0.18	—	mA	
Deep Sleep[8]	S5: Deep Sleep	DSLP	—	—	0	µA	CXA3846GF cuts all power of CXD5603GF's core
Shut down[8]	S6: Shutdown	SD	—	—	0	µA	

Current consumption / LDO[9]

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
LDO_IN	$LDO_{EN\_LDO\_IN}$	—	10	50	µA	LDO_EN: VDD_IO_ANA LDO is enabled
	$LDO_{DIS\_LDO\_IN}$	—	0.5	5	µA	LDO_EN: GND LDO is disabled

Current consumption / IO

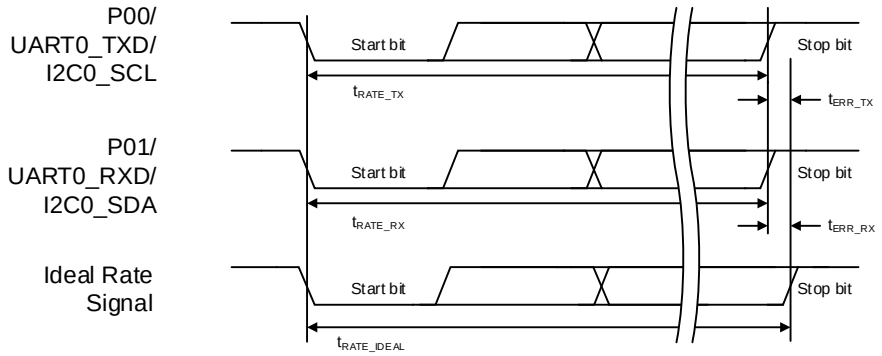
Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Digital IO Vdd leak (VDD_IO0, VDD_IO1)	IO_D	—	—	50	µA	IO drive current is not included
Analog IO Vdd leak (VDD_IO_ANA)	$IO_{A\_LDO\_EN}$	—	60	150	µA	LDO is enabled
	$IO_{A\_LDO\_DIS}$	—	5	50	µA	LDO is disabled

AC characteristics

V_{Min} in the diagrams below is the minimum recommended operating voltage for each power supply. In addition, items that specify a time difference are positive in the direction following the reference timing.

[7] Sum of VDD_CORE, VDDA_LNA, VDDA_LO, VDDA_ANA, VDDA_XOSC and LDO0_OUT current
[8] Please refer to the CXA3846GF data sheet for the its core current
[9] Sum of VDD_IO_ANA of LDO0/1

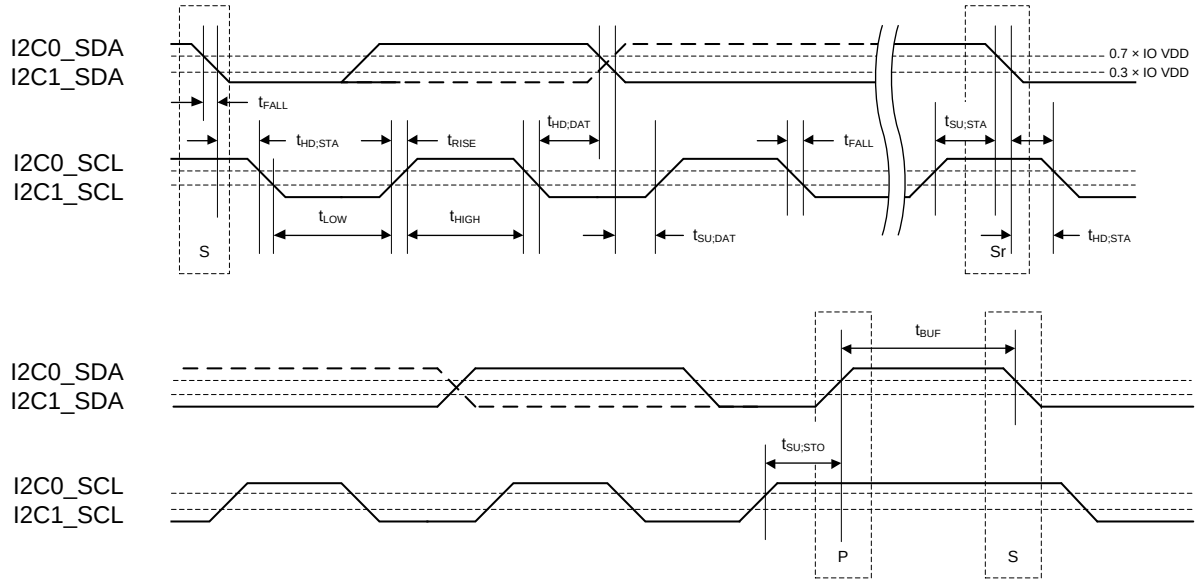
UART (Host interface)



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
UART Error Rate (except TX @ 115.2 kbps)	R_{BRT_ERR}	-1	—	1	%	t_{ERR_TX} / t_{RATE_IDEAL} t_{ERR_RX} / t_{RATE_IDEAL}
UART Error Rate (TX @ 115.2kbps)	$R_{BRT\_ERR\_FD\_TX}$	-4	—	4	%	t_{ERR_TX} / t_{RATE_IDEAL}

These timing budgets are changed by PCB (Printed Circuit Board) design. Please evaluate UART function on your PCB carefully.

I²C (Host interface and CXA3846GF interface)

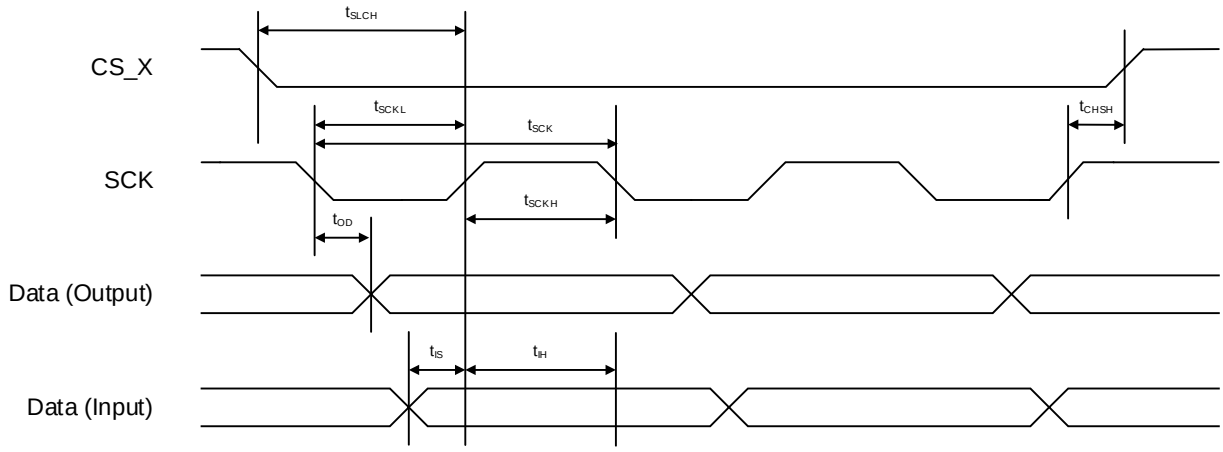


Item	Symbol	Standard-Mode		Fast-Mode		Fast-Mode Plus[10]		Unit	Remarks
		Min.	Max.	Min.	Max.	Min.	Max.		
SCL clock frequency	f_{SCL}	0	100	0	400	0	1000	kHz	—
HOLD time (repeated) START condition	$t_{HD;STA}$	4	—	0.6	—	0.26	—	us	—

[10] Host Interface only

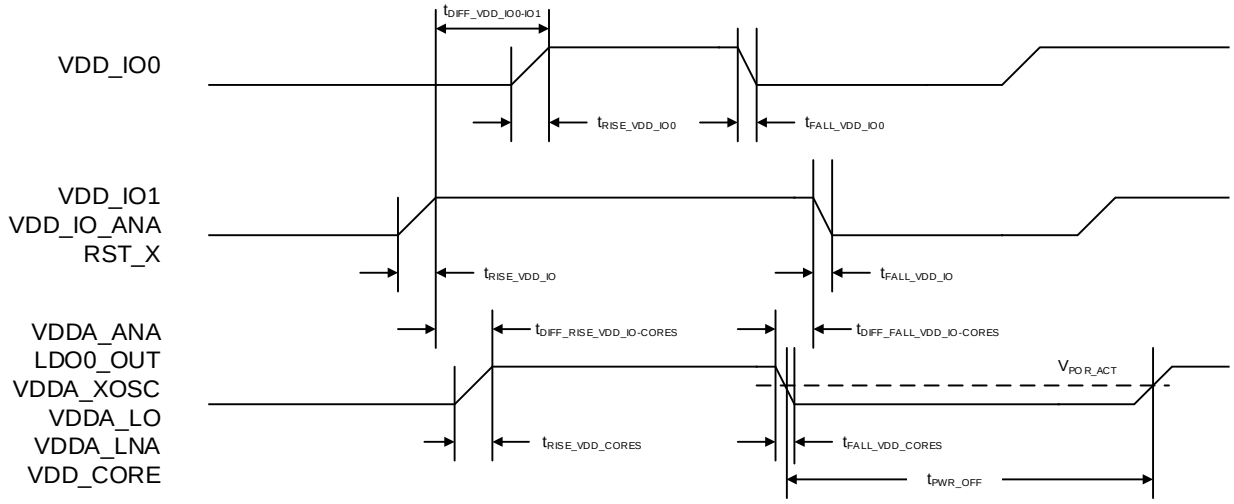
Item	Symbol	Standard-Mode		Fast-Mode		Fast-Mode Plus[10]		Unit	Remarks
		Min.	Max.	Min.	Max.	Min.	Max.		
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	0.5	—	us	—
LOW period of the SCL clock	t_{HIGH}	4	—	0.6	—	0.26	—	us	—
Setup time for a repeated START condition	$t_{SU;STA}$	4.7	—	0.6	—	0.26	—	us	—
Data hold time	$t_{HD;DAT}$	0	—	0	—	-	—	us	—
Data setup time	$t_{SU;DAT}$	250	—	100	—	50	—	ns	—
Rise time of both SDA and SCL signals	t_{RISE}	—	1000	20	300	—	120	ns	—
Fall time of both SDA and SCL signals	t_{FALL}	—	300	—	300	—	120	ns	—
Setup time for STOP condition	$t_{SU;STO}$	4	—	0.6	—	0.26	—	us	—
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	0.5	—	us	—
Capacitive load for each bus line	C_L	—	73	—	73	—	29	pF	4.7 kΩ Pull-up

External FLASH memory interfaces



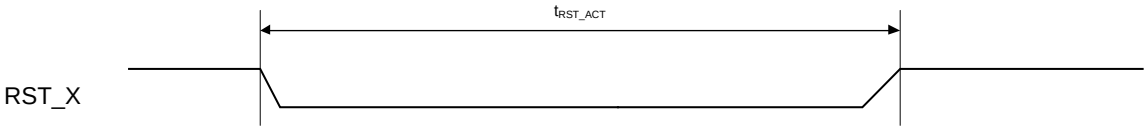
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
SCK Period	t_{SCK}	—	25.6	—	ns	39MHz
SCK Duty Ratio	t_{SCKH} / t_{SCK} (t_{SCKL}/t_{SCK})	40	50	60	%	—
CS_X active setup time	t_{SLCH}	7	—	—	ns	—
CS_X active hold time	t_{CHSH}	5	—	—	ns	—
IO Output Delay Time	t_{OD}	-10.36	—	12.86	ns	—
IO Input Setup Time	t_{IS}	0	—	—	ns	—
IO Input Hold Time	t_{IH}	15.36	—	—	ns	—

Power-on / Power-off



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Time difference from VDD_IO1 and VDD_IO_ANA rise to VDD_IO0	$t_{DIFF\_VDD\_IO0\text{-}IO1}$	—	—	—	ms	—
VDD_IO0 rise time	$t_{RISE\_VDD\_IO0}$	—	—	—	ms	—
VDD_IO0 fall time	$t_{FALL\_VDD\_IO0}$	—	—	—	ms	—
Power off period	t_{PWR_OFF}	100	—	—	ms	—
VDD_IO1, VDD_IO_ANA and RST_X rise time	$t_{RISE\_VDD\_IO}$	—	—	—	ms	—
VDD_IO1, VDD_IO_ANA and RST_X fall time	$t_{FALL\_VDD\_IO}$	—	—	—	ms	—
Time difference from VDD_IO1 and VDD_IO_ANA rise to VDD Cores[11]	$t_{DIFF\_RISE\_VDD\_IO\text{-}CORES}$	0	—	—	ms	—
Time difference from VDD_IO1 and VDD_IO_ANA fall to VDD Cores	$t_{DIFF\_FALL\_VDD\_IO\text{-}CORES}$	0	—	—	ms	—
VDD Cores rise time	$t_{RISE\_VDD\_CORES}$	0.08	—	4.00	ms	Keep monotonically increasing
VDD Cores fall time	$t_{FALL\_VDD\_CORES}$	—	—	—	ms	Keep monotonically decreasing
POR activating voltage	V_{POR_ACT}	—	—	50	mV	

Reset



[11] VDDA_LNA, VDDA_LO, VDDA_ANA, VDDA_XOSC, LDO_OUT0 and VDD_CORE

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
RST assert period	t_{RST_ACT}	100	—	—	ms	—

Clocks

- XOSC_IN (in buffer mode)

Item	Symbol	Min.	Typ.	Max.	Unit
Input voltage range	V_{IN}	0.8	—	1.4	Vpp
Input Frequency	F_{IN}	—	26.0	—	MHz
Input frequency characteristics	F_{IN_C}	-0.5	—	0.5	ppm
Duty Cycle	D_C	40	—	60	%

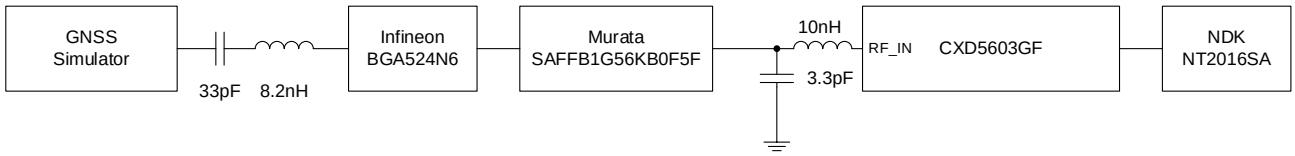
- XOSC_IN / XOSC_OUT (in oscillator mode)

Item	Symbol	Min.	Typ.	Max.	Unit
Frequency	F_{IN}	—	19.2	—	MHz
Frequency tolerance@25˚C	F_{IN_T}	-20	—	20	ppm
Frequency characteristics over temperature	F_{IN_C}	-12	—	12	ppm
Phase noise@1 kHz	P_N	—	-125	—	dBc/Hz
Harmonics Distortion	D_H	—	—	-8	dBc

- RTC_CLK_IN

Item	Symbol	Min.	Typ.	Max.	Unit
Input Frequency	F_{IN}	—	32.768	—	kHz
Frequency Tolerance	F_{IN_T}	-300	—	300	ppm
Duty Cycle	D_C	5	—	95	%

Test Circuit



Reliability Qualification

ESD Strength

- CDM: ±125 V (JEDEC)
- HBM: ±1000 V (JEDEC)

Moisture Sensitivity Level

MSL1 (JEDEC)

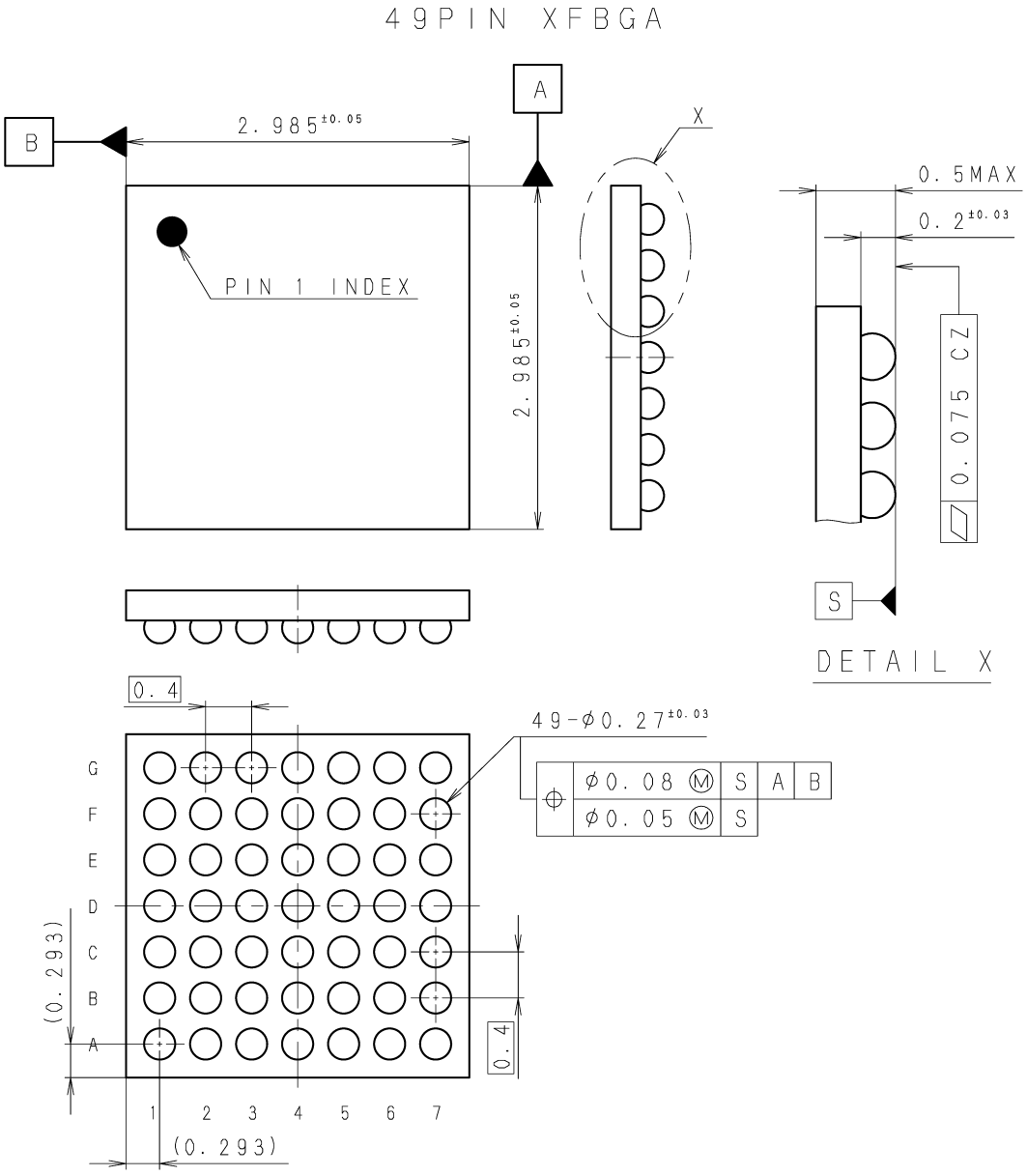
Reflow Profile

IPC/JEDEC J-STD-020

Application Circuit & Recommended Components

Please see to “CXD5603GF Application Note for Hardware Implementation”.

Package Outline



PACKAGE STRUCTURE

SONY CODE	XFBGA-49S-311
JEITA CODE	S-XFBGA49-2.985x2.985-0.4
JEDEC CODE	————

PACKAGE MATERIAL	Si SUBSTRATE
TERMINAL MATERIAL	Sn-4.0Ag-0.5Cu
PACKAGE MASS	0.0087g

PART No. AP-2000-49BGAF1	Rev. 0
ISSUED '15.12.09	REVISED
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR.
REMARKS PKG CODE:GF-49-AAF	

Purpose of Use of the Products:

Customer shall use the Products with the utmost concern for safety, and shall not use the Products for any purpose that may endanger life or physical wellbeing, or cause serious damage to property or the environment, either through normal use or malfunction.
Use of the Products for purposes other than those stipulated in this specification is strictly prohibited.
Furthermore, usage of the Products for military purposes is strictly prohibited at all times.

Safe Design:

- Customer is responsible for taking due care to ensure the product safety design of its products in which the Products are incorporated, such as by incorporating redundancy, anti-conflagration features, and features to prevent mis-operation, in order to prevent accidents resulting in injury, death, fire, or other social damage as a result of failure.

Product Information:

- The product specifications, circuit examples, and any and all other technical information and content contained in this specification, as well as any other information and materials provided to Customer in connection with the Products (collectively, “Product Information”) have been provided to Customer for reference purpose only, and the availability and disclosure of such Product Information and its usage by Customer shall not be construed as giving any indication that Sony, its subsidiaries and/or its licensors will license any right, including intellectual property rights in such Product Information by any implication or otherwise.
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