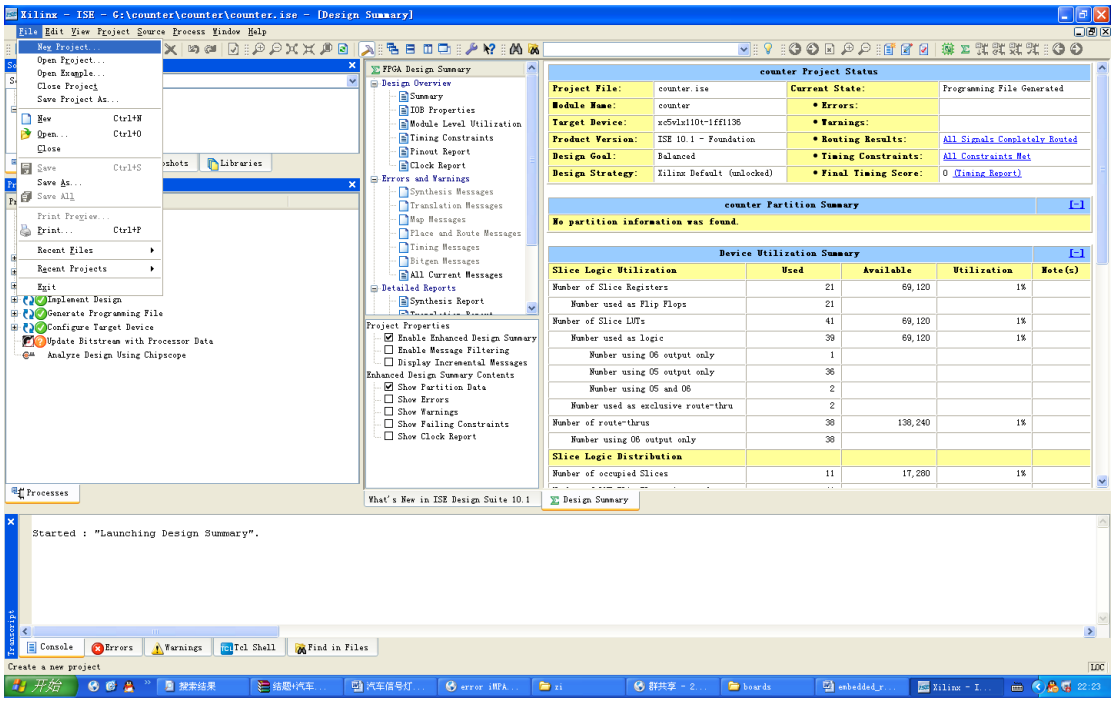
Lab 2. ISE Design Flow-2

Objective:

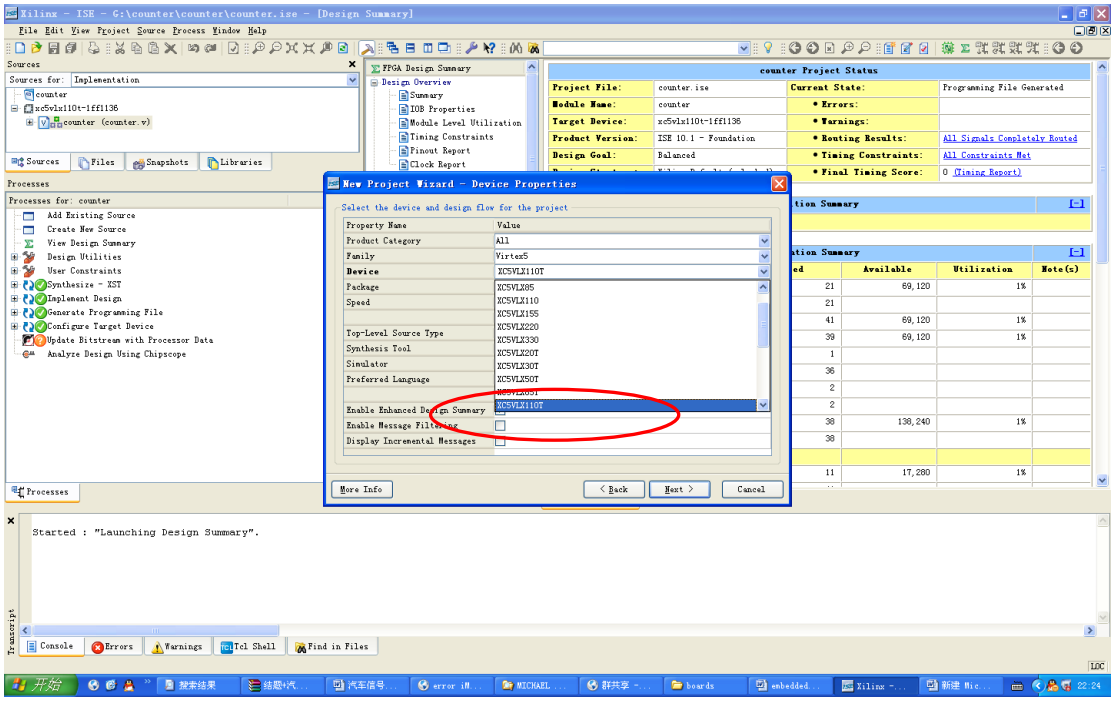
- Learn how to enter IO constraints in ISE.
- Get familiar with synthesis, place and route.
- Understand how to do timing simulation.
- Learn how to configure FPGA with iMPACT .

1. Create a new project.

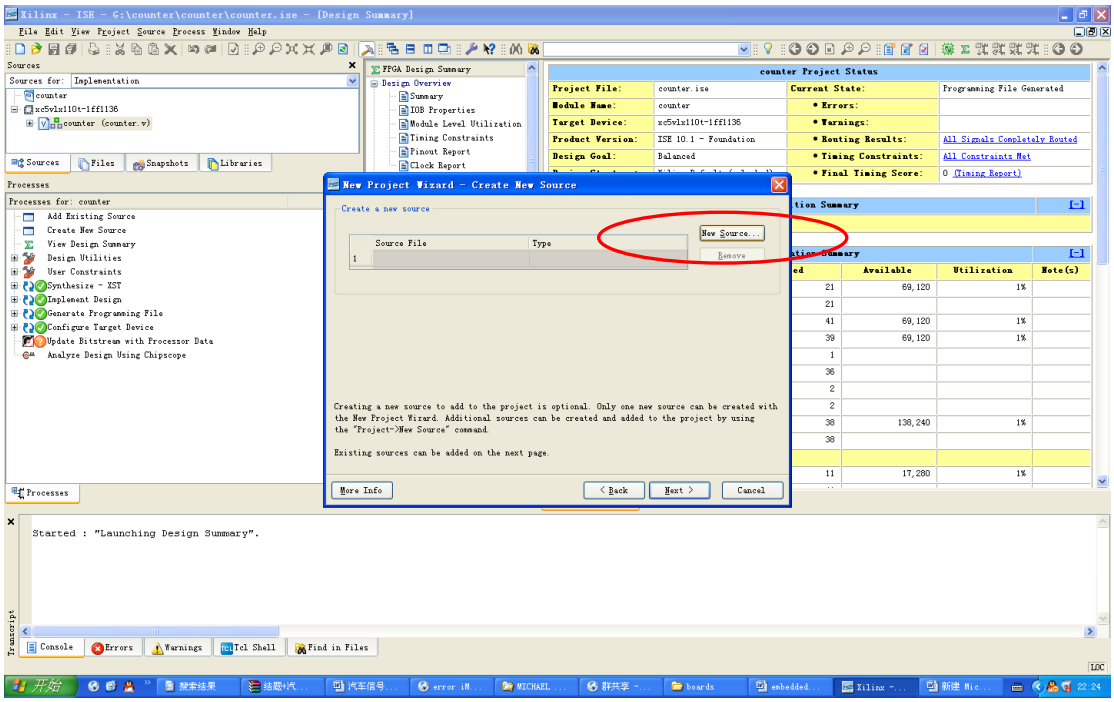


2. Assign the project name and location.

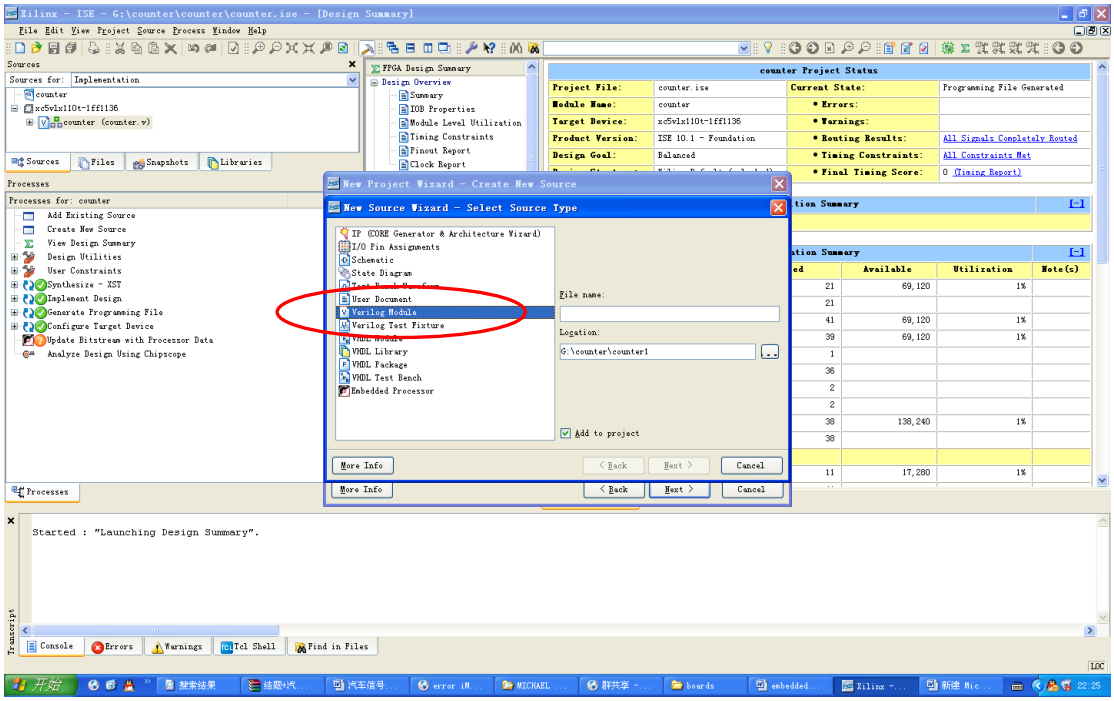
3. Fill in the device type with XC5VLX110T.



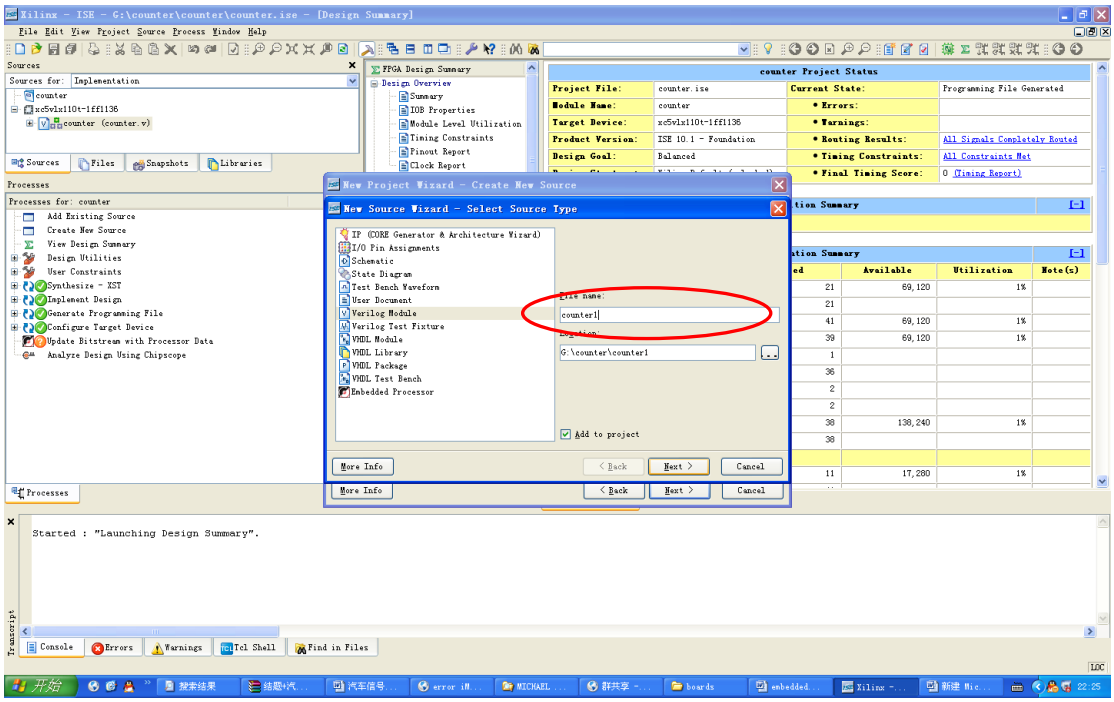
4. Create a Verilog New Source as follows.



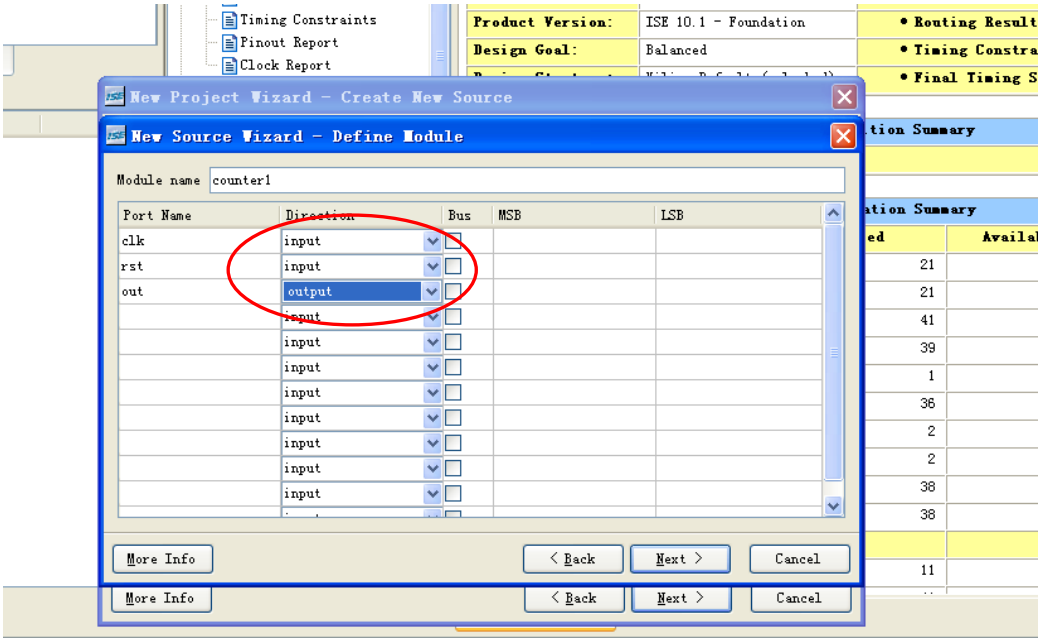
5. Select verilog module as the source type.



6. Type in the file name **counter1**.

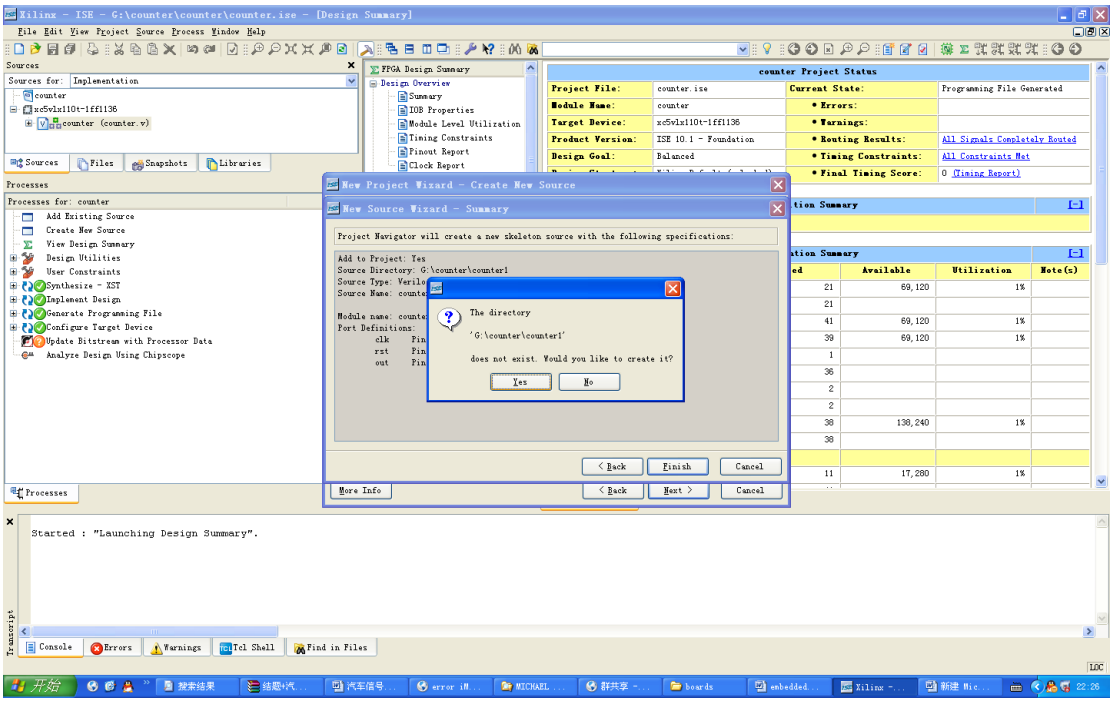


7. Declare the ports for the counter design by filling in the port information as shown below.

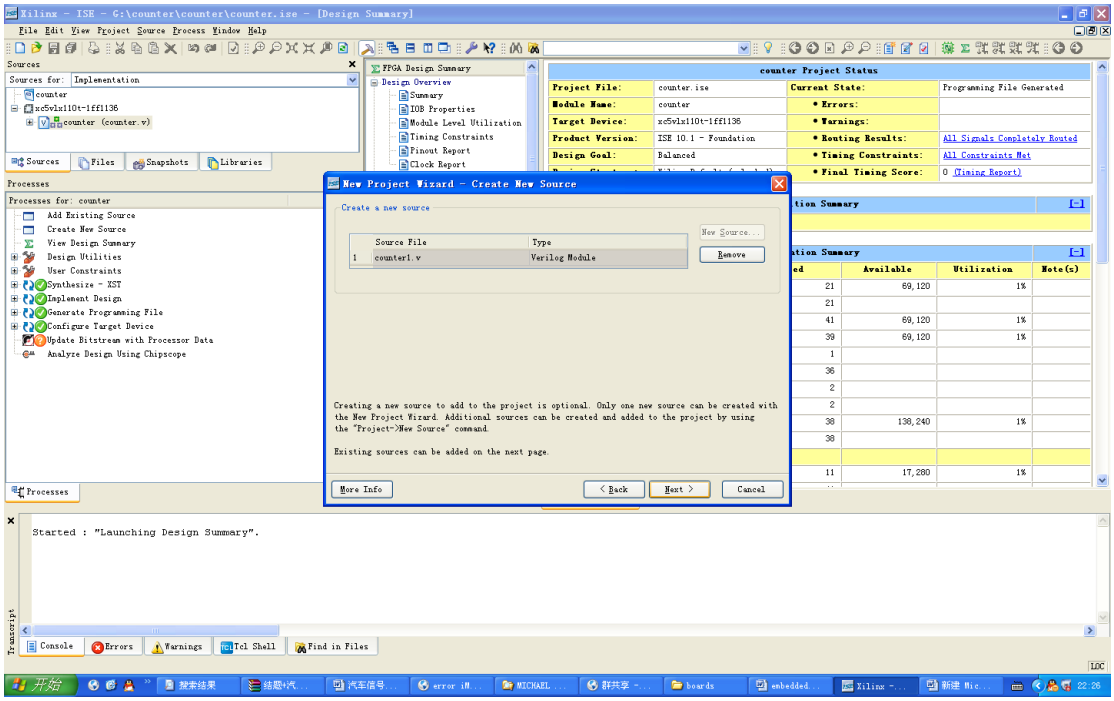


Click next，

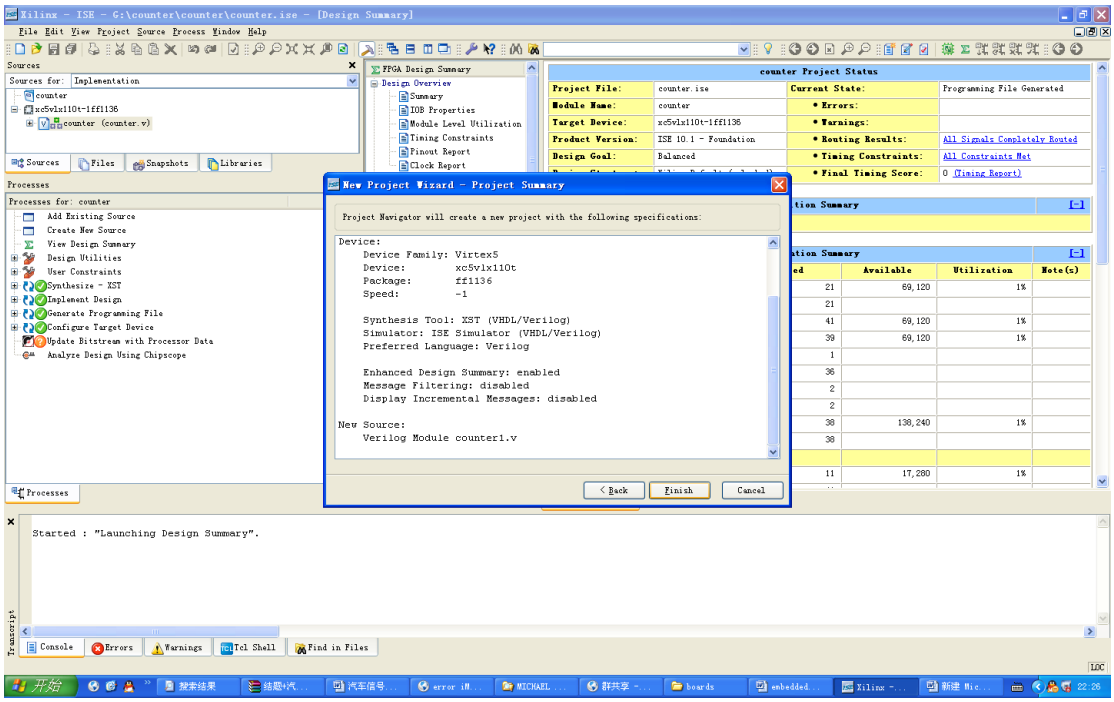
Click yes



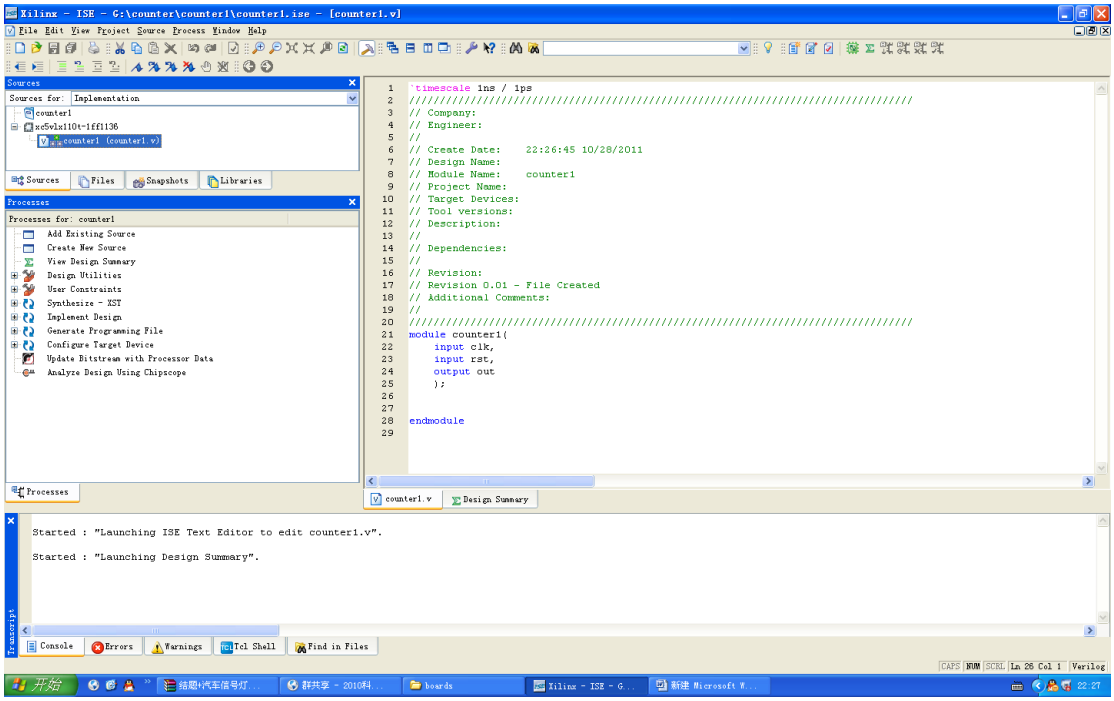
Click next,



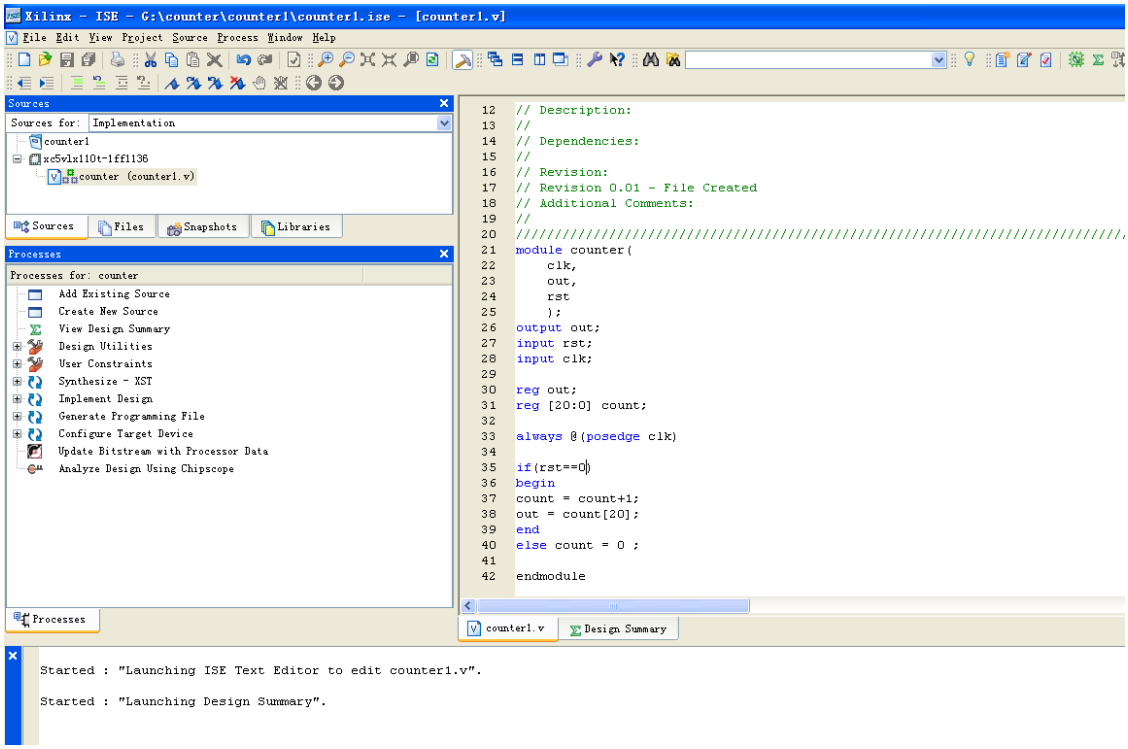
Click finish,



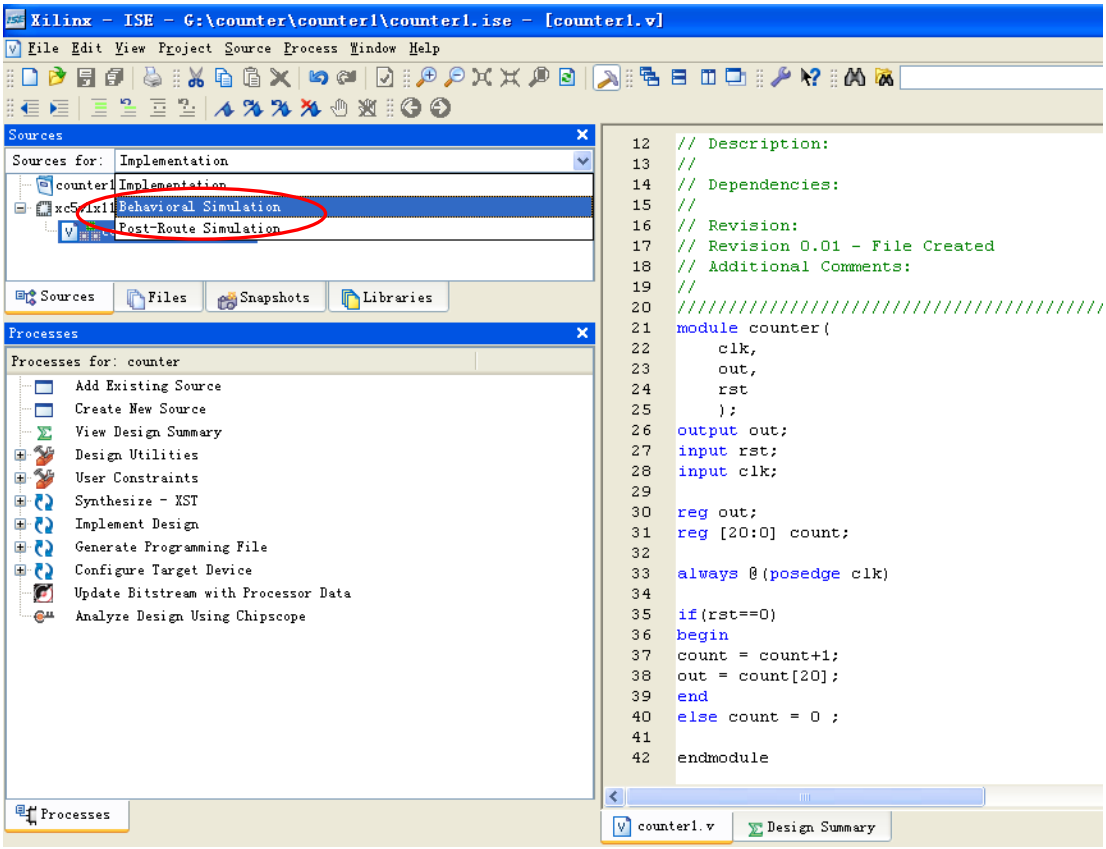
The source file containing the source module displays in the Workspace.



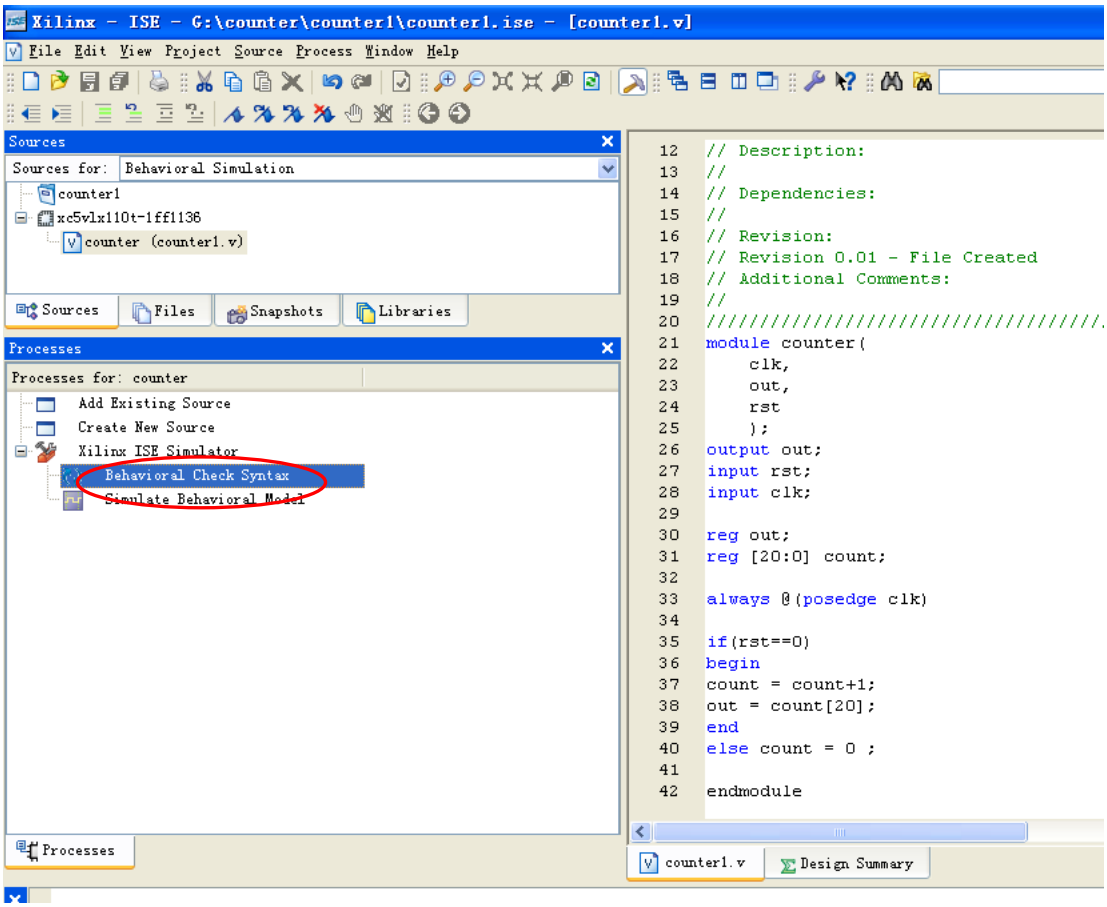
8. Fill the codes as follows.



9. Verify the functionality using Behavioral Simulation:



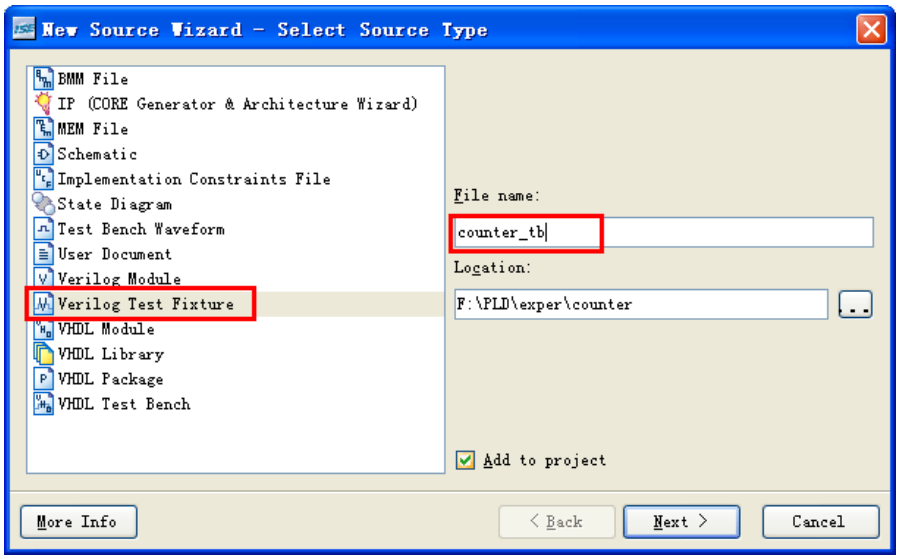
Double click Behavioral Check Syntax to check syntax.



Change the line “out = count[20];” in the source file to “out = count[4];” in order to save the simulation time.

10. Create the test bench by selecting **Project** > **New Source…**

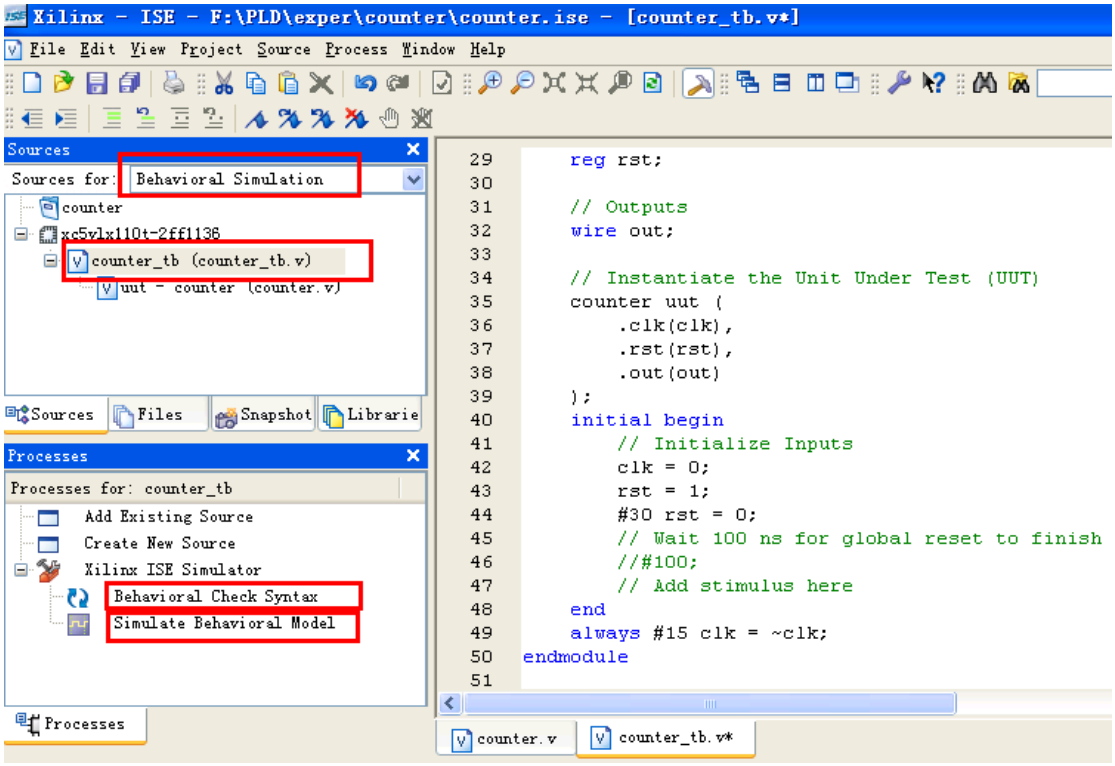
Select **Verilog Test Fixture**，Fill in **File Name**：counter_tb。Click **Next**，**Next**，**Next**，**Finish**。



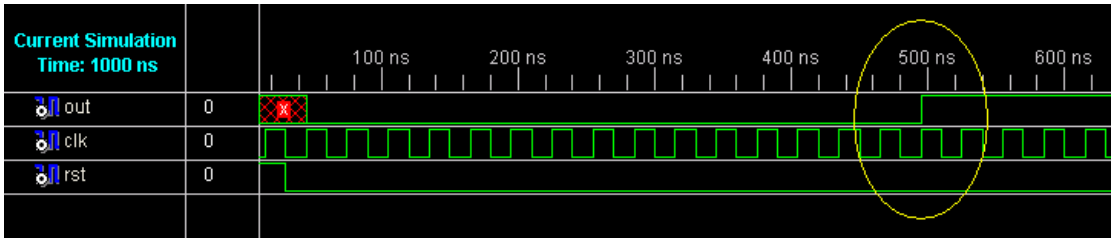
Fill in the code as follows (counter_tb.v).

```
25  module counter_tb;
26
27      // Inputs
28      reg clk;
29      reg rst;
30
31      // Outputs
32      wire out;
33
34      // Instantiate the Unit Under Test (UUT)
35      counter uut (
36          .clk(clk),
37          .rst(rst),
38          .out(out)
39      );
40      initial begin
41          // Initialize Inputs
42          clk = 0;
43          rst = 1;
44          #30 rst = 0;
45          // Wait 100 ns for global reset to finish
46          //#100;
47          // Add stimulus here
48      end
49      always #15 clk = ~clk;
50  endmodule
```

3）In the Sources window, select Sources for: **Behavioral Simulation,** Click counter_tb. In the Process window, click the “+” to expand the Xilinx ISE Simulator process and double **click Simulate Behavioral Model** process as shown in the following.

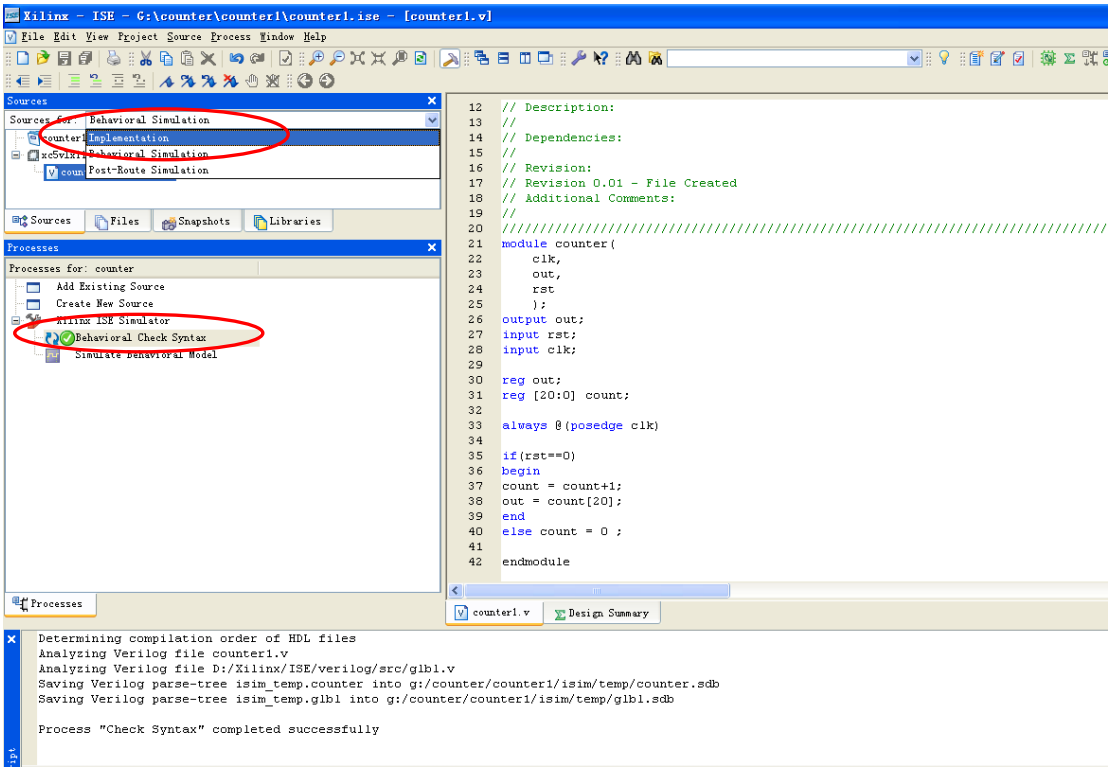


The simulation waveform will look like the following:

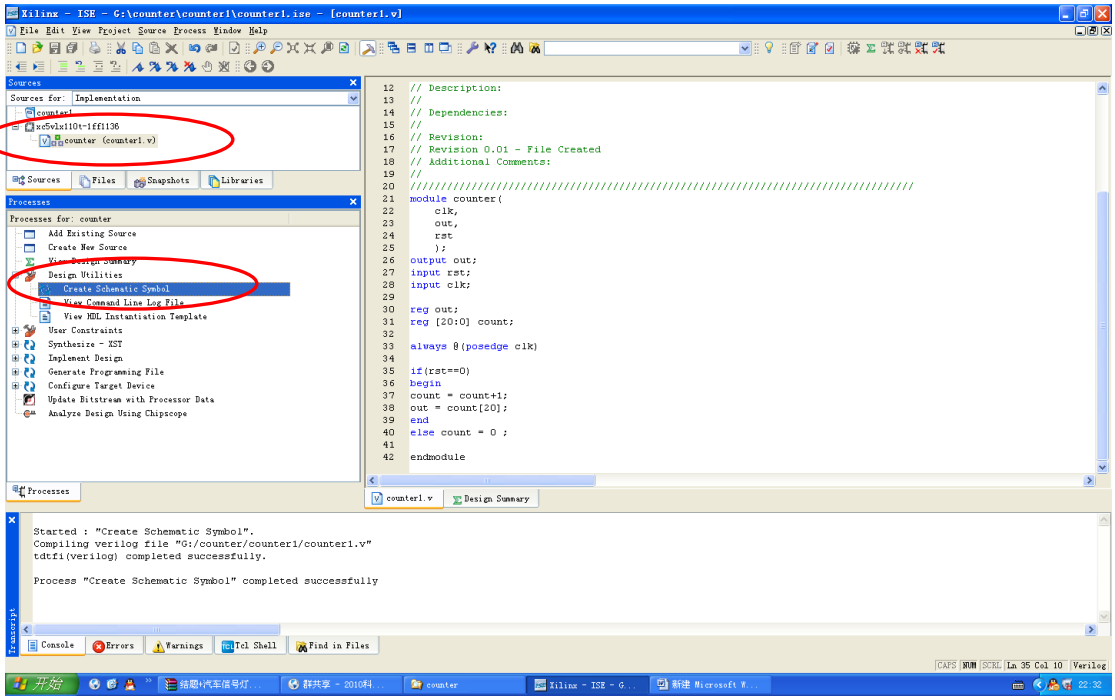


The signal clk flips every 15ns. The period is equal to 30ns。The signal out = count[4] flips every 2^4 periods. The first flip occurs at around 495ns.

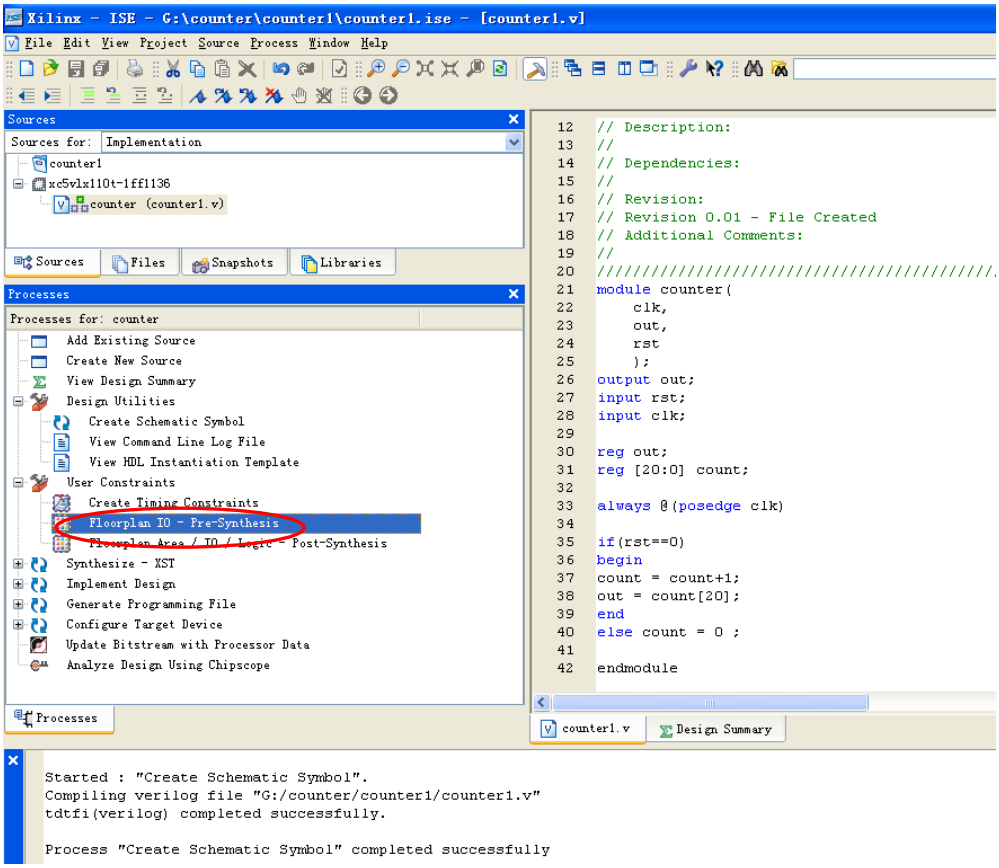
11. Implementing the design. Choose Source for Implementation in the Sources window.



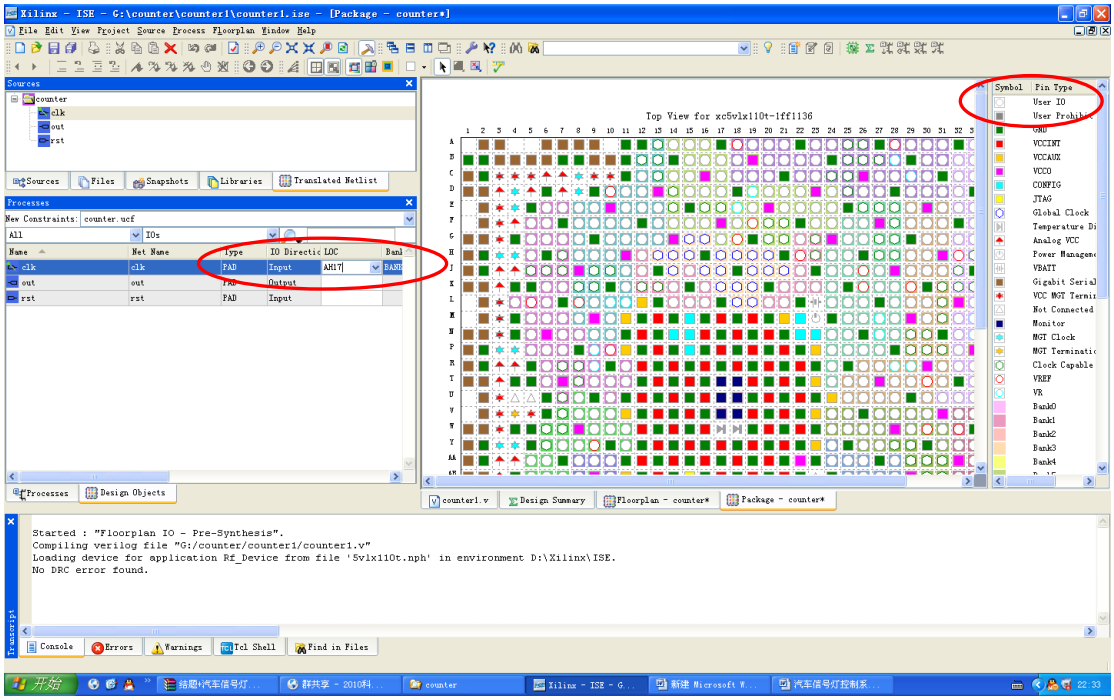
Select the code counter.v，double click“Create schematic symbol ” to generate circuit symbol.（Synthesis is not implemented yet）：

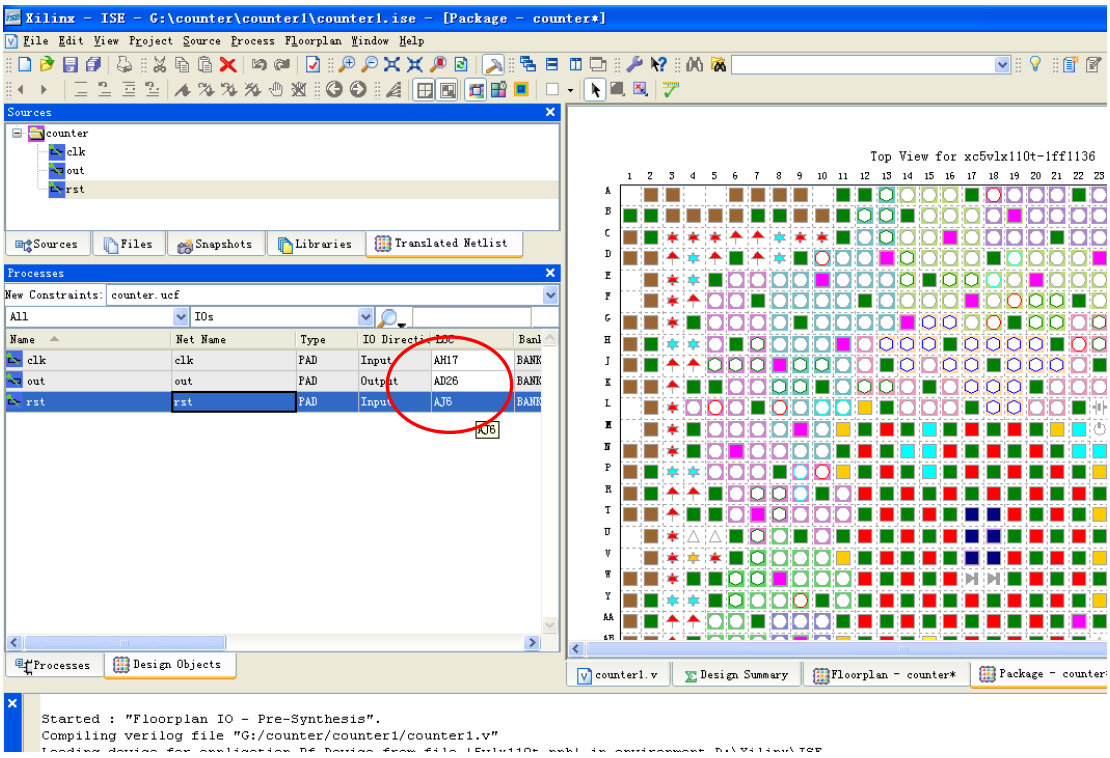


Assign pin locations：



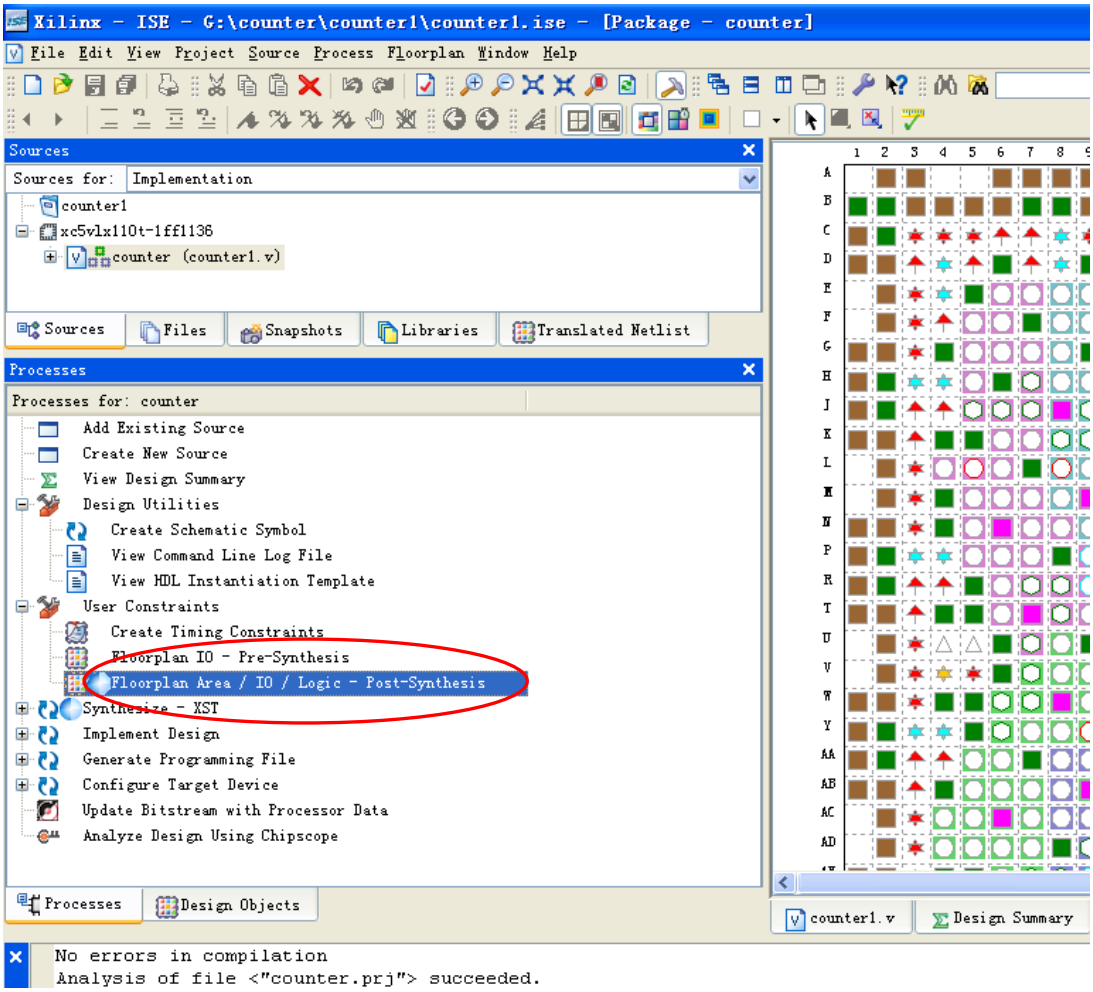
Specify the pin locations as follows.（You can also assign the pin using the diagram）:





Click save button to save the file.

Double click Floor.... as follows,



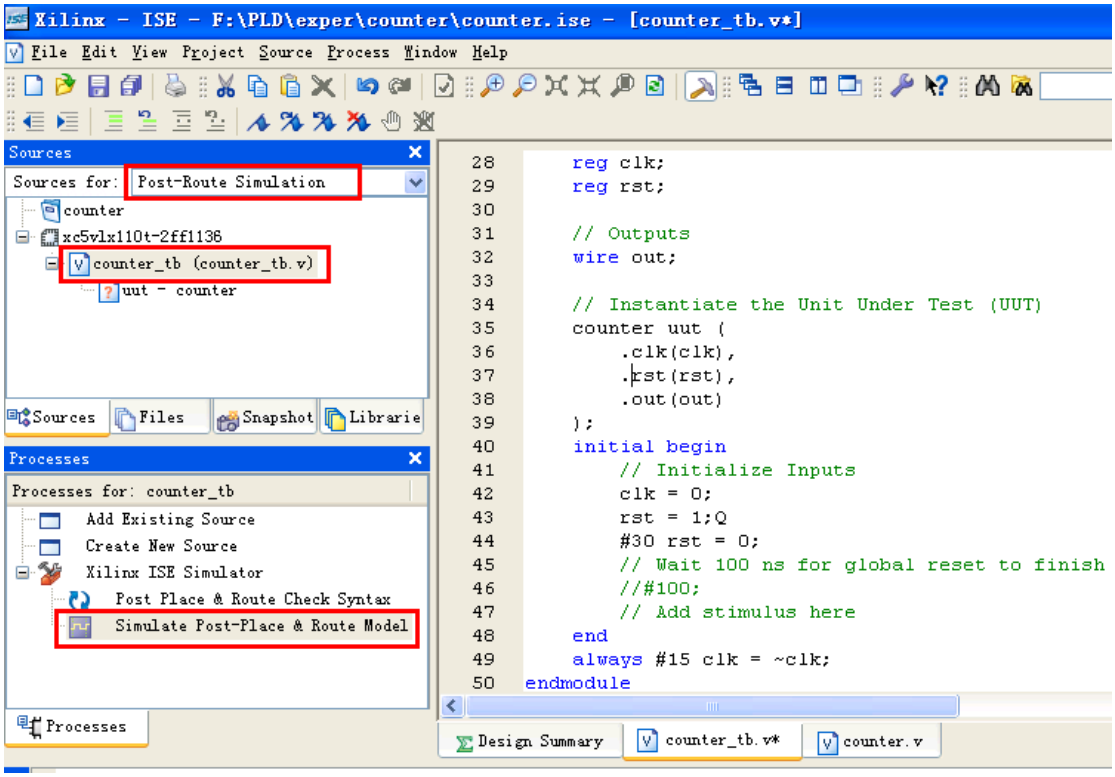
Double click Synthesize-XST to synthesize the circuit.

12. Double click Implement Design to place and route.

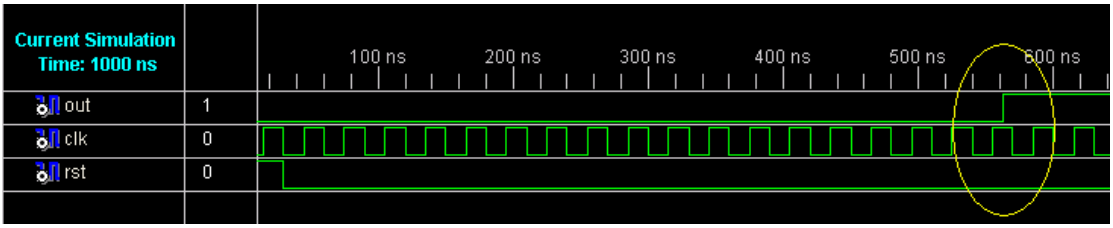
13. Timing simulation.

1）In the Sources window, select Sources for: **Post-Route Simulation。**

2）Click counter_tb，In the Processes window expand **Xilinx ISE Simulator**，double **Simulate Post-Place & Route Model** to perform timing simulation as follows:



The simulated waveform looks like the following：

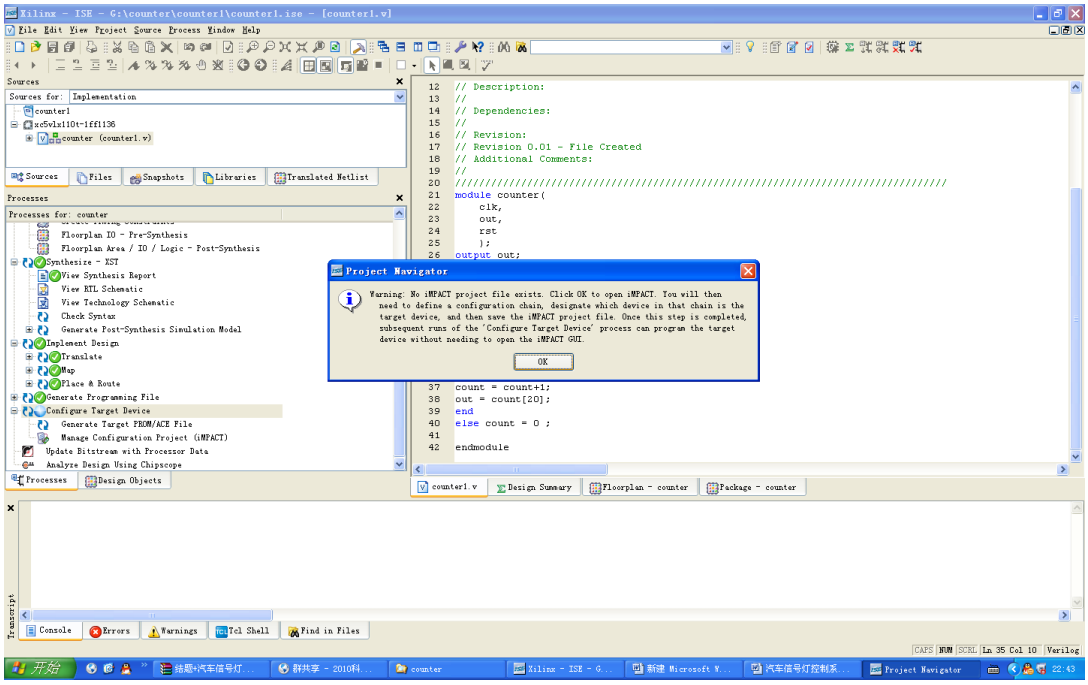


The time that the signal rises is later than that in the behavioral simulation, about 60ns’ delay.

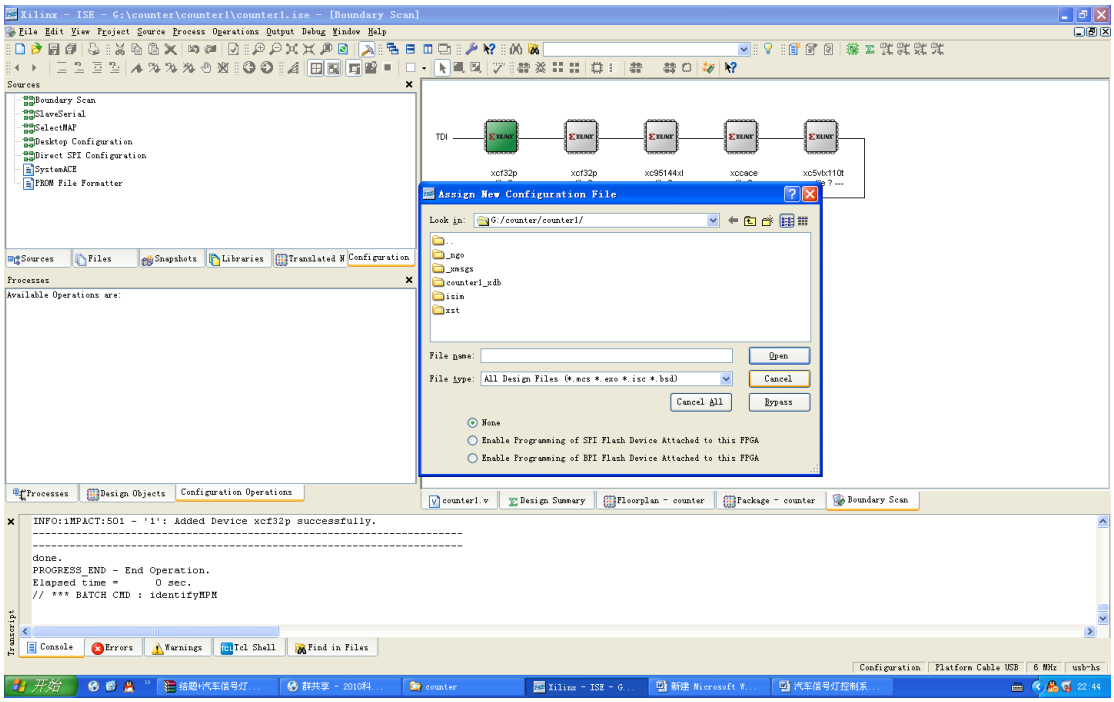
14. Change the line “out = count[4];” in the source file back to “out = count[20];”

Redo the implementation.

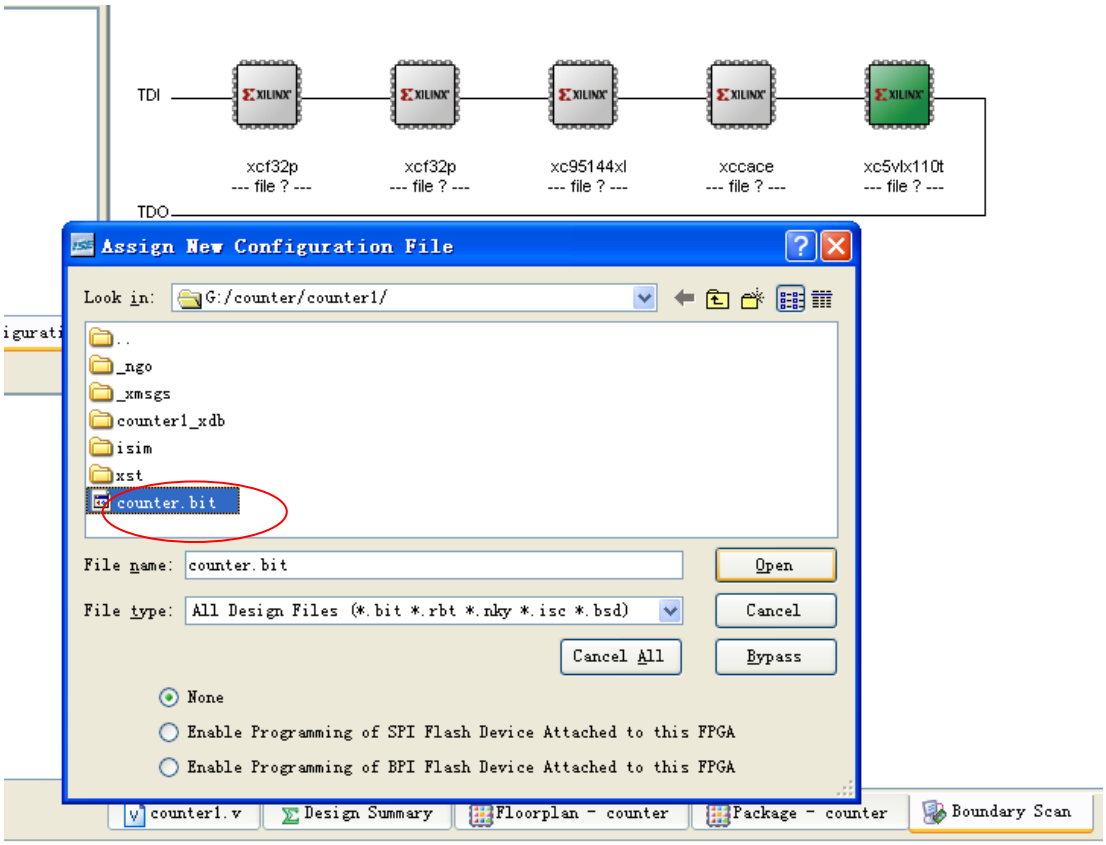
Double click Configure Target Device， generate “.bit” program file and download it to the board.



Click OK：

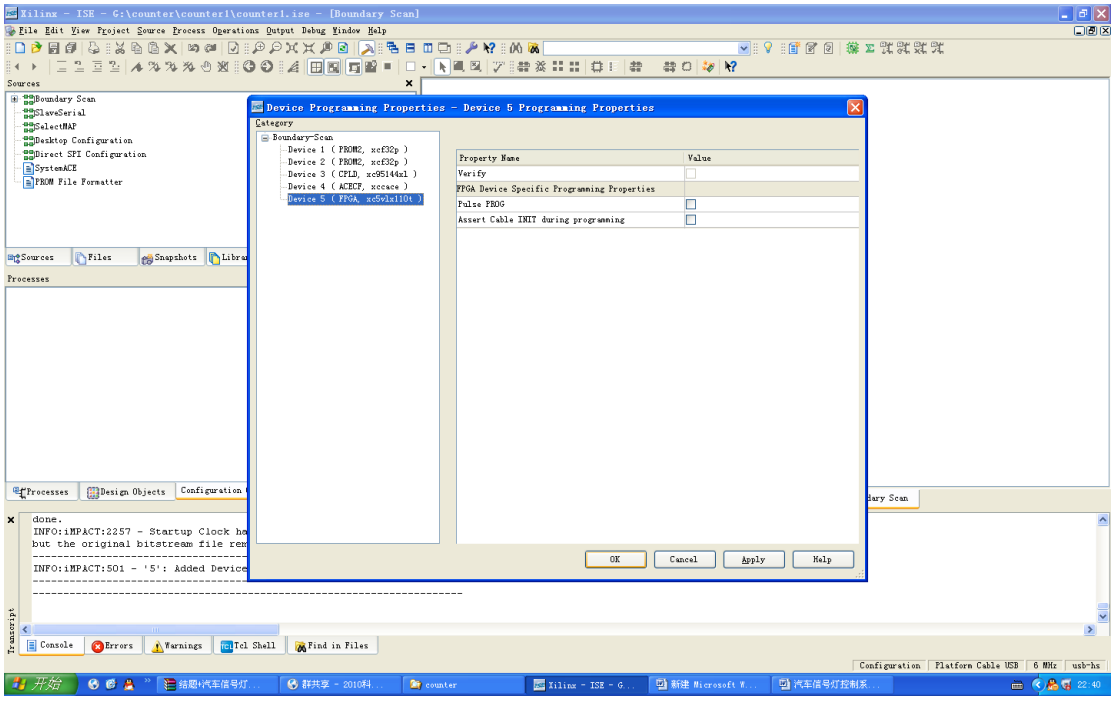


Click Cancel until you see the following：

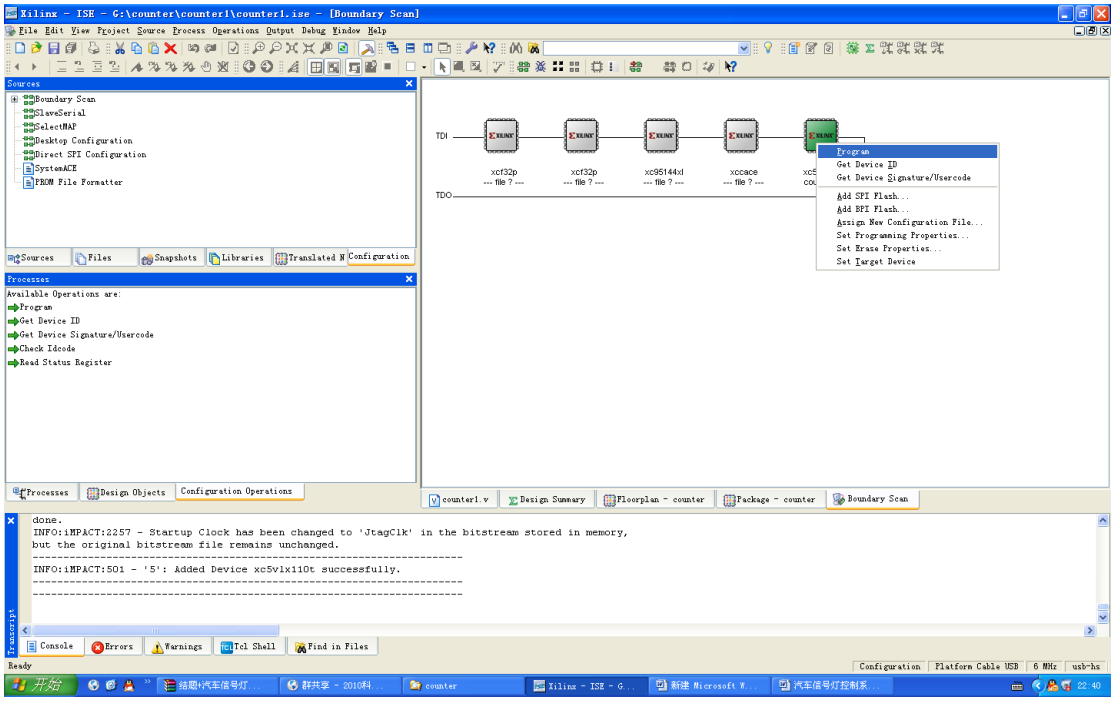


Select the counter.bit file to open.

Click OK：



Select Device 5, and click OK：



15. Right click on the last device (green), and select Program. The Programing Properties dialog box opens. Click OK to program the device, and you will see the message “Program succeeded”.

Watch the LED on the target board.

16. Assign the output pin to AD25， and redo the implementation and configuration, watch the output。

(Thanks Jia Ligang and Li Hong for document contribution.)