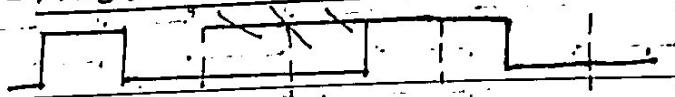


217.32



Bit time. Error occurred.

217.33

见书

254.1, 4, 5, 7

见书

255.8

On the book.

the difference is: a ~~will~~ will read J & K when CLK drop

b will read J & K when CLK up

255.10. 256.14

On the book.

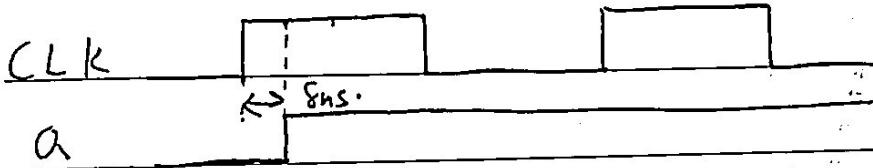
256.16

(Q: 0 0 0 0 | 1)

256.17

on the book.

257.22.



257.24

When a ↑ is produced, we give  $t=0$ .

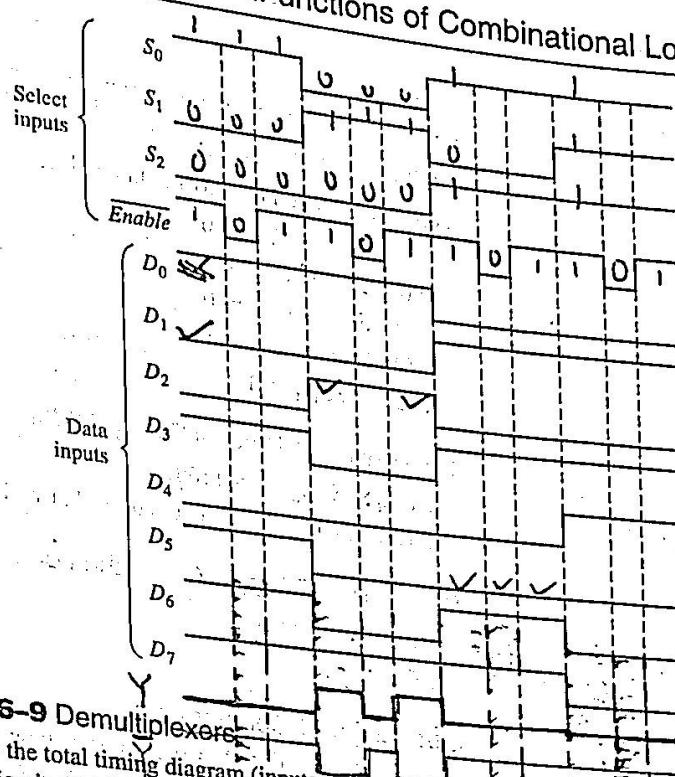
and ↑ convey to F-F,  $t=5\text{ ns}$

and in  $t=5+2=7\text{ ns}$ ,  $Q_A$  and  $\bar{Q}_A$  produced.

and in  $t=5+2 \times 2=9\text{ ns}$ ,  $Q_B$  and  $\bar{Q}_B$  produced.

so the min  $T=9\text{ ns}$ , max frequency is  $\frac{1}{T} = \frac{1}{9} \times 10^9 \text{ Hz}$

►FIGURE 6-69



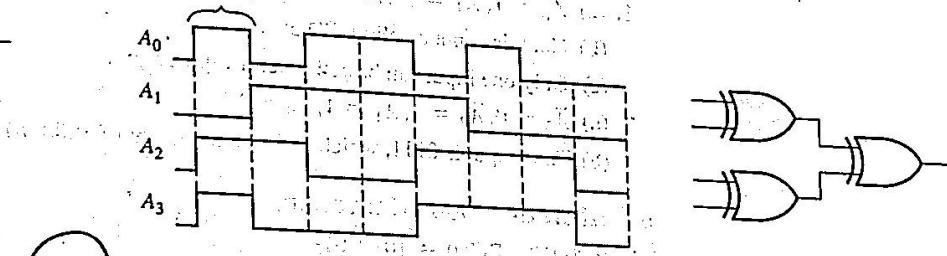
### Section 6-9 Demultiplexers

31. Develop the total timing diagram (inputs and outputs) for a 74HC154 used in a demultiplexing application in which the inputs are as follows: The data-select inputs are repetitively sequenced through a straight binary count beginning with 0000, and the data input is a serial data stream carrying BCD data representing the decimal number 2468. The least significant digit (8) is first in the sequence, with its LSB first, and it should appear in the first 4-bit positions of the output.

### Section 6-10 Parity Generators/Checkers

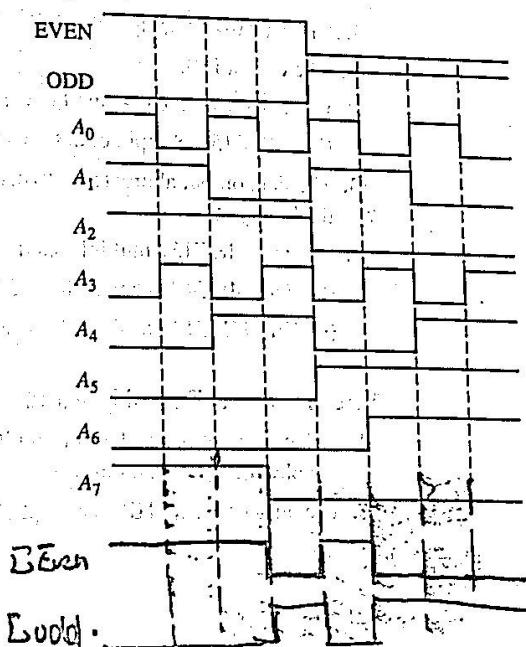
32. The waveforms in Figure 6-70 are applied to the 4-bit parity logic. Determine the output waveform in proper relation to the inputs. For how many bit times does even parity occur, and how is it indicated? The timing diagram includes eight bit times.

Bit time



33. Determine the  $\Sigma$  Even and the  $\Sigma$  Odd outputs of a 74HC280 9-bit parity generator/checker for the inputs in Figure 6-71. Refer to the function table in Figure 6-54.

►FIGURE 6-71



12. An astable multivibrator  
 (a) requires a periodic trigger input  
 (c) is an oscillator  
 (e) answers (a), (b), (c), and (d)
- (b) has no stable state  
 (d) produces a periodic pulse output  
 (f) answers (b), (c), and (d) only

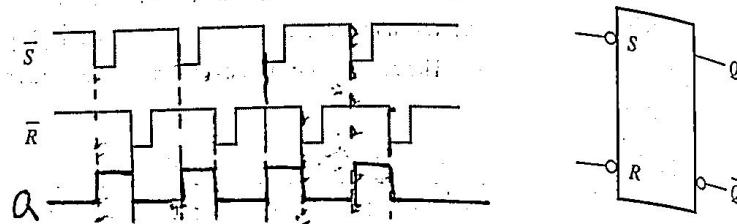
## PROBLEMS

Answers to odd-numbered problems are at the end of the book.

### Section 7-1 Latches

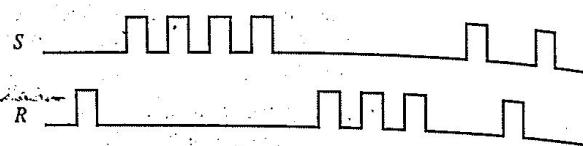
1. If the waveforms in Figure 7-61 are applied to an active-LOW input  $\bar{S}$ - $\bar{R}$  latch, draw the resulting  $Q$  output waveform in relation to the inputs. Assume that  $Q$  starts LOW.

► FIGURE 7-61



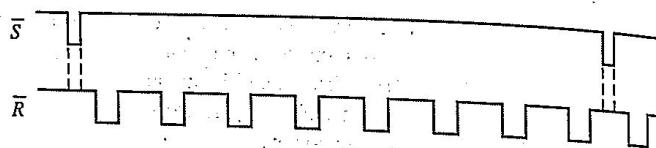
2. Solve Problem 1 for the input waveforms in Figure 7-62 applied to an active-HIGH S-R latch.

► FIGURE 7-62



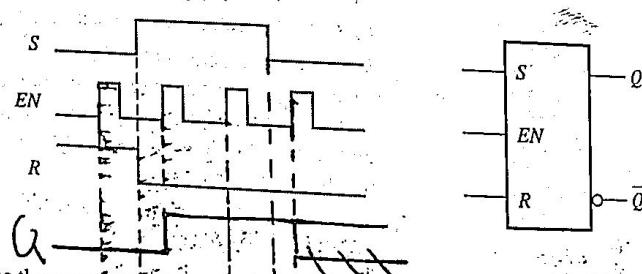
3. Solve Problem 1 for the input waveforms in Figure 7-63.

► FIGURE 7-63



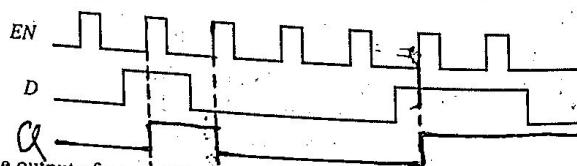
4. For a gated S-R latch, determine the  $Q$  and  $\bar{Q}$  outputs for the inputs in Figure 7-64. Show the results in proper relation to the enable input. Assume that  $Q$  starts LOW.

► FIGURE 7-64



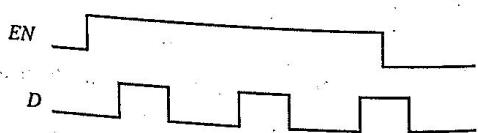
5. Determine the output of a gated D latch for the inputs in Figure 7-65.

► FIGURE 7-65



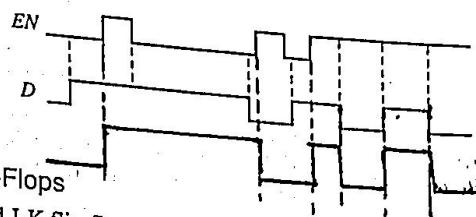
6. Determine the output of a gated D latch for the inputs in Figure 7-66.

► FIGURE 7-66



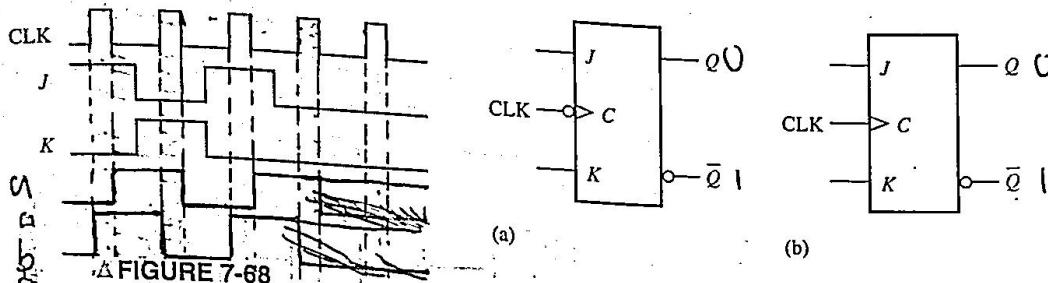
7. For a gated D latch, the waveforms shown in Figure 7-67 are observed on its inputs. Draw the timing diagram showing the output waveform you would expect to see at  $Q$  if the latch is initially RESET.

►FIGURE 7-67



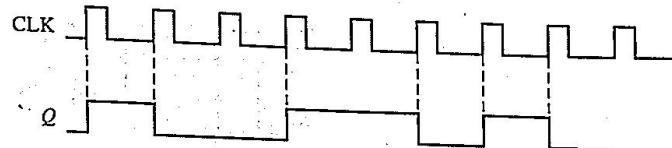
### Section 7-2 Flip-Flops

8. Two edge-triggered J-K flip-flops are shown in Figure 7-68. If the inputs are as shown, draw the  $Q$  output of each flip-flop relative to the clock, and explain the difference between the two. The flip-flops are initially RESET.



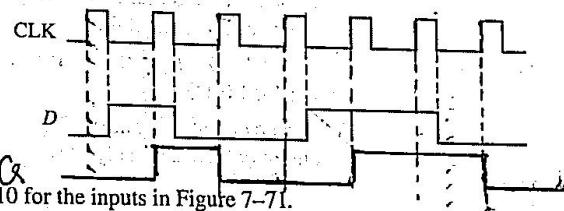
9. The  $Q$  output of an edge-triggered D flip-flop is shown in relation to the clock signal in Figure 7-69. Determine the input waveform on the D input that is required to produce this output if the flip-flop is a positive edge-triggered type.

►FIGURE 7-69



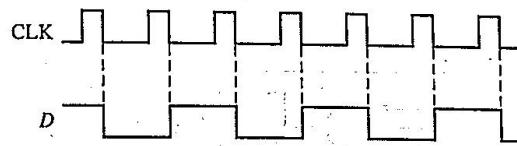
10. Draw the  $Q$  output relative to the clock for a D flip-flop with the inputs as shown in Figure 7-70. Assume positive edge-triggering and  $Q$  initially LOW.

►FIGURE 7-70



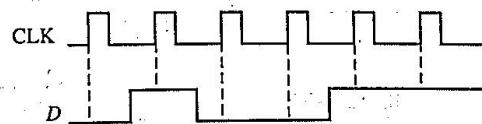
11. Solve Problem 10 for the inputs in Figure 7-71.

►FIGURE 7-71



12. For a positive edge-triggered D flip-flop with the input as shown in Figure 7-72, determine the  $Q$  output relative to the clock. Assume that  $Q$  starts LOW.

►FIGURE 7-72



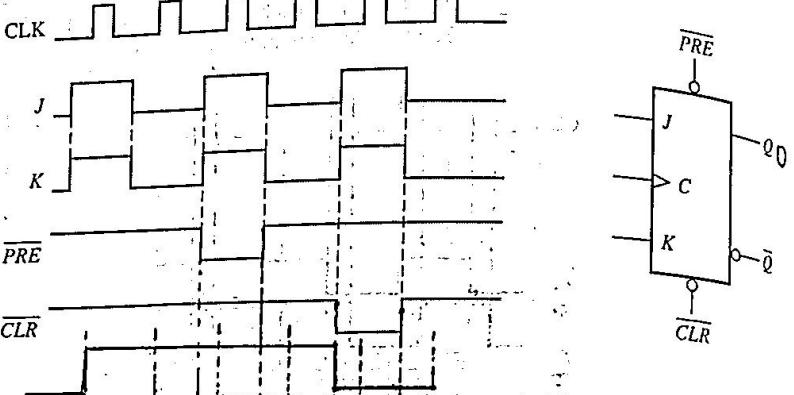
13. Solve Problem 12 for the input in Figure 7-73.

► FIGURE 7-73



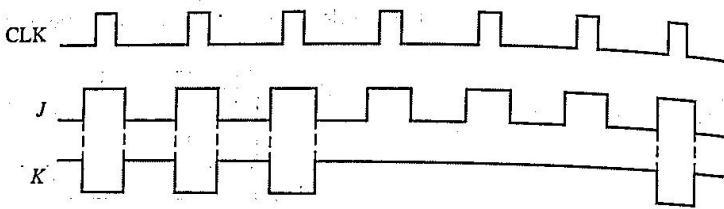
14. Determine the  $Q$  waveform relative to the clock if the signals shown in Figure 7-74 are applied to the inputs of the J-K flip-flop. Assume that  $Q$  is initially LOW.

► FIGURE 7-74



15. For a negative edge-triggered J-K flip-flop with the inputs in Figure 7-75, develop the  $Q$  output waveform relative to the clock. Assume that  $Q$  is initially LOW.

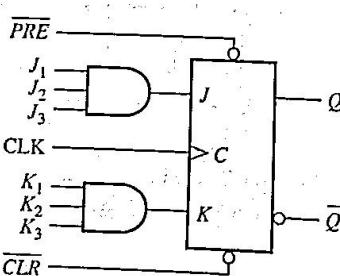
► FIGURE 7-75



16. The following serial data are applied to the flip-flop through the AND gates as indicated in Figure 7-76. Determine the resulting serial data that appear on the  $Q$  output. There is one clock pulse for each bit time. Assume that  $Q$  is initially 0 and that  $\overline{PRE}$  and  $\overline{CLR}$  are HIGH. Right-most bits are applied first.

$J_1: 1\ 0\ 1\ 0\ 0\ 1\ 1; J_2: 0\ 1\ 1\ 1\ 0\ 1\ 0; J_3: 1\ 1\ 1\ 1\ 0\ 0\ 0; K_1: 0\ 0\ 0\ 1\ 1\ 1\ 0; K_2: 1\ 1\ 0\ 1\ 1\ 0\ 0;$   
 $K_3: 1\ 0\ 1\ 0\ 1\ 0\ 1$

17. For the circuit in Figure 7-76, complete the timing diagram in Figure 7-77 by showing the  $Q$  output (which is initially LOW). Assume  $\overline{PRE}$  and  $\overline{CLR}$  remain HIGH.



► FIGURE 7-76

