Design Flow - Verification for AFTx07 Tape out

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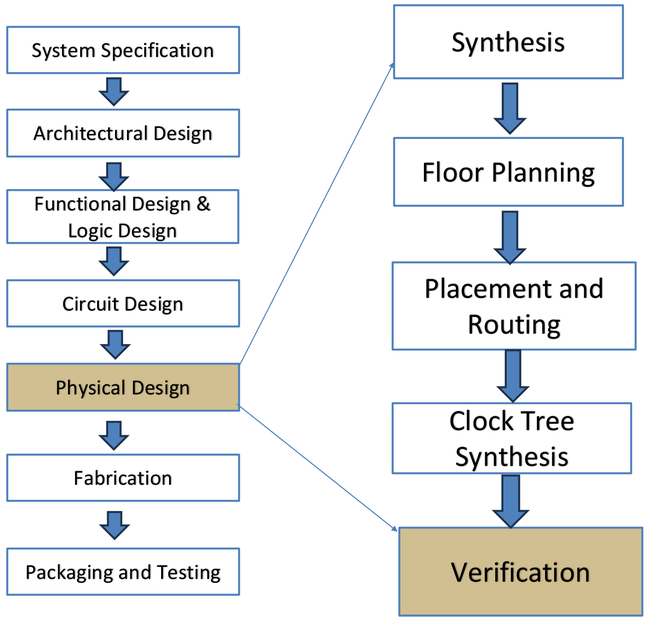
OVERVIEW

The verification team's responsibility is to run and debug key verification checks, including Design Rule Checking (DRC) and Layout Versus Schematic (LVS). Our team is using the MITLL research process design kit. We are using industry-standard tools such as Flowtool, Virtuoso, and Calibre, enabling us to detect and correct design rule violations systematically. Through our verification flow, we have successfully executed DRC and LVS checks which identify key issues such as density violations, spacing violations, and discrepancies between the synthesized and the circuit diagram netlist(s).

VLSI Design Flow



Tools Used

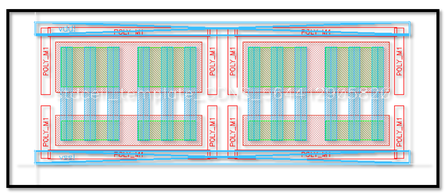
- Cadence Flowtool
- Cadence Virtuoso, Innovus and Genus
- Siemens Calibre

Verification Steps

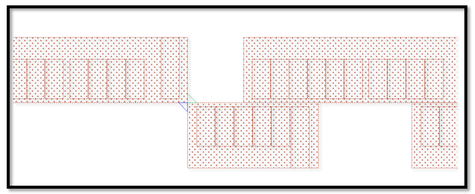
- DRC (Design Rule Check): Checks layout against foundry rules.
- LVS (Layout vs. Schematic): Confirms layout matches schematic/netlist.

Design Rule Check (DRC) Errors

- Spacing violations: Two layers too close together.
- Width violations: Wires or layers too narrow to manufacture reliably.
- Antenna violations: Long metal wires accumulate charge during fabrication, damaging transistors.
- Density violations: Deviation from required feature density limits

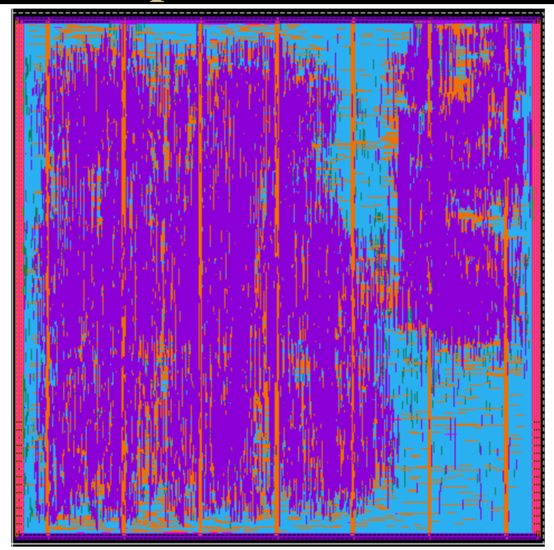


Fill Cell



Example of a spacing violation

Full Chip View of AFTx07



DRC Errors in AFTx07

Check / Cell	Results	Flat
Check R_12.01_POLY_WIDTH	888	3625846
Check R_15.05_NSD_SPC	1000	1000
Check R_16.05_PSD_SPC	1000	1000
Check D_1.01_MIN	1	1
Check D_12.01_MIN	1	1
Check D_29.01_MIN	5	5
Check D_32.01_MIN	1	1
Check D_34.01_MIN	1	1
Check D_36.01_MIN	1	1
Check D_38.01_MIN	1	1
Check D_44.01_MIN	1	1
Check D_46.01_MIN	1	1
Check auto_POLYGENF	1000	1000
Check auto_ACTGENF	1000	1000