Implementing DFT on a RISC-V SoC

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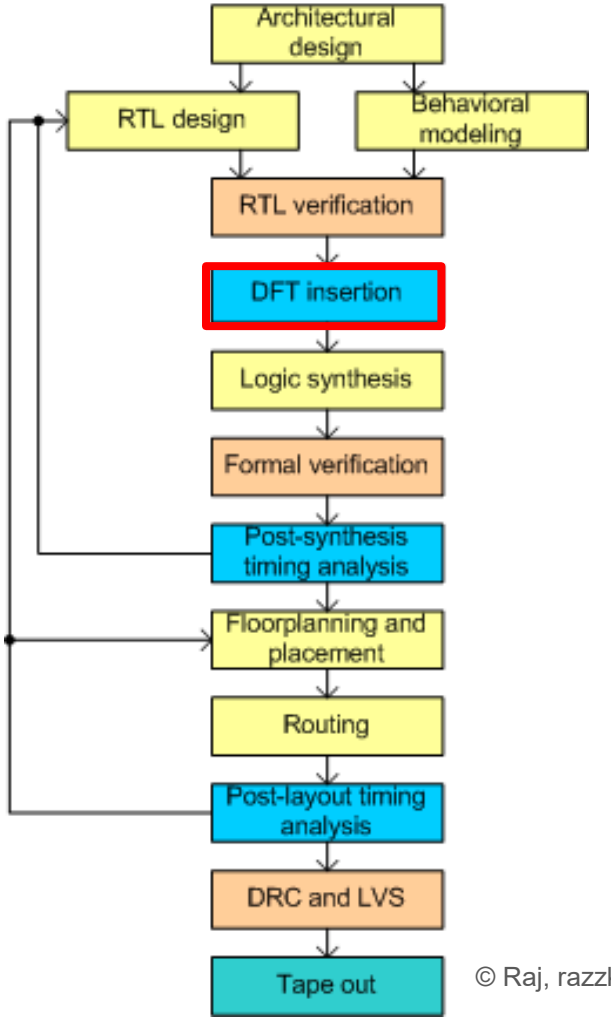
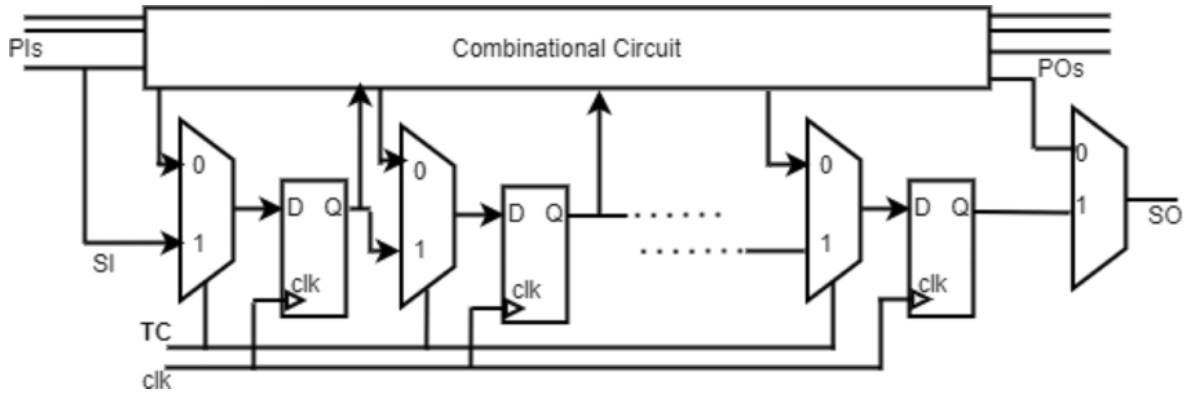
Design Flow: Why Test?

- Without testing, nothing ships
- New nodes → higher failures: find and fix issues with test
- Other testings: LEC, LDRC, STA etc.
- Other DFT method: LBIST



Scan

- Scan flip-flops: FFs with mux for test data
- Scan Chains
- Scan Compression
- Enhance observabitlity and controlability using the pattern generated by ATPG



Automatic Test Pattern Generation

1. Netlist Parsing
    a. Purpose: interpret circuit's netlist and prepare for further analysis and testing
    b. Create database, Design Rule Checking(DRC), Levelization…
2. Preprocessing
    a. Purpose: prepare the circuit for effective test pattern generation
    b. Fault collapsing, testability analysis, learning, redundant fault identification
3. Test Generation
    a. Purpose: create actual test patterns to detect the identified faults
    b. Random test pattern generation, deterministic test pattern generation
4. Test Compaction
    a. Purpose: reduce the volume of test data and the time required for testing without compromising fault coverage
    b. Dynamic test compaction, static test compaction

Methodology

On-Chip Clock Controllers (OCC)

- Scan shift-in slower than chip clock
- Save test time: run at fast clock, launch/ capture at slow clock

ATPG Compression

- 2% of ATPG bits are care bits
- OTHER POINTS

Power Saving

- Gate combinational blocks
- Ramp-up test clock frequency
- Clock skewing
- Manipulate ATPG don’t-care bits

Results

```
Running test coverage estimation...

 138824  faults were added to fault list.
************************************************************
 *  NOTICE:  The following DRC violations were previously  *
 *  encountered. The presence of these violations is an    *
 *  indicator that it is possible that the ATPG patterns   *
 *  created during this process may fail in simulation.    *
 *                                                         *
 *  Rules:  N20                                            *
 ************************************************************
 ATPG performed for stuck fault model using internal pattern source.
 ------------------------------------------------------------
 #patterns     #faults     #ATPG faults  test      process
 stored     detect/active  red/au/abort  coverage  CPU time
 ---------  -------------  ------------  --------  --------
 Begin deterministic ATPG: #uncollapsed_faults=125091, abort_limit=10...
 0          121932   3159         0/0/6    97.29%      0.09
 0            1837   1320         2/0/6    98.65%      0.09
 0             659    657         4/2/6    99.15%      0.10
 0             223    426         6/8/6    99.31%      0.10
 0             150    263       11/13/6    99.43%      0.10
 0              84    143       17/27/6    99.50%      0.11
 0              76     38       27/46/6    99.56%      0.12
 0              28      4       29/49/8    99.58%      0.12
```

```
            Pattern Summary Report
-----------------------------------------------
#internal patterns                            0
-----------------------------------------------
Uncollapsed Stuck Fault Summary Report
-----------------------------------------------

fault class                     code   #faults

------------------------------  ----  ---------

Detected                         DT     133745
Possibly detected                PT         20
Undetectable                     UD       4509
ATPG untestable                  AU        546
Not detected                     ND          4
-----------------------------------------------

total faults                             138824
test coverage                            99.58%
-----------------------------------------------
```

Future Plan

Implement DFT on AFTx07

- Protocol for Synopsys Fusion Compiler
- Perform Scan Insertion, ATPG
  - scan design security and improving testability
- Attempt Compression, Power Saving
  - optimizing gate combinational block
  - test clock frequencies
  - clock skewing

References

- Trustworthy Scan Design and Testability Using Obfuscation and Logic Locking Scheme for Wireless Network Application - Scientific Figure on ResearchGate. Available from: https://www.researchgate.net/figure/Traditional-scan-based-DfT-4_fig1_358673811 [accessed 13 Nov 2024]

Acknowledgements

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