Design Flow - Verification

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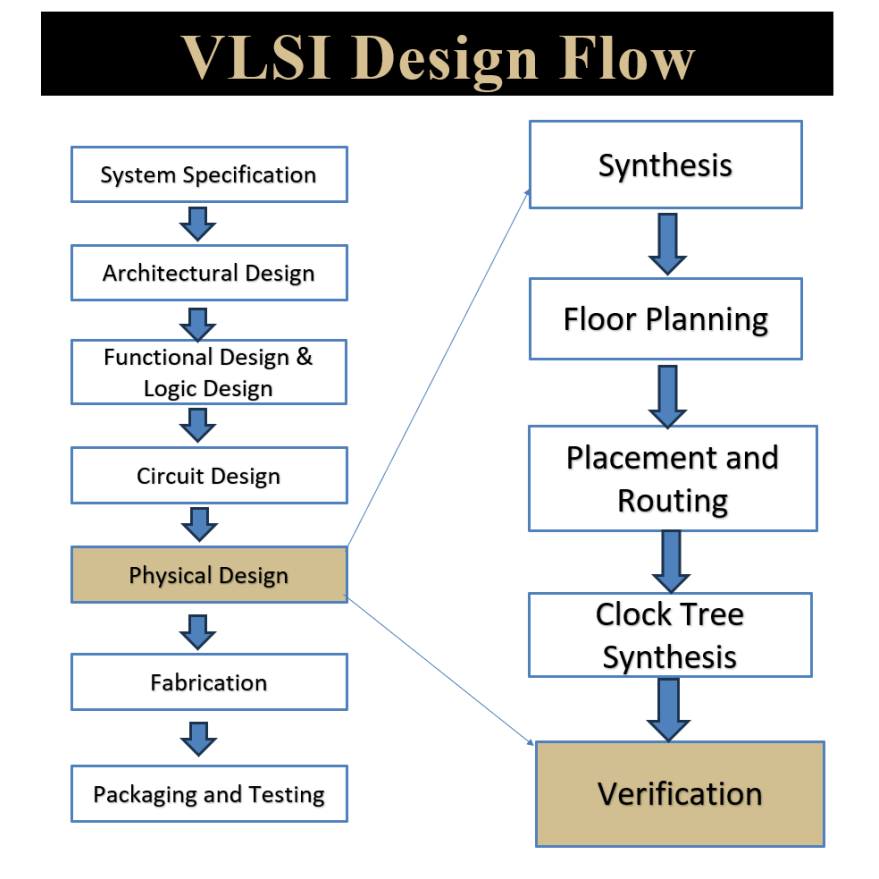
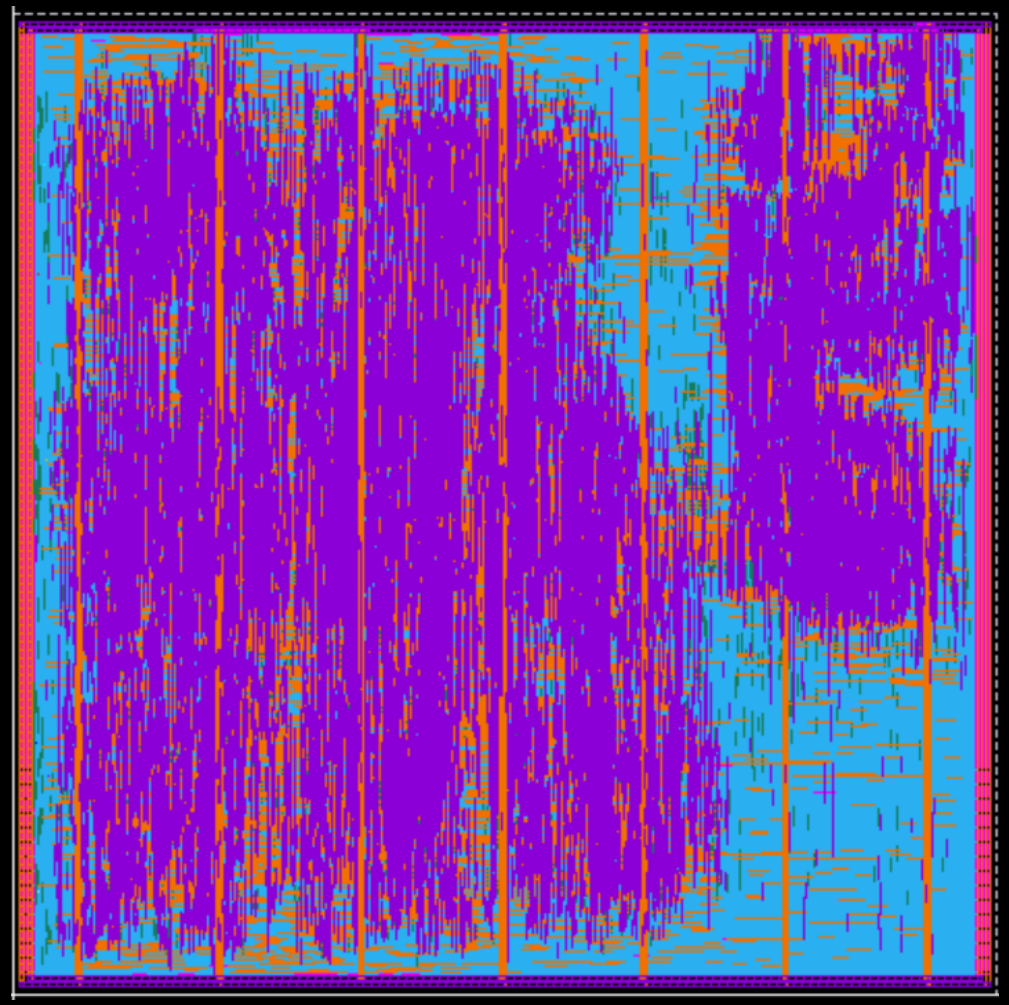
Introduction



Verification Steps:

- DRC (Design Rule Check): Checks layout against foundry rules.
- LVS (Layout vs. Schematic): Confirms layout matches schematic/netlist.

Chip Layout



Design Rule Check

- How do to run DRC?
- Initial Errors from the DRC run
- Changes made to the flow

How to run DRC using Calibre

Run the flow using flowtool

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GDSII file (layout file)

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Virtuoso

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Calibre – run nmDRC

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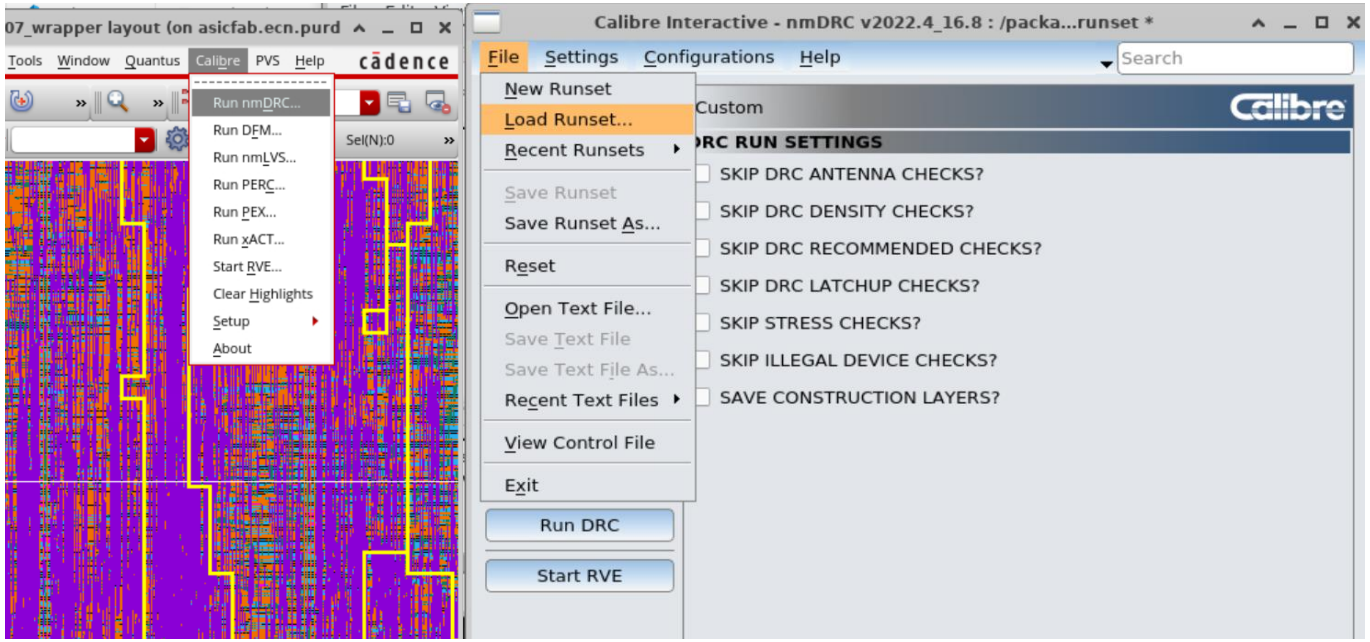
Load DRC runset from pdk in Calibre

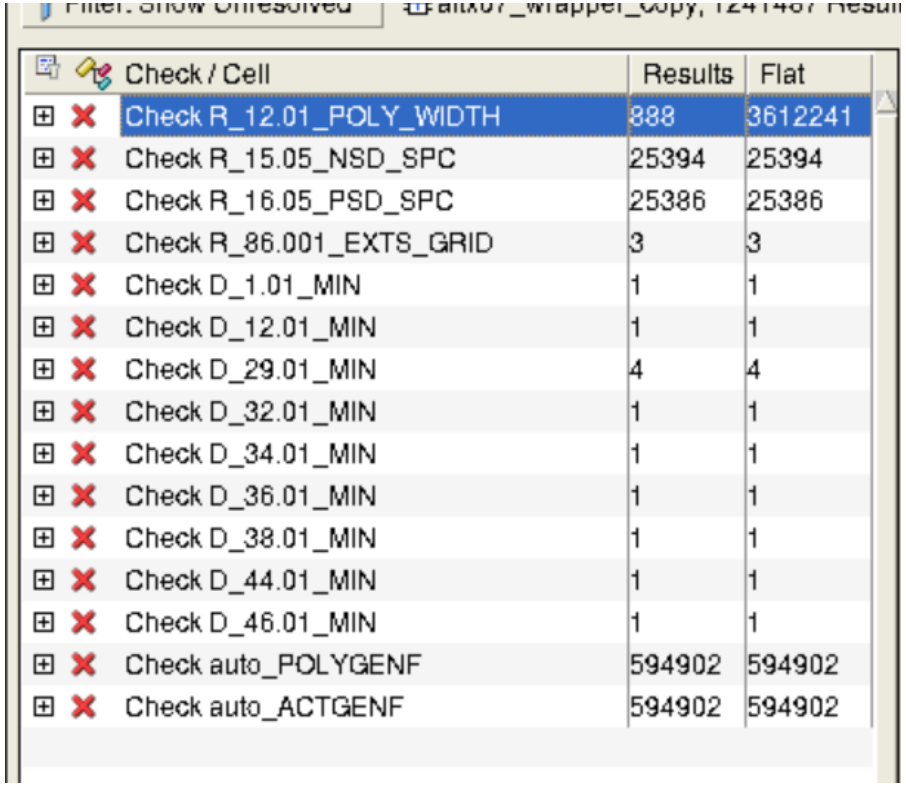
↓

Run DRC



Initial Errors from the DRC run

- Poly layer had incorrect width.
- NSD and PSD layers had spacing violations.
- EXTS GRID coordinates not aligned to the nearest micrometer.
- Remaining errors were density-related

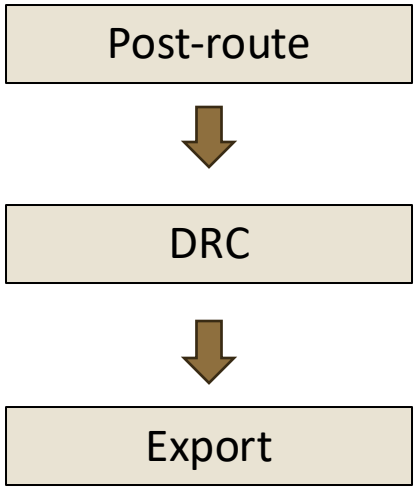


Check / Cell	Results	Flat
Check R_12.01_POLY_WIDTH	888	3612241
Check R_15.05_NSD_SPC	25394	25394
Check R_16.05_PSD_SPC	25386	25386
Check R_86.001_EXTS_GRID	3	3
Check D_1.01_MIN	1	1
Check D_12.01_MIN	1	1
Check D_29.01_MIN	4	4
Check D_32.01_MIN	1	1
Check D_34.01_MIN	1	1
Check D_36.01_MIN	1	1
Check D_38.01_MIN	1	1
Check D_44.01_MIN	1	1
Check D_46.01_MIN	1	1
Check auto_POLYGENF	594902	594902
Check auto_ACTGENF	594902	594902

Changes Made

Flow.yaml

- Added a DRC step in the *implementation* block before the export step



Innovus_steps.tcl

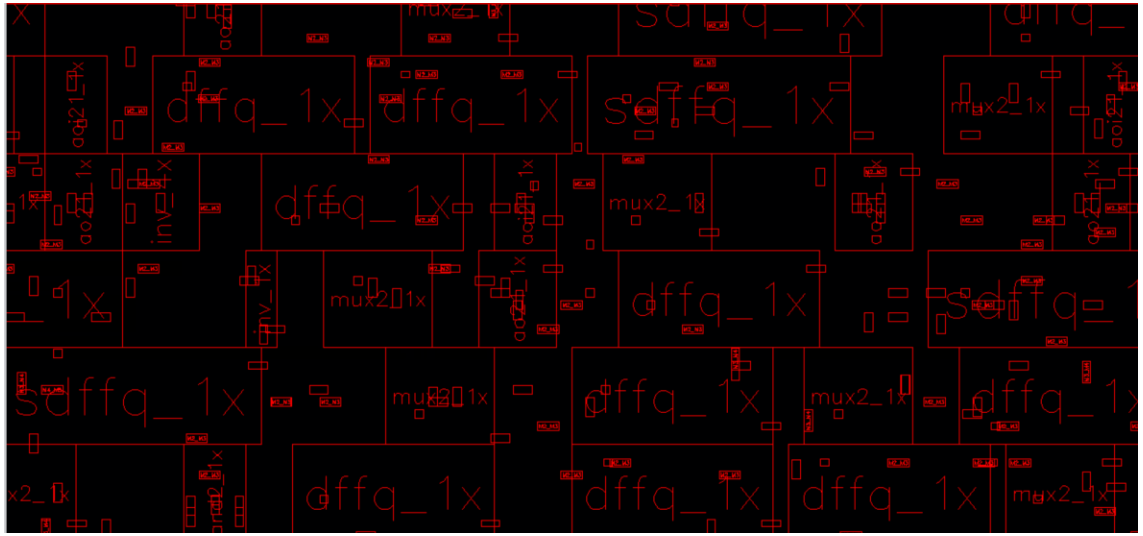
- Added *run_drc* flow step to address spacing violations.
- Commands used:
  - check_drc at start and end
  - add_fillers

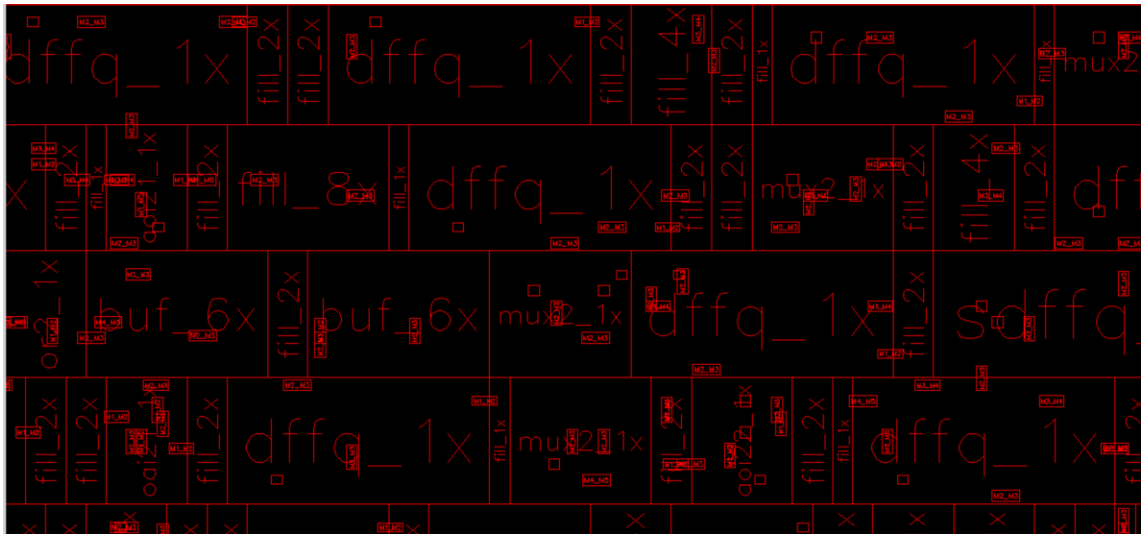
```
################################################################
# STEP run_drc
################################################################
create_flow_step -name run_drc -owner cadence {
  check_drc -out_file [file join [get_db flow_report_directory] [get_db flow_report_name] drc_violations_initial.rpt]

  add_fillers -base_cells {fill_16x fill_8x fill_4x fill_2x fill_1x}

  check_drc -out_file [file join [get_db flow_report_directory] [get_db flow_report_name] drc_violations_final.rpt]
}
```

Results - DRC

- Layout before and after fill
- Final results from the DRC run

Layout before and after fill cells



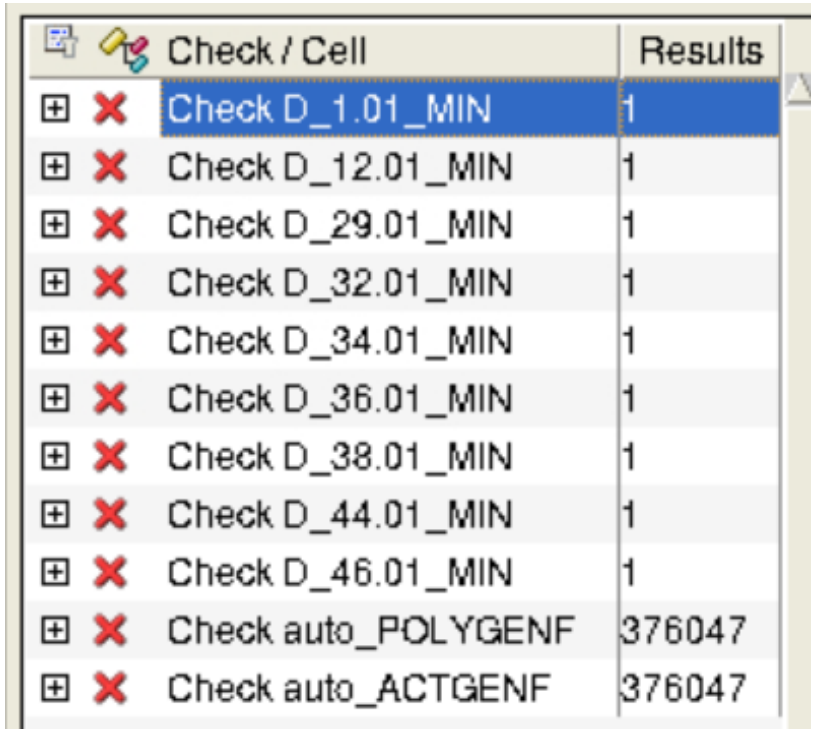


Final results from the DRC run

•Adding fill cells resolved poly width error and spacing violations.

•Manually fixed EXTS_GRID violations by rounding coordinates to the nearest micrometer.

•No timing issues after addition of fill cells



Check / Cell	Results
Check D_1.01_MIN	1
Check D_12.01_MIN	1
Check D_29.01_MIN	1
Check D_32.01_MIN	1
Check D_34.01_MIN	1
Check D_36.01_MIN	1
Check D_38.01_MIN	1
Check D_44.01_MIN	1
Check D_46.01_MIN	1
Check auto_POLYGENF	376047
Check auto_ACTGENF	376047

Layout vs. Schematic

- *How to run LVS?*
- *Issues found in flex counter/work-flow*

HOW TO RUN LVS

Run the flow using flowtool

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GDSII file (layout file)

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Verilog file (schematic file)

↓

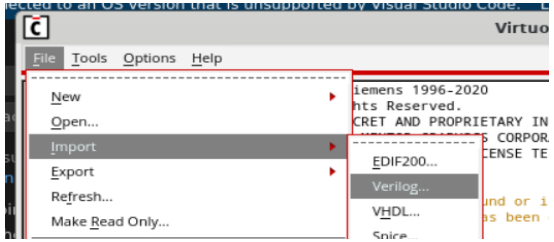
Calibre-runnmLvs

↓

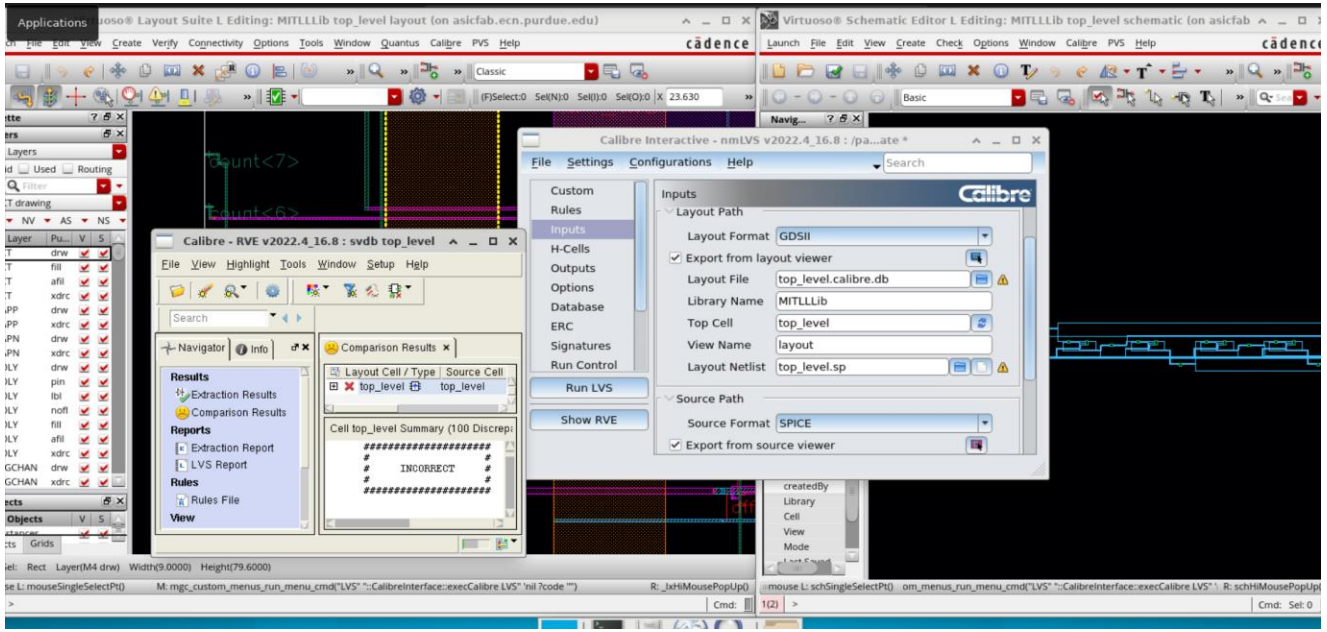
Load LVS runset and rules

↓

Run LVS

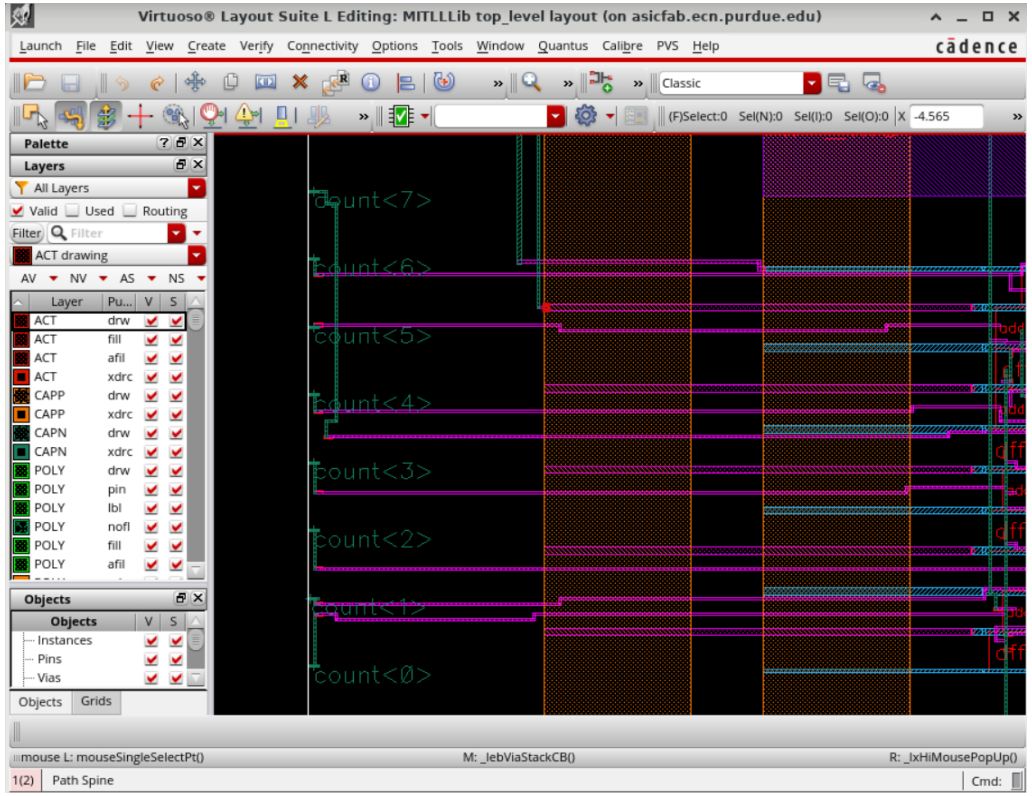


**check final report project doc for detailed steps on importing schematic



Initial Errors (Attempting) To Run LVS

1) Issues with exporting netlists:
   - it couldn't recognize the vss! And vdd! Nets in our net list + instances of 'unknown' cells
2) Flex counter: labels missing for the I/O's pads; needed to manually added
3) A plethora of isses once we were able to run LVS, indicating a higher level issue



Issue #1, #2

1) Straightforward (thanks Tim!) fix: specify unknown cells when writing the net list so LVS doesn't mistakenly flag it

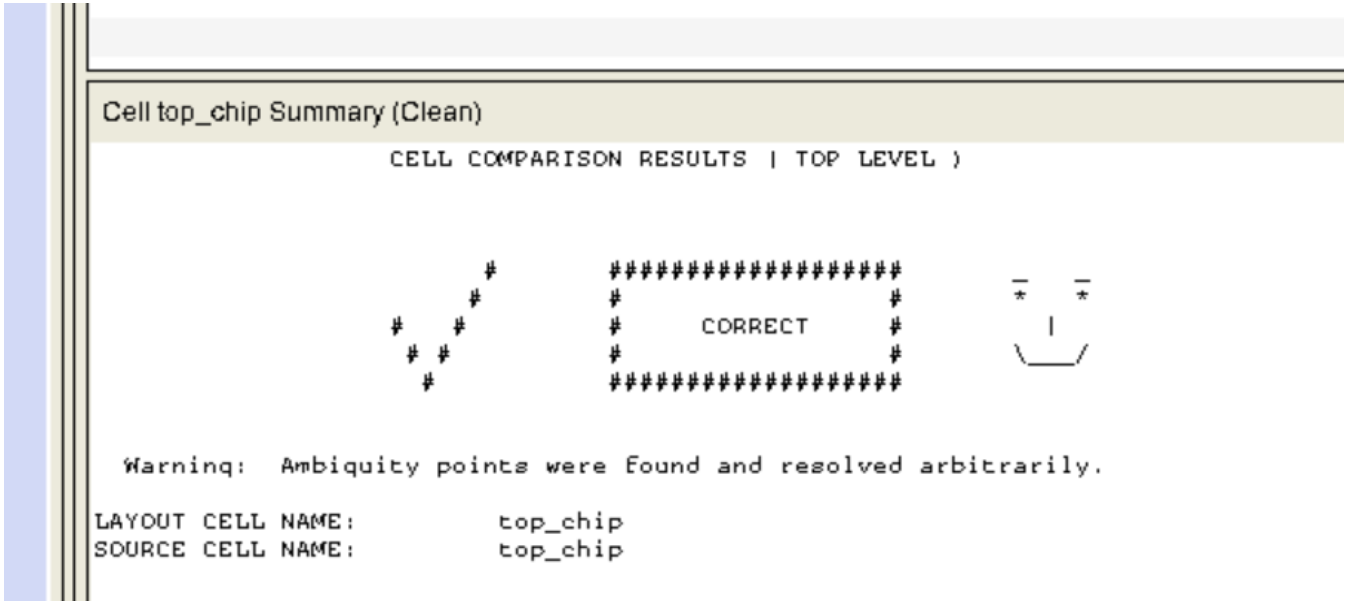
2) Add labels for I/O pads such as VSS, VSSIO, etc. And re-run LVS to see fixes

```
set unknown_cells {
  fill_1x fill_2x fill_4x fill_16x \
  spacer_1 spacer_5 spacer_10 spacer_30 spacer_60 \
  corner \
}


write_netlist out/top_chip.lvs.v -exclude_insts_of_cells $unknown_cells -exclude_leaf_cell
write_netlist out/top_chip.lvs.v -exclude_insts_of_cells $unknown_cells
}
```

Issue #3

- A large amount of issues were due to the IO pads not being connected to the ring, leading to the power and ground nets beind shorted, which propagated to LVS issues globally. Once fixed, LVS passed (thanks Tei!)



After

Next Steps

- *Run DRC with IO pads in layout*
- *Automate LVS workflow*

THANK YOU

Questions?