

## Application

### Front end

User  
Interface

TensorFlow  
Model  
Ingestion

### Middle End

Model  
Analysis

Hardware  
Design  
Parameters

Abstract  
Hardware Macro  
Object Library

System Architecture  
Generation

### Back end

Verilog  
Skeleton &  
Templates

RTL  
Generation

## Legend

Abstract model

Full Design Needed

HW-mapped model

Partial Design Needed

Control

No Design Needed

## FPGA

Auxiliary IP

Generated  
Core Engine

Ext. Interfaces

FPGA CAD  
Tool