# Op-amp Design (expt.5)

- **Design** and simulate in Multisim, an operational amplifier circuit.
- The four ‘building blocks’ are:
  - differential input stage (long-tailed pair)
  - common emitter amplifier
  - emitter follower
  - current mirror circuit
- Briefly investigate each of these circuits in turn before combining them to produce the operational amplifier circuit to a given specification.

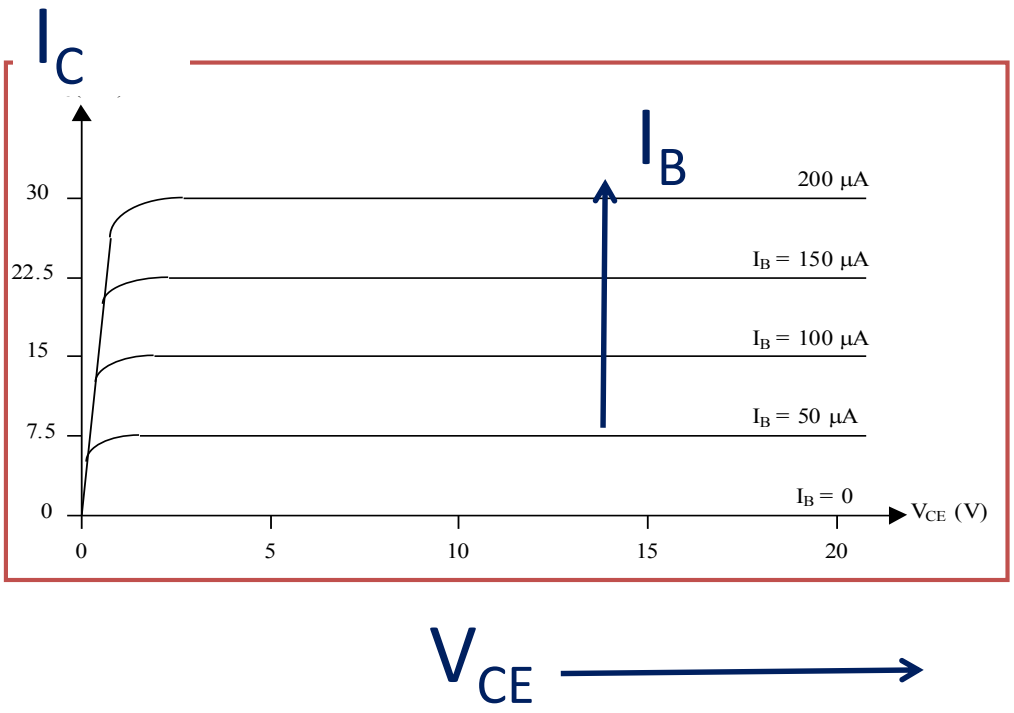
These slides are on CANVAS under ‘Experiment 5’

# Specification

- Differential input impedance, $R_{id} > 100\ k\Omega$
- Voltage gain ($A_{ol}$) greater than 500,000
- Output impedance, $R_o < 1\ k\Omega$
- Output voltage to be ‘zero’ volts for zero input
- Frequency response down to D.C.
- Supply voltage +9 to -9 V
- total current consumption not greater than 5 mA

# DC characteristics

## [see 'Part 2' slides on CANVAS]




Common-emitter, **DC** current gain

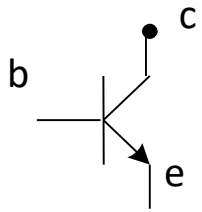
$$h_{FE} = \frac{I_C}{I_B}$$

Common-emitter, **AC** current gain

$$h_{fe} = \frac{\Delta I_C}{\Delta I_B} = \frac{i_c}{i_b}$$

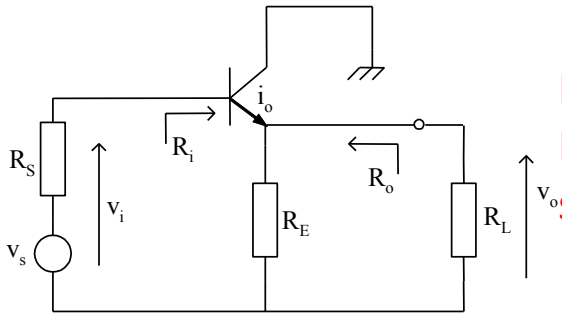
Q: How could we estimate AC gain from DC characteristics?

Note: different notation $h_{FE} \equiv \beta$ $h_{fe} \equiv \beta_o$

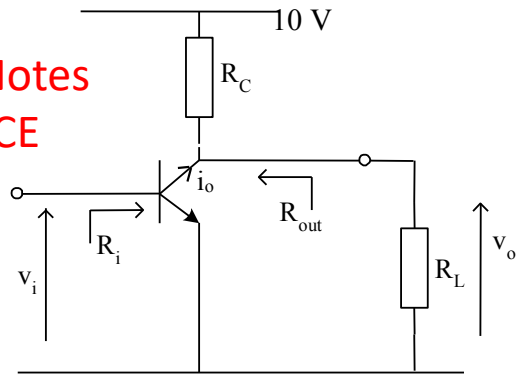


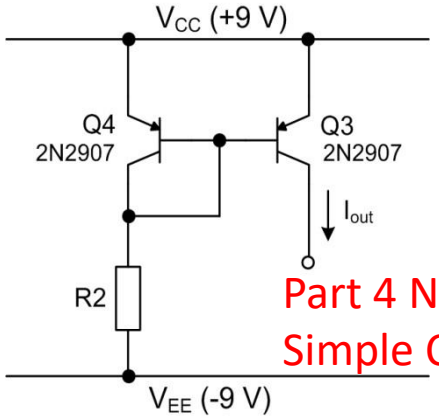
# Pre-lab

- Learn how to design the ‘building blocks’

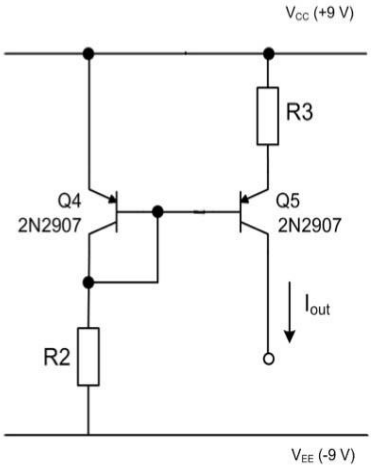



Part 2 Notes
EF and CE stages

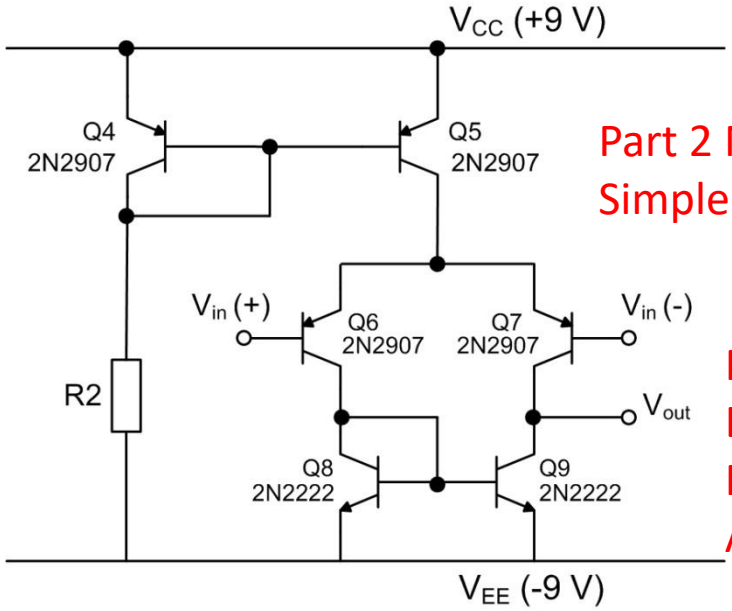



Part 4 Notes
Simple CM



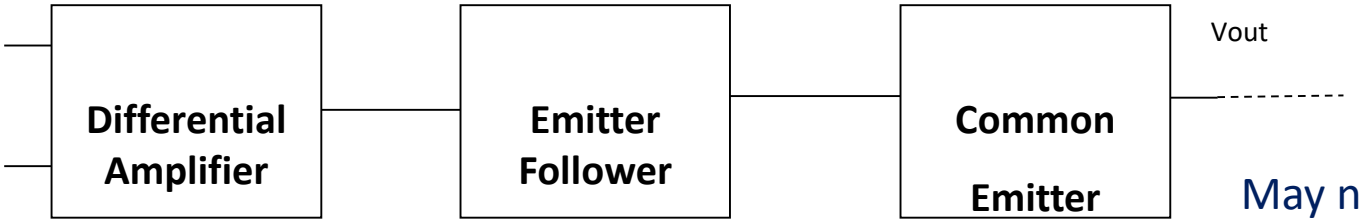

Part 4 Notes
Widlar CM



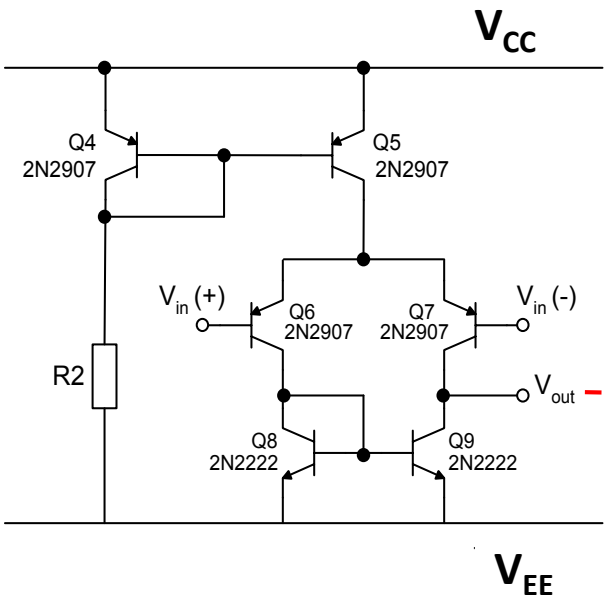

Part 2 Notes
Simple CM

Part 3 notes
Differential Amp
Part 5 Notes
Active loads

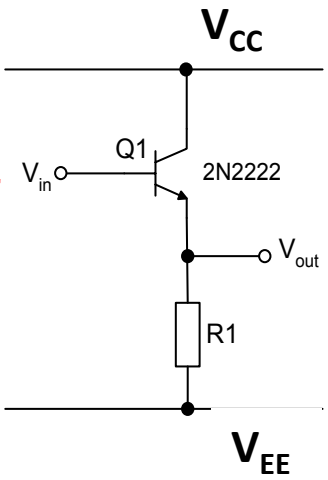
# Putting it together...

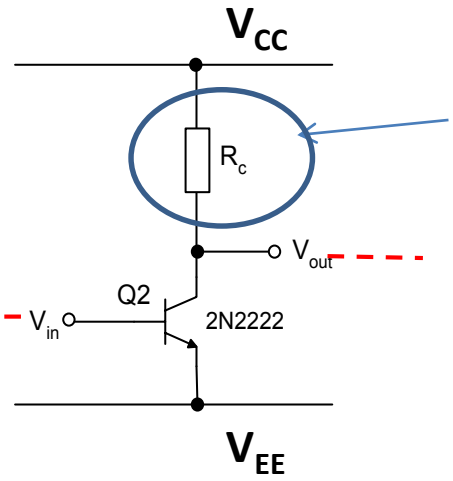



May need another block to meet the spec on $R_{OUT}$....




A CC stage to match the input and CE voltage gain stages

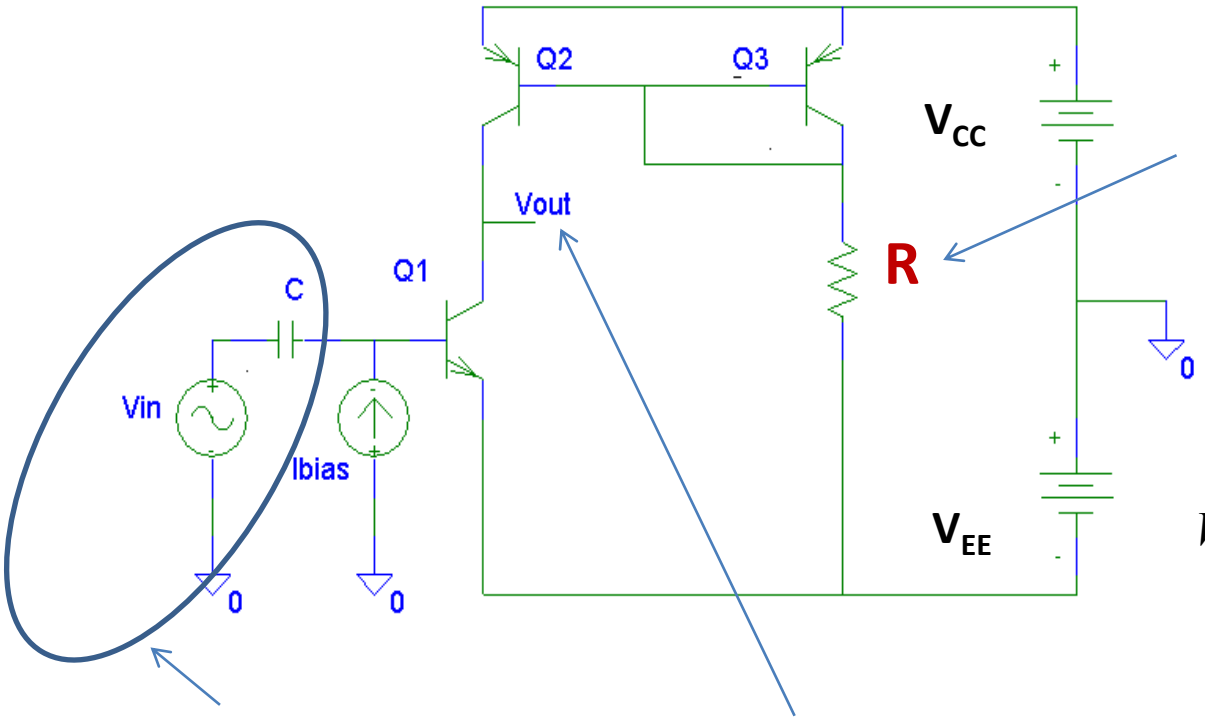



Use an active load here, not a resistor or you won't get enough gain

- Always check the dc levels (voltages, currents) first
- Remember loading effects of one stage on another

# CE amp with CM load




$V_{CC}$ = 9 V, $V_{EE}$ = -9 V

What is the V-drop across the resistor?

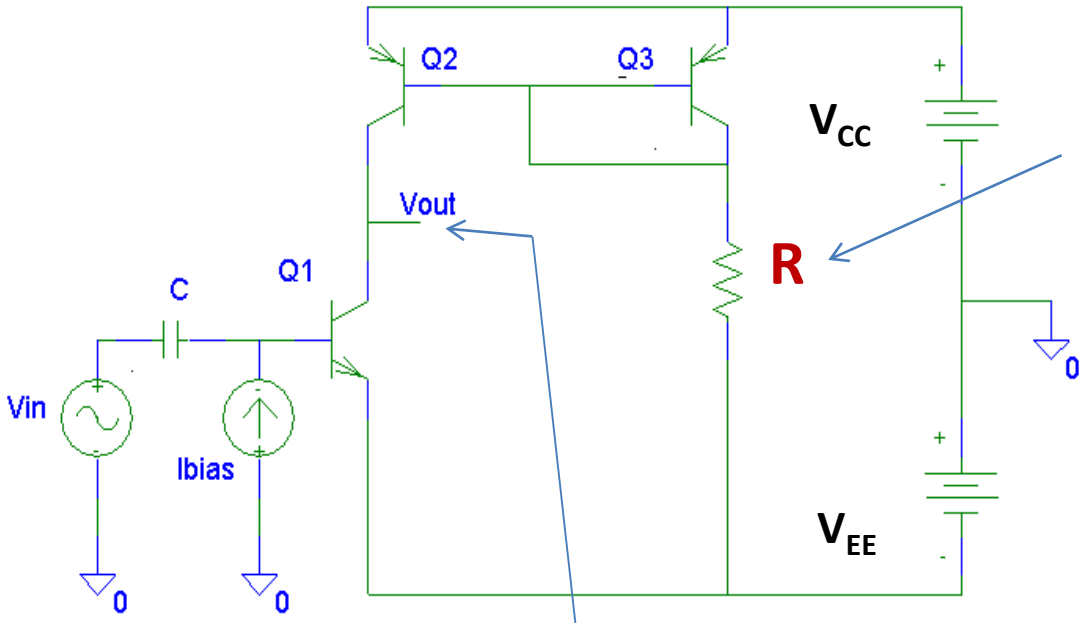
What value will give 1 mA (say)?

$$V_R = \frac{9-(-9)-0.6}{I_C}$$

Can use this to check the gain once you have it biased correctly

Set $I_C$ to your desired value
Choose $I_{bias}$ to set $V_{out} \approx 0$ V (use a dc sweep of $I_{bias}$ as before)

# Output resistance of a CE amp with CM load




$V_{CC}$ = 9 V, $V_{EE}$ = -9 V

What is the V-drop across the resistor?

What value will give 1 mA?

$$r_{ce} = \frac{V_A}{I_C}$$

$$R_{OUT} = r_{ce1} // r_{ce2}$$

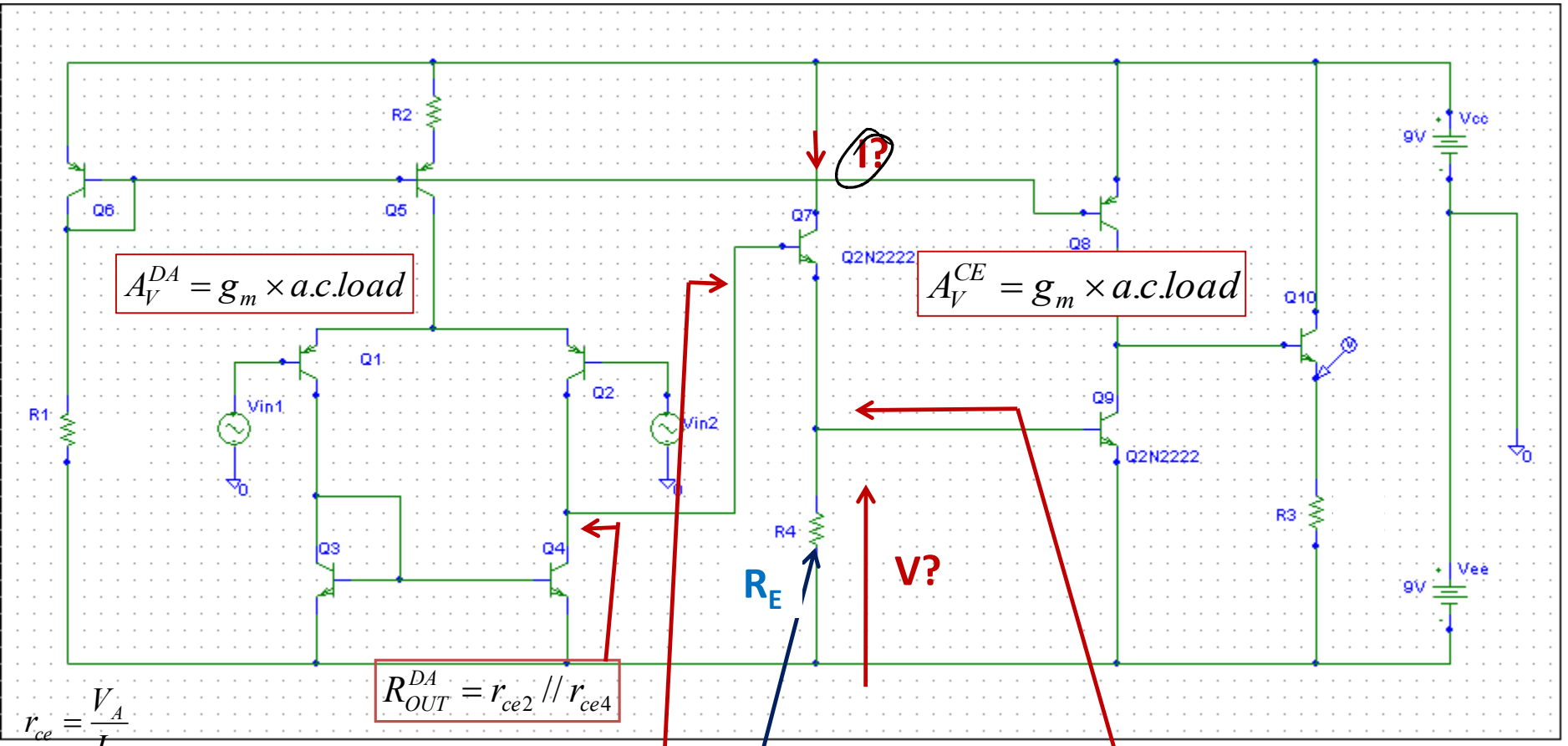
If the CE is connected to a load (another stage), it's ac load is

$$r_{ce1} // r_{ce2} // R_{in}(next\ stage)$$

You can find the Early voltage from the model listing for the transistor

Same analysis applies for the Diff Amp output

# Matching the Diff Amp to the CE




$$r_{ce} = \frac{V_A}{I_C}$$

$$R_{in}^{CC} = r_{be}(Q_7) + (\beta_o + 1)R_E // r_{be}(Q_9)$$

$$R_{OUT}^{CC} \approx \left[\frac{r_{be}(Q_7) + R_o(Diff.Amp)}{\beta_o + 1}\right] // R_E$$

$$r_{be} = \frac{\beta_o}{g_m} = \frac{\beta_o}{40I}$$

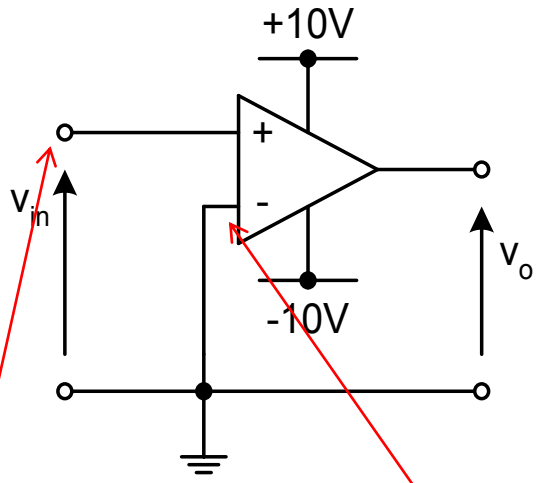
$R_E$ effectively acts as a current source (with $V_{EE}$)

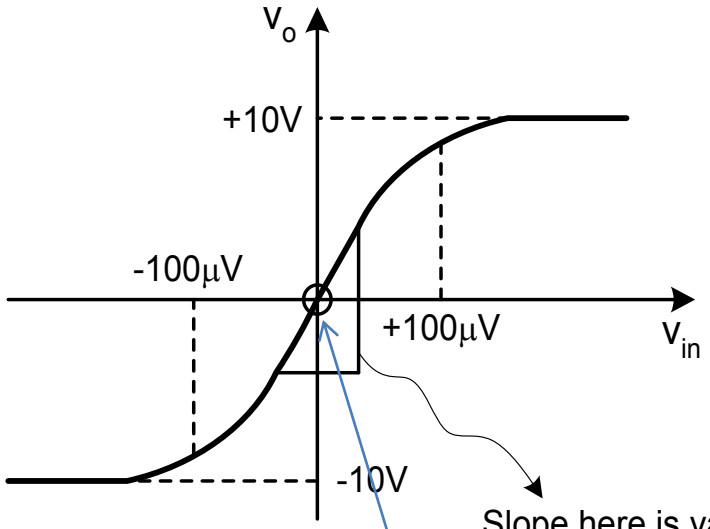
Ac load for Diff. amp. is $r_{ce2} // r_{ce4} // R_{in}(CC)$

# The VTC is a handy way to estimate gain

## (and investigate offsets)

First, look at the **Voltage Transfer Curve** (VTC) of an amplifier.




Slope here is value of $A_{ol}$ quoted by manufacturer

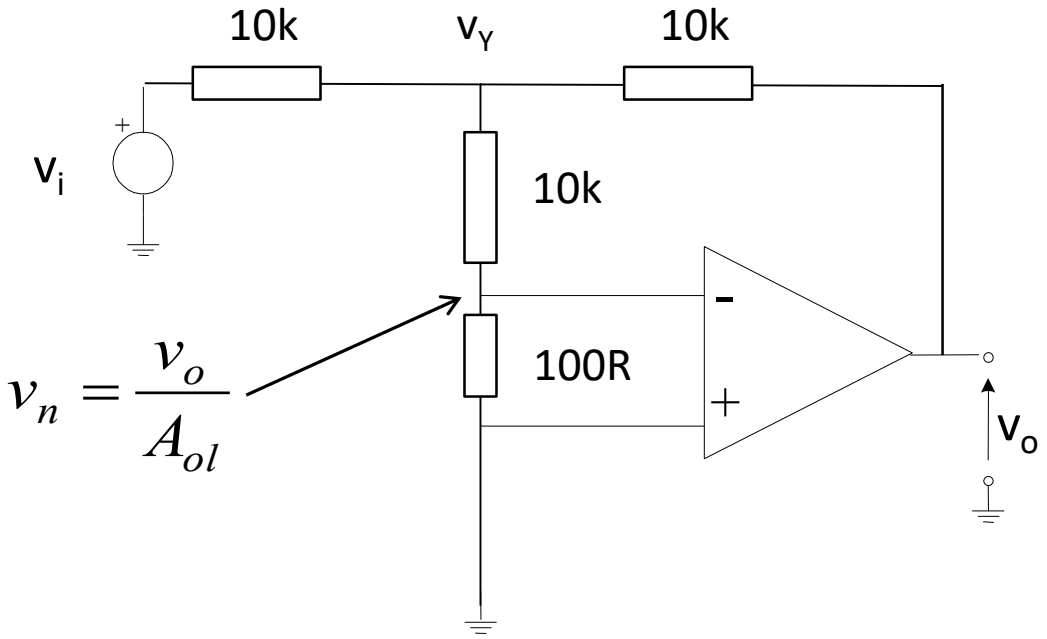
Sweep the voltage on the positive input

Attach the negative input to ground)

Usually see a small voltage offset here: Measure it and then build into the input voltage source to set the output close to 0 V.

# Or: alternative way to measure $A_{ol}$

- Measuring the very high $A_{ol}$ is problematic as the amplifier is unstable.
- A method for measuring $A_{ol}$ is shown below.




$$v_n = \frac{v_o}{A_{ol}}$$

$$A_{ol} = \frac{v_o}{v_Y} \times 101$$

**Exercise:** Prove the equation by equating currents between $v_Y$ and ground

# Hints for calculations

**Design Notes Expt 5**

**Setting the differential input resistance**

$$R_{id} = 2r_{be} = \frac{2\beta_o}{g_m} = \frac{2\beta_o}{40I_C}$$

So bias current, $I_O$ in differential amplifier is

$$I_O = 2I_C = 2\frac{2\beta_o}{40R_{id}}$$

$$I_O = \frac{\beta_o}{10R_{id}}$$

Now to design the Widlar current mirror to bias the diff amp stage.

$$R_E I_O = V_T \ell n\left(\frac{I_{ref}}{I_O}\right) \text{ or } I_{ref} = I_O \exp\left(\frac{I_O R_E}{V_T}\right)$$

Don't know $R_E$ or $I_{ref}$

Try $I_O R_E = V_T$

# Some advice

- Study the script and think about the design beforehand..
- **Use your ELEC271 notes!**
- **Bring your record of the pre-lab questions to the laboratory – needed when designing the complete OPAMP circuit.**
- Always check dc levels FIRST!! – check they are as expected
- Remember loading effects of one stage on another (Part 2 notes)
- Ask questions
- Good luck