**01. A \_\_\_\_** **memory address (MAR)\_\_\_\_\_\_ register specifies the address in memory for the next read or write.**

**02. A \_\_\_\_** **memory buffer (MBR)\_\_\_\_\_ register contains the data to be written into memory or receives the data read from memory.**

**03. The most common classes of interrupts are: program, timer, I/O and \_\_\_\_** **hardware failure\_\_\_\_.**

**04. A(n) \_\_\_\_** **timer\_\_\_\_\_ interrupt is generated by a timer within the processor and allows the operating system to perform certain functions on a regular basis.**

**05. A(n) \_\_\_\_** **I/O\_\_\_\_ interrupt is generated by an I/O controller to signal normal completion of an operation, request service from the processor, or to signal a variety of error conditions.**

**06. A \_\_\_\_** **disabled\_\_\_\_ interrupt simply means that the processor can and will ignore that interrupt request signal.**

**07. The collection of paths connecting the various modules is called the \_\_\_\_** **interconnection\_\_\_\_ structure.**

**08. A \_\_\_\_\_** **bus\_\_\_\_\_ is a communication pathway connecting two or more devices.**

**09. The \_\_\_\_\_** **control\_\_\_\_ lines are used to control the access to and the use of the data and address lines.**

**10. Bus lines can be separated into two generic types: \_\_\_** **dedicated\_\_\_\_ and multiplexed.**

**11. With \_\_\_\_\_\_** **asynchronous\_\_\_\_ timing the occurrence of one event on a bus follows and depends on the occurrence of a previous event.**