Bài 3:

	lw	sw	add	beq	j
RegDst	0	x	1	x	x
RegWrite	1	0	1	0	0
MemRead	1	x	x	x	x
MemWrite	0	1	0	0	0
MemtoReg	1	x	0	x	x
Branch	0	0	0	1	0
Jump	0	0	0	0	1
ALUSrc	1	1	0	0	x
ALUOp	00	00	10	01	xx