Toronto Metropolitan University

Department of Electrical, Computer, & Biomedical Engineering
Faculty of Engineering & Architectural Science

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Instructor	Prof. Fei Yuan

Assignment/Lab Number:	Design Project
Assignment/Lab Title:	Amplifier Design Project

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1. Introduction

An amplifier can be simply described as an electronic device/component which increases or decreases the amplitude of an output compared to its input. The amount of amplification of a specific amplifier is measured by its "gain". For the output signal's amplitude to be increased, the amplifier should have an absolute gain larger than 1, whereas a lower powered signal would be produced by an amplifier with an absolute gain between 0 and 1. Transistor amplifiers are being used commonly today, and are of two types: Bipolar Junction Transistors(BJTs) and Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs). Bipolar Junction Transistors can be set up in 3 ways, namely, Common Emitter Amplifier (CE Amp), Common Base Amplifier (CB Amp), and Common Collector Amplifier (CC Amp). Each type of configuration has its own properties. The objective of this Design Project was to design, simulate, and implement an amplifier circuit which would fulfill a set of specifications

2. Specifications

The final design of the amplifier should possess the following specifications:

1. Power supply: **+10 V** relative to ground;
2. Total quiescent current drawn from the power supply: **No larger than 10 mA**;
3. No-load voltage gain (at 1 kHz): **|Avo| = 50 (± 10%)**;
4. Maximum no-load output voltage swing (at 1 kHz): **No smaller than 8 V peak to peak;**
5. Maximum loaded output voltage swing (at 1 kHz and RL = 1 $k\Omega$): **No smaller than 4 V peak to peak;**
6. Loaded voltage gain (at 1 kHz, with RL = 1kΩ): **No smaller than 90% of the no-load voltage gain;**
7. Input resistance (at 1 kHz): **No smaller than 20 kΩ;**
8. Amplifier type: **Inverting or non-inverting;**
9. Frequency response: **20 Hz to 50 kHz (−3 dB response);**
10. Type of transistor: **BJT;**
11. Number of stages (transistors): **No more than 3;**
12. Capacitors permitted: $\mathbf{0.1\ \mu F}$, $\mathbf{1.0\ \mu F}$, $\mathbf{2.2\ \mu F}$, $\mathbf{4.7\ \mu F}$, $\mathbf{10\ \mu F}$, $\mathbf{47\ \mu F}$, $\mathbf{100\ \mu F}$, $\mathbf{220\ \mu F}$
13. Resistances permitted: **Values smaller than 220 kΩ from the E24 series.**
14. Other components (BJTs, diodes, Zener diodes, etc.): Only those present in the ELE404 lab kit. Additional Requirements:
    a. The output voltage must be free from distortions (clipping, etc.) under all test conditions.
    b. The source resistance, Rs, must be 600 Ω under all test conditions.

To meet the specifications, an amplifier circuit with 3 BJT connected as CC-CE-CC will be used.

3. Calculation and Analysis

What we know:

Firstly, what we already know from the required specifications is that Vcc is +10V from requirement 1 and that the frequency is 1kHz. Also, we know that the no-loaded voltage gain (Avo) has to be around 50 V/V (±10%) and the loaded voltage gain (Av) has to be around 90% of 50 (±10%) which is 40 to 60 V/V. The input resistance (Rin) has to be no smaller than 20 kΩ. Also, we know that RL (load resistance) is 1 kΩ and that the maximum loaded output swing cannot be smaller than 4 V peak to peak (Vo pk-pk = 4 V). Additionally for not loaded output swing cannot be smaller than 8 V peak to peak. Rest of the specifications will be tried to be met when trialing and erroring the final design.

To start, since the voltage gains we need to have in our circuit are massive (around 40-50 V/V) and the input resistance we need is also massive (around 20 kΩ), we need to possess an amplifier or a multistage amplifier that fulfills these requirements. After careful consideration, The first stage (CC stage) of the amplifier is used to reach the input resistance design specification of 20kΩ. Then, a common emitter amplifier (CE amp) is essential as it provides the high amount of voltage gain we need, but the common collector amplifier (CC amp) stabilizes the 1kΩ load by reducing the output resistance so that the gain does not drop by a significant amount..

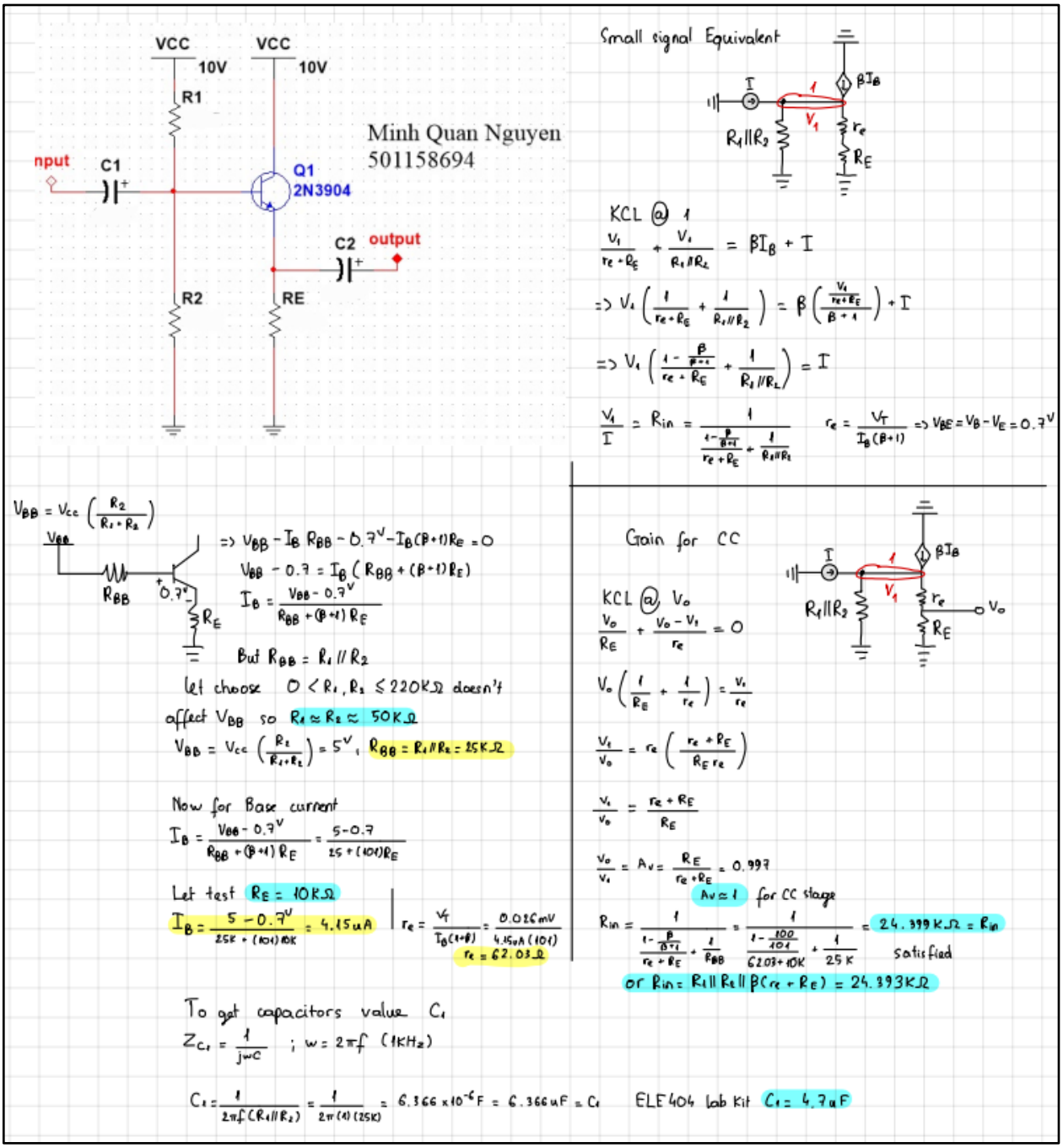
So overall, stage 1 will be the CC amplifier with CE amplifier followed by the CC amplifier (multistage amplifier) in order to stabilize the 1kΩ load by reducing the output resistance so that the gain does not drop by a significant amount.

Assumptions:

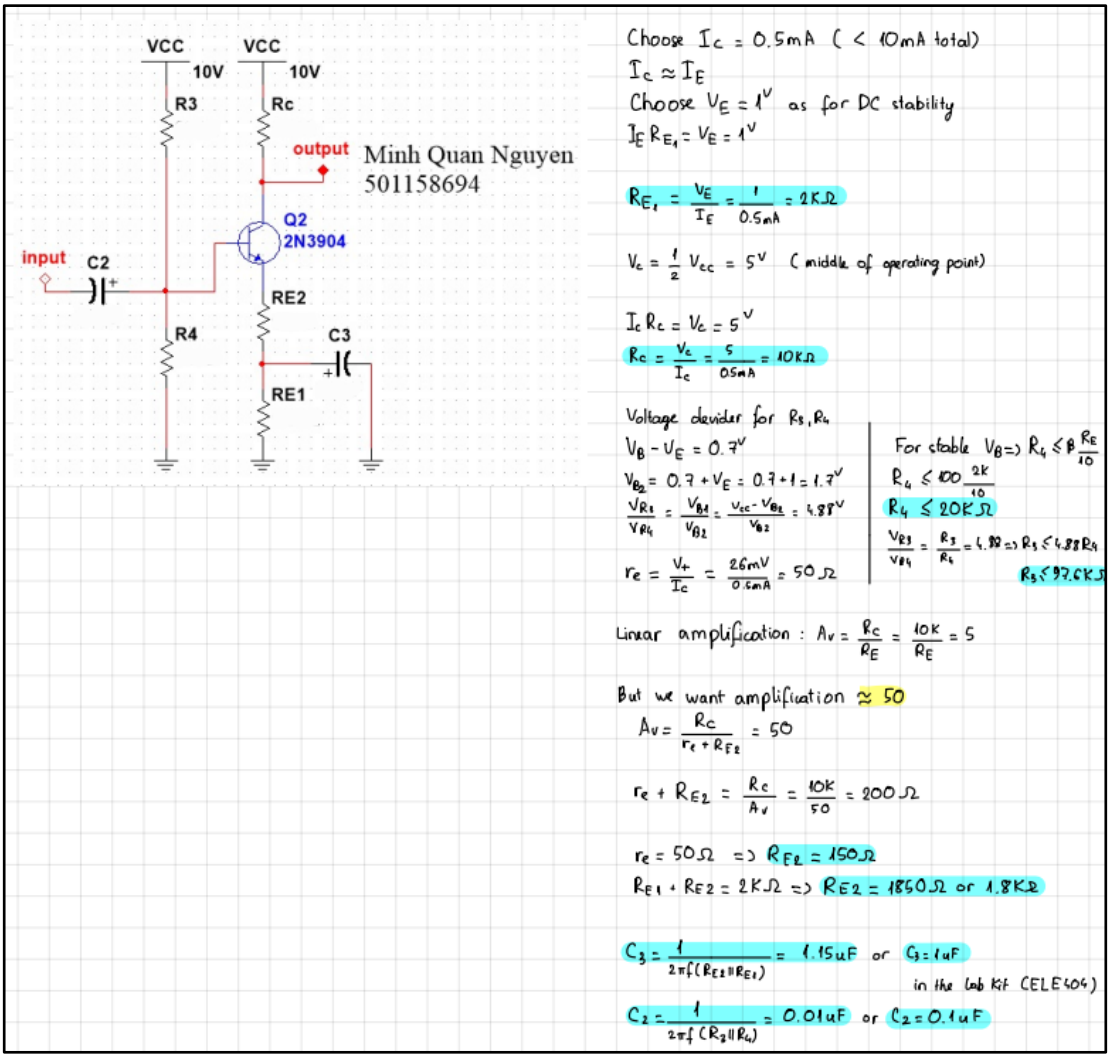
For our amplifier to work, we need to first establish some assumptions. Using our **2N3904 transistor** characteristics, we can assume β = 100. Also, since an amplifier has to be in active mode, we know all of this: $V_{BE,ON} = 0.3V$; $V_{CE,sat} = 0.7V$; $I_C = \beta I_B$; $I_C = (\frac{\beta}{\beta+1})I_E$; and $V_{CE} > V_{CE,sat}$. Using this information, stages 1, 2, and 3 can be analyzed.

Manual Calculation:

First Stage (CC Amplifier)



Second Stage (CE Amplifier)



Choose $I_C = 0.5mA$ (< 10mA total)

$I_C \approx I_E$

Choose $V_E = 1^V$ as for DC stability

$I_E R_{E_1} = V_E = 1^V$

$R_{E_1} = \frac{V_E}{I_E} = \frac{1}{0.5mA} = 2K\Omega$

$V_c = \frac{1}{2} V_{cc} = 5^V$ (middle of operating point)

$I_c R_c = V_c = 5^V$

$R_c = \frac{V_c}{I_c} = \frac{5}{0.5mA} = 10K\Omega$

Voltage devider for R_3, R_4

$V_B - V_E = 0.7^V$

$V_{B_2} = 0.7 + V_E = 0.7 + 1 = 1.7^V$

$\frac{V_{R_3}}{V_{R_4}} = \frac{V_{B_1}}{V_{B_2}} = \frac{V_{cc} - V_{B_2}}{V_{B_2}} = 4.88^V$

$r_e = \frac{V_t}{I_c} = \frac{26mV}{0.5mA} = 50\Omega$

For stable V_B => $R_4 \leq \beta \frac{R_E}{10}$

$R_4 \leq 100 \frac{2K}{10}$

$R_4 \leq 20K\Omega$

$\frac{V_{R_3}}{V_{R_4}} = \frac{R_3}{R_4} = 4.88 \Rightarrow R_3 \leq 4.88 R_4$

$R_3 \leq 97.6K\Omega$

Linear amplification : $A_V = \frac{R_c}{R_E} = \frac{10K}{R_E} = 5$

But we want amplification ≈ 50

$A_V = \frac{R_c}{r_e + R_{E_2}} = 50$

$r_e + R_{E_2} = \frac{R_c}{A_V} = \frac{10K}{50} = 200\Omega$

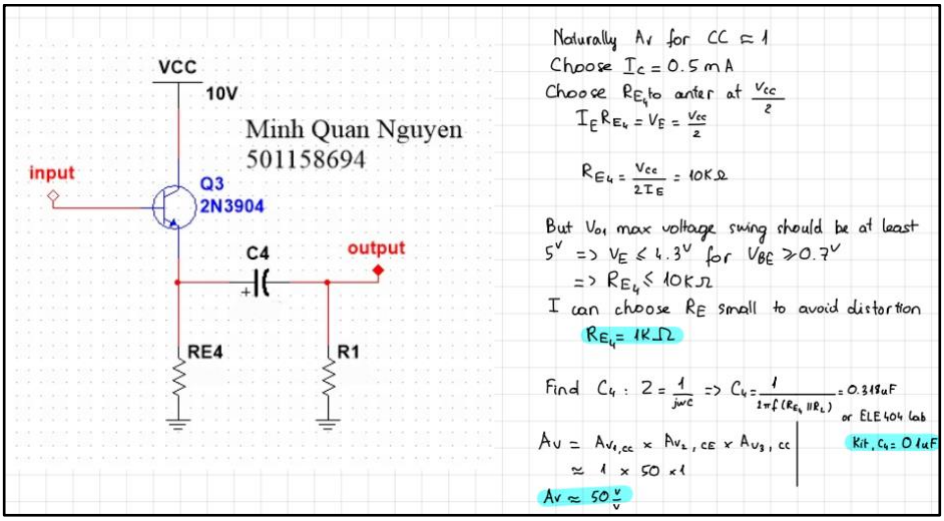
$r_e = 50\Omega \Rightarrow R_{E_2} = 150\Omega$

$R_{E_1} + R_{E_2} = 2K\Omega \Rightarrow R_{E_2} = 1850\Omega$ or $1.8K\Omega$

$C_3 = \frac{1}{2\pi f (R_{E_2} \| R_{E_1})} = 1.15uF$ or $C_3 = 1uF$ in the lab kit CELE404)

$C_2 = \frac{1}{2\pi f (R_3 \| R_4)} = 0.01uF$ or $C_2 = 0.1uF$

Third Stage (CC Amplifier)



Naturally A_V for CC $\simeq 1$

Choose $I_C = 0.5mA$

Choose R_{E_4} to anter at $\frac{V_{cc}}{2}$

$I_E R_{E_4} = V_E = \frac{V_{cc}}{2}$

$R_{E_4} = \frac{V_{cc}}{2 I_E} = 10K\Omega$

But V_{o_1} max voltage swing should be at least 5^V => $V_E \leq 4.3^V$ for $V_{BE} \geq 0.7^V$

=> $R_{E_4} \leq 10K\Omega$

I can choose R_E small to avoid distortion

$R_{E_4} = 1K\Omega$

Find C_4 : $Z = \frac{1}{j\omega C}$ => $C_4 = \frac{1}{2\pi f (R_{E_4} \| R_L)} = 0.318uF$ or ELE 404 lab Kit, $C_4 = 0.1uF$

$A_V = A_{V_1,cc} \times A_{V_2,CE} \times A_{V_3,cc}$

$\simeq 1 \times 50 \times 1$

$A_V \simeq 50 \frac{V}{V}$

4. Simulation

Circuit Simulation

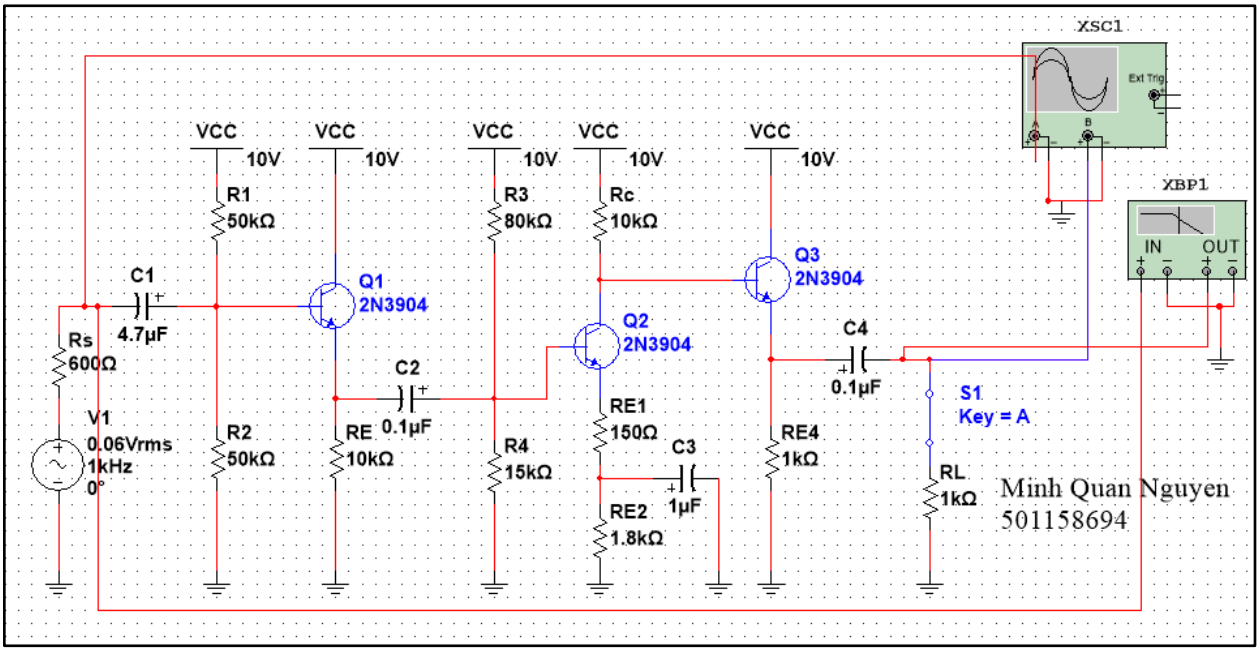


Figure 1. Simulated Circuit Design

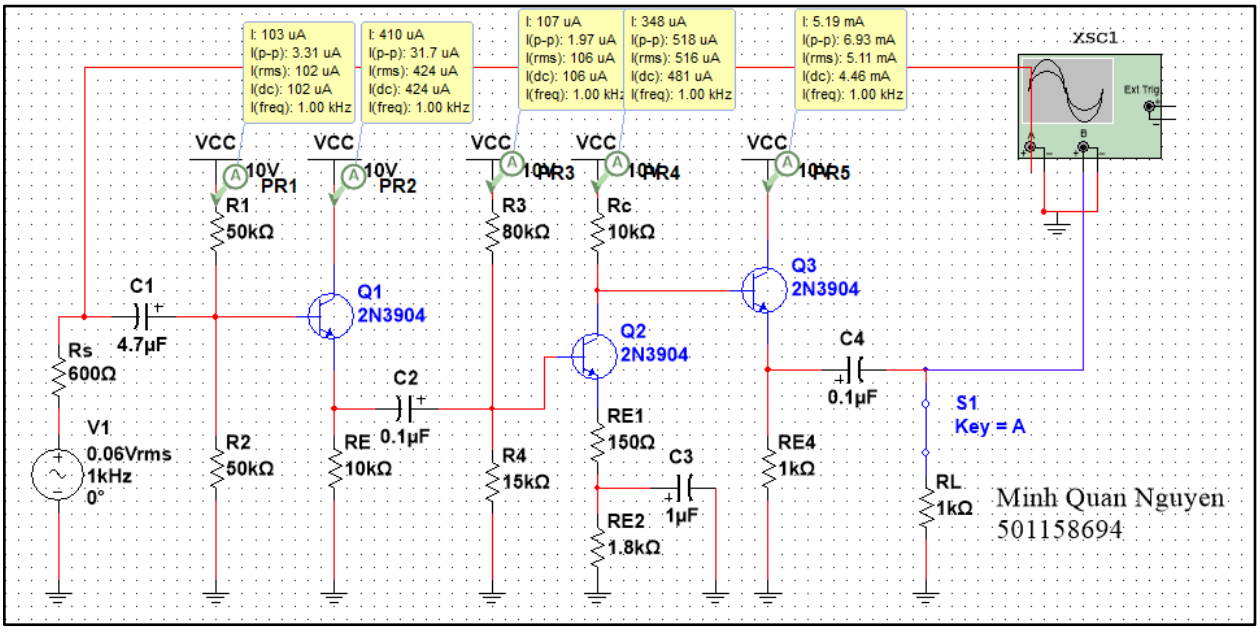


Figure 1.a. Simulated Circuit Design Notation

Simulation Result

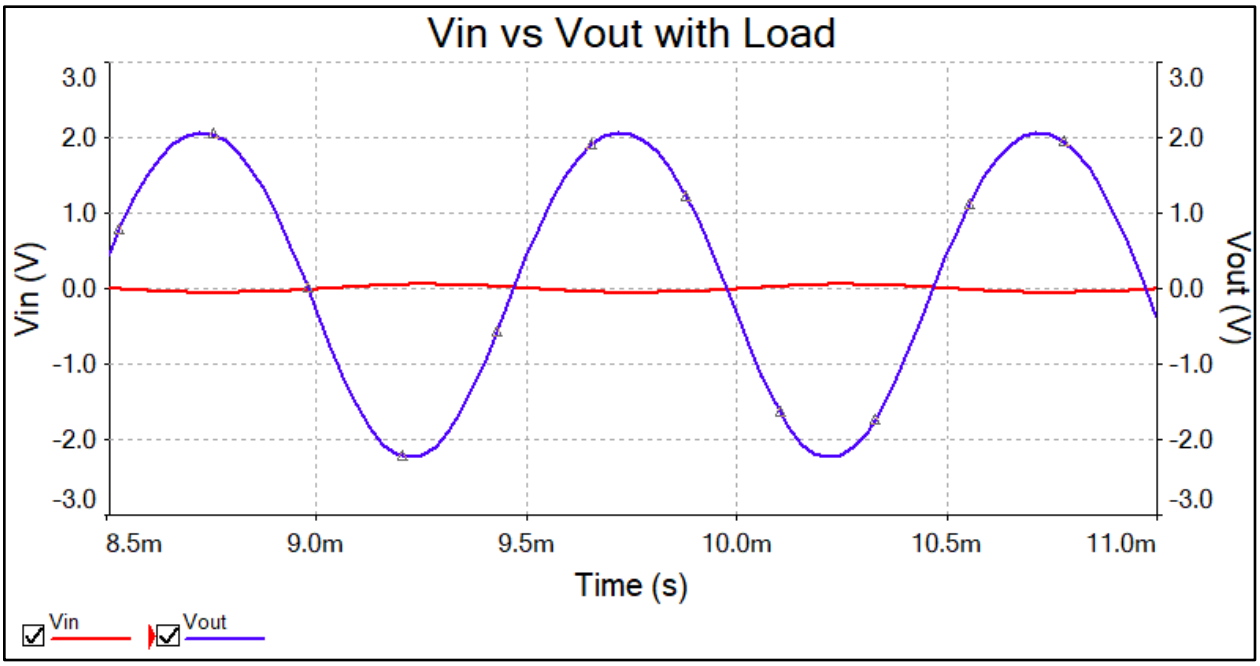


Figure 2. Graph of input voltage and output voltage with load

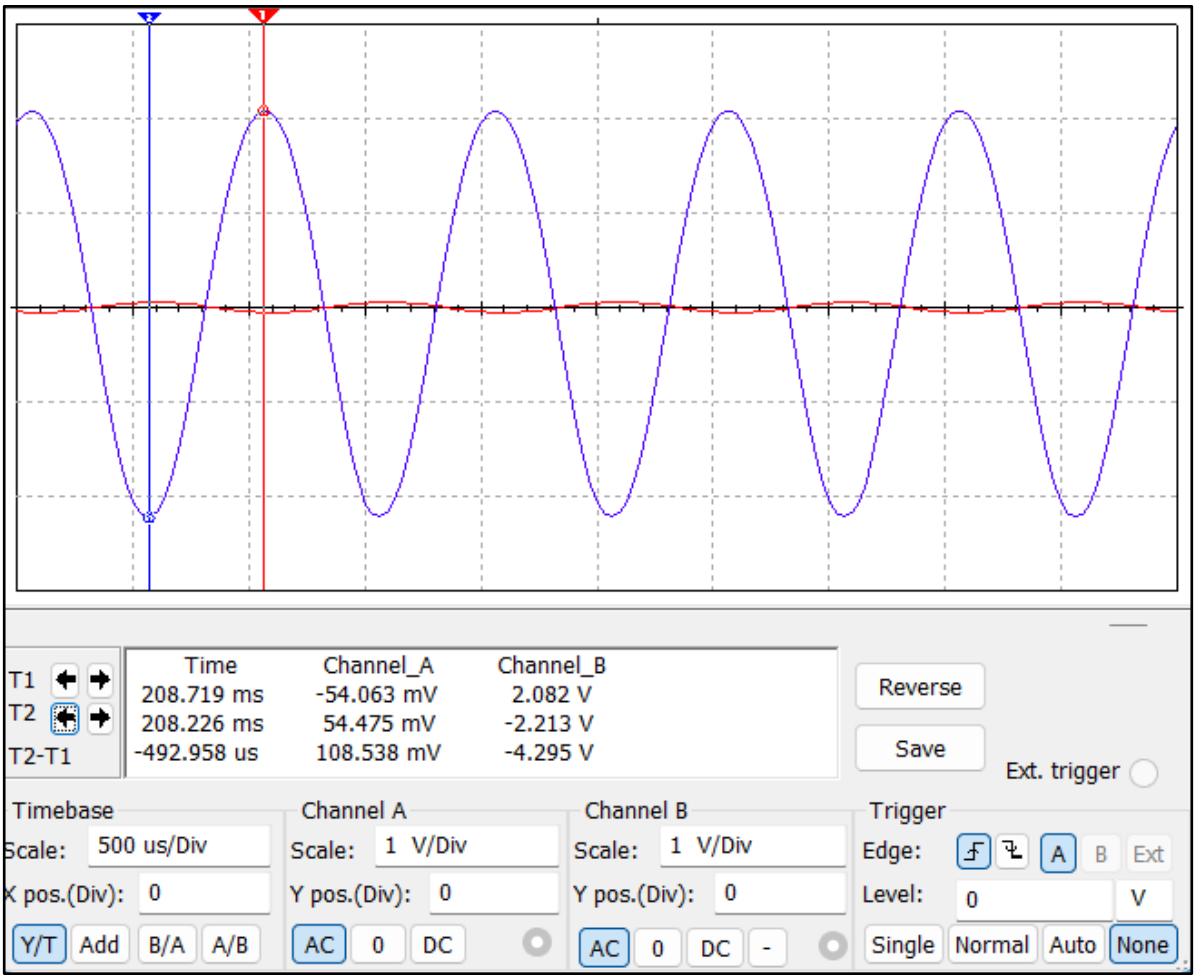


Figure 2.a Graph of input voltage and output voltage with load

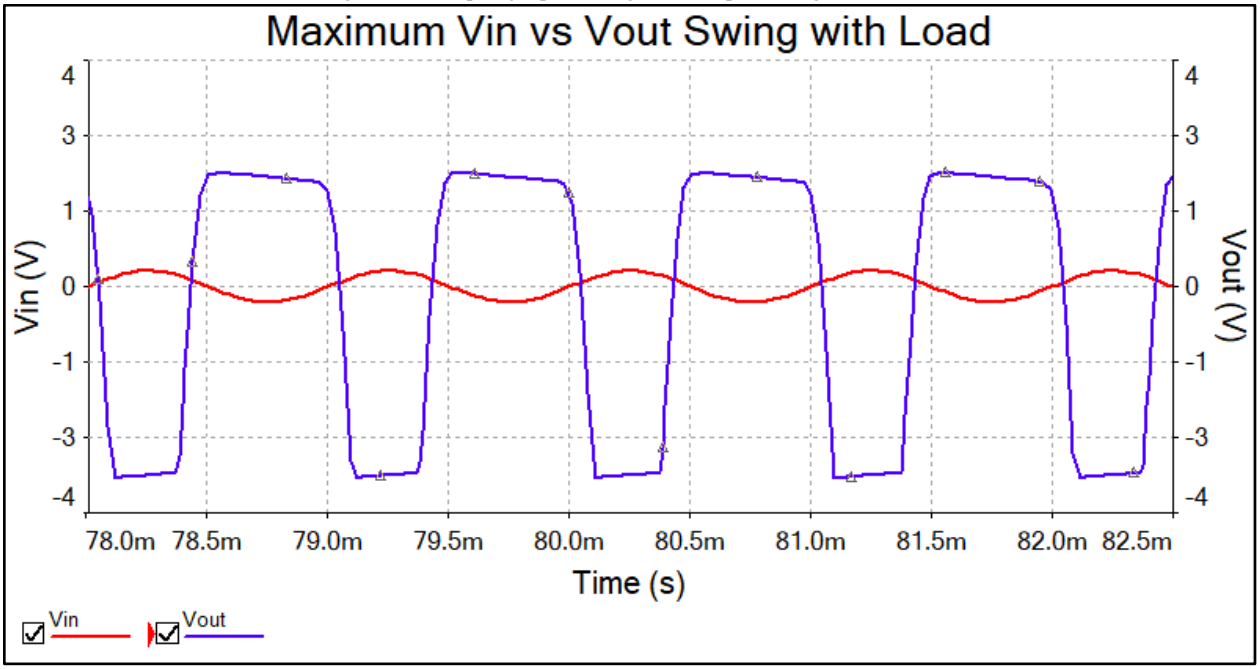


Figure 2.b Graph of maximum input voltage and output voltage with load

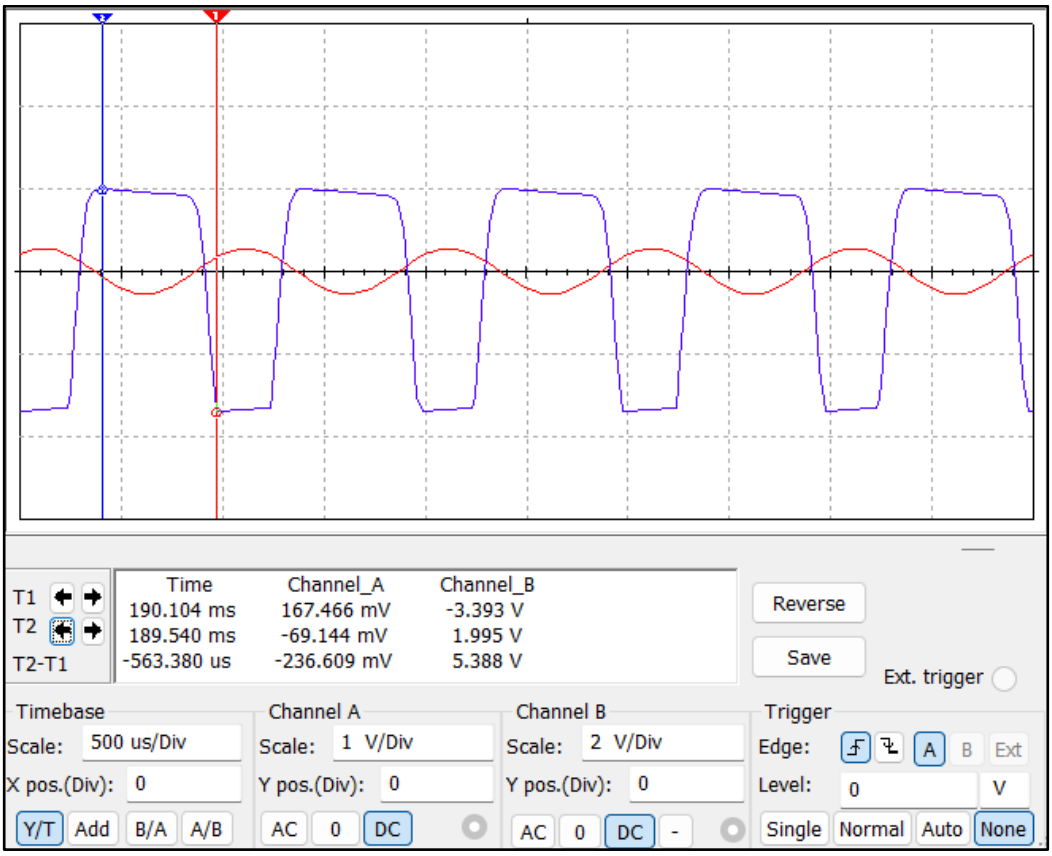


Figure 2.c Graph of maximum input voltage and output voltage with load

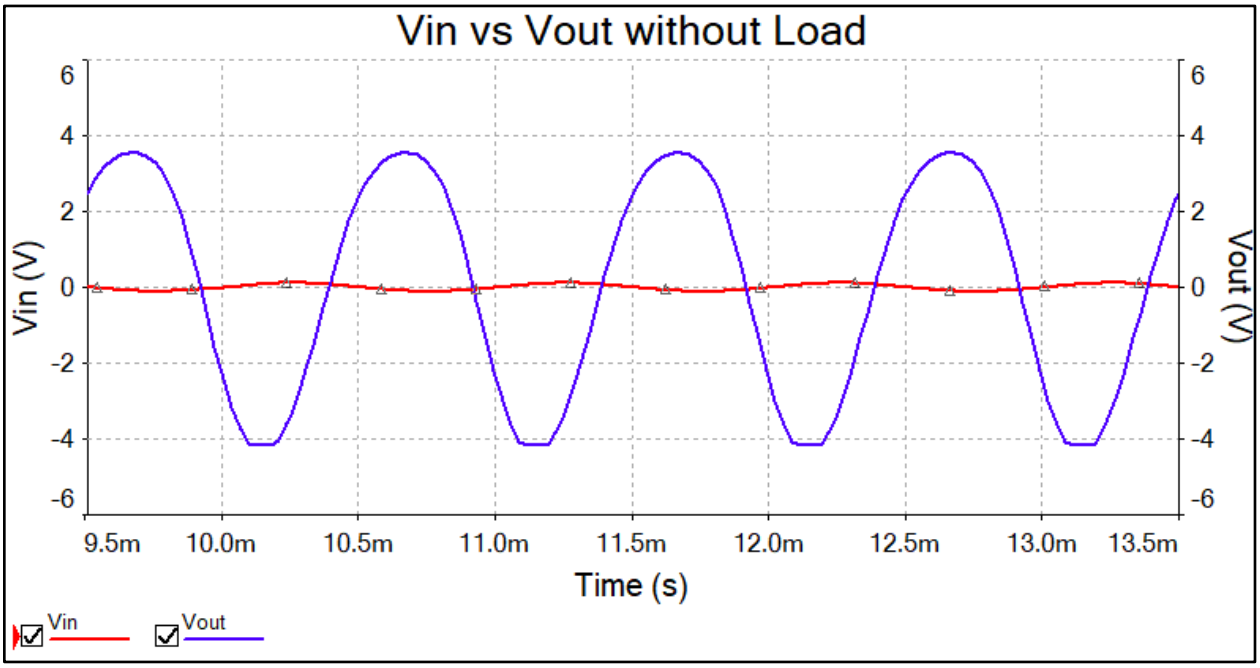


Figure 3. Graph of input voltage and output voltage without load

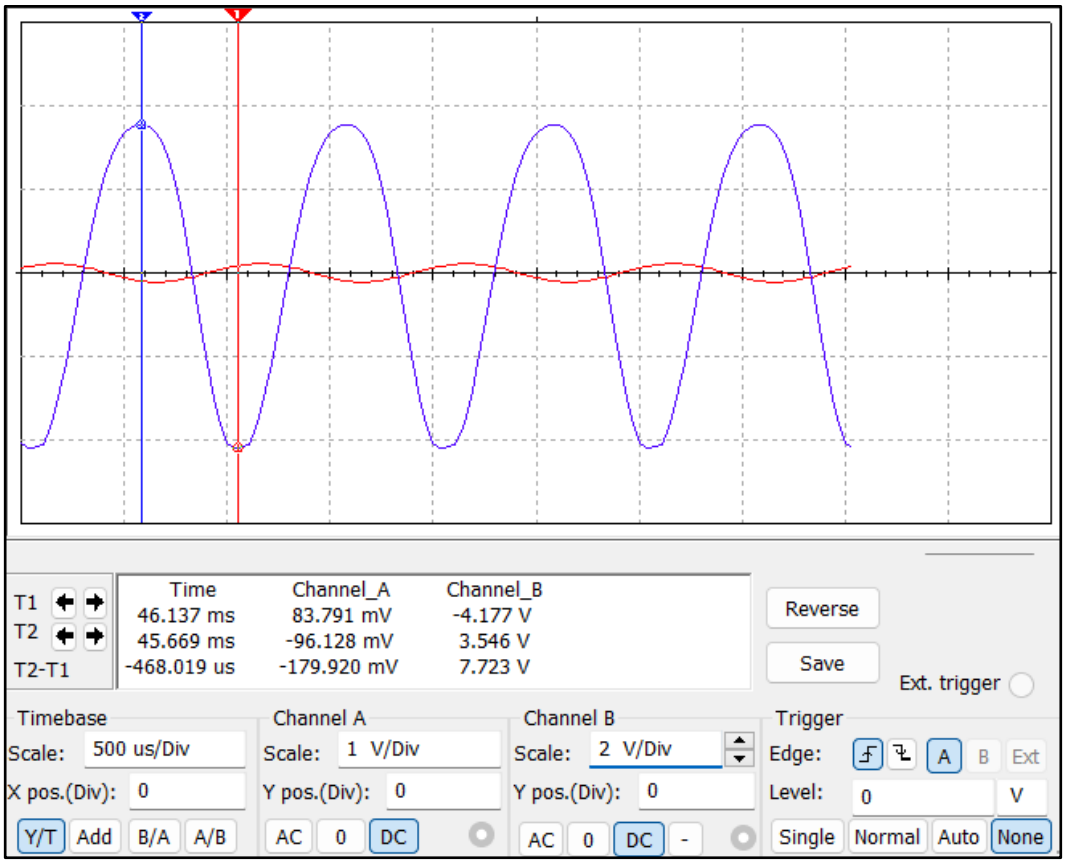


Figure 3.a Graph of input voltage and output voltage without load

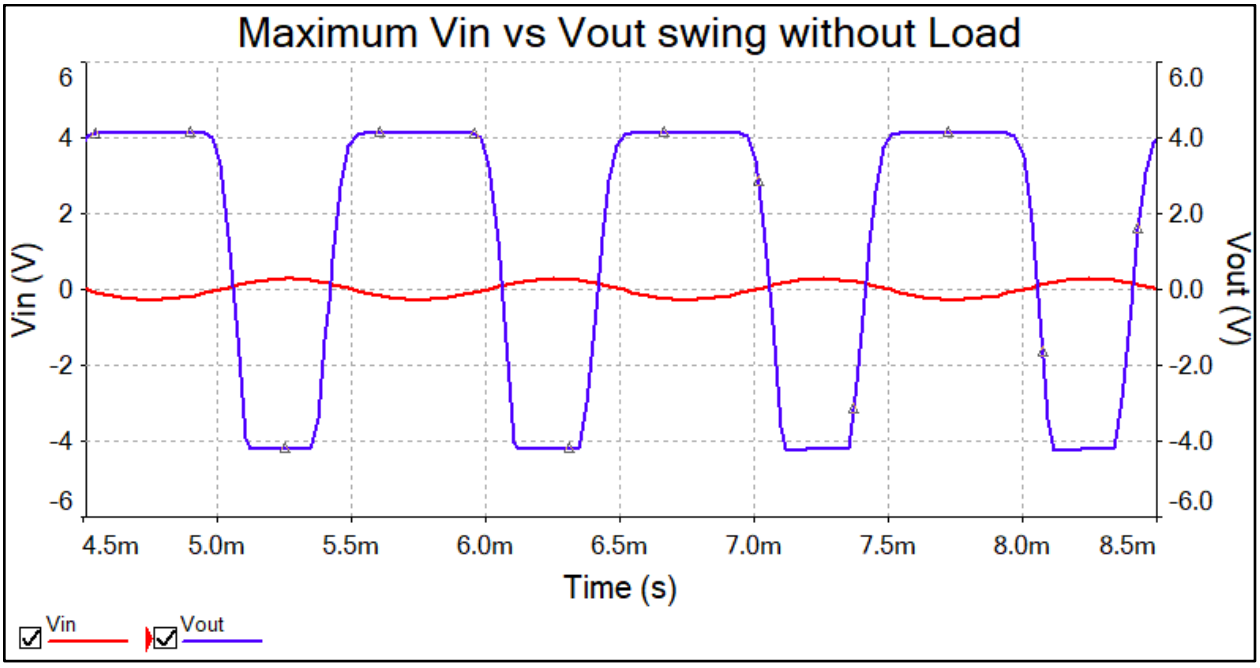


Figure 3.b Graph of maximum input voltage and output voltage without load

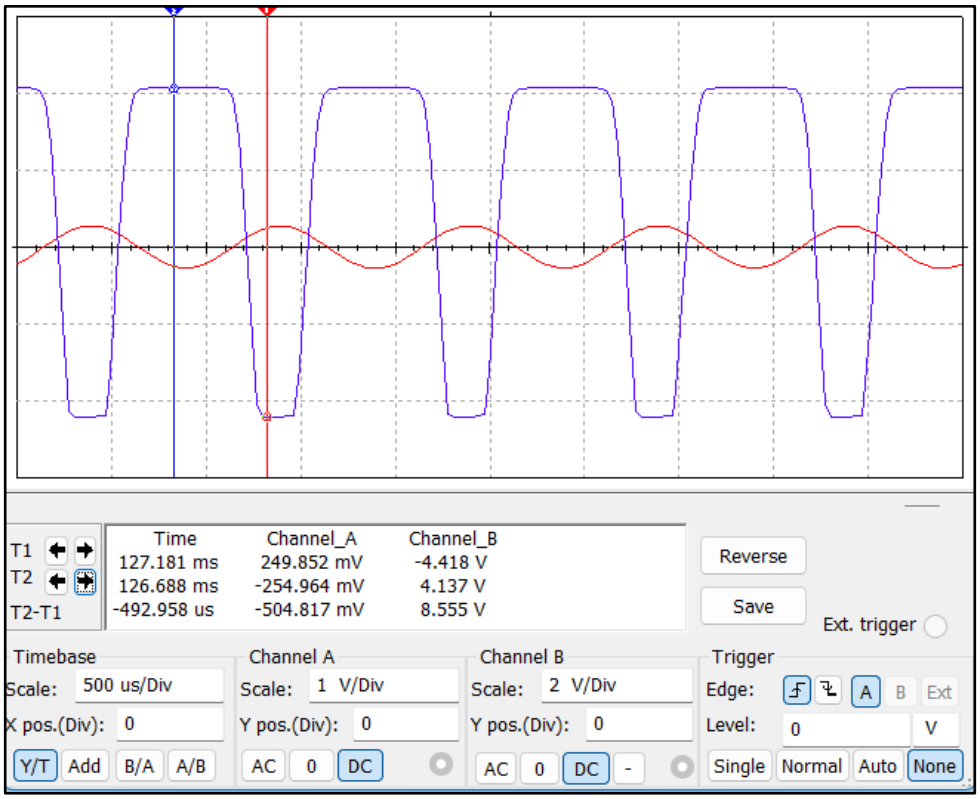


Figure 3.c Graph of maximum input voltage and output voltage without load

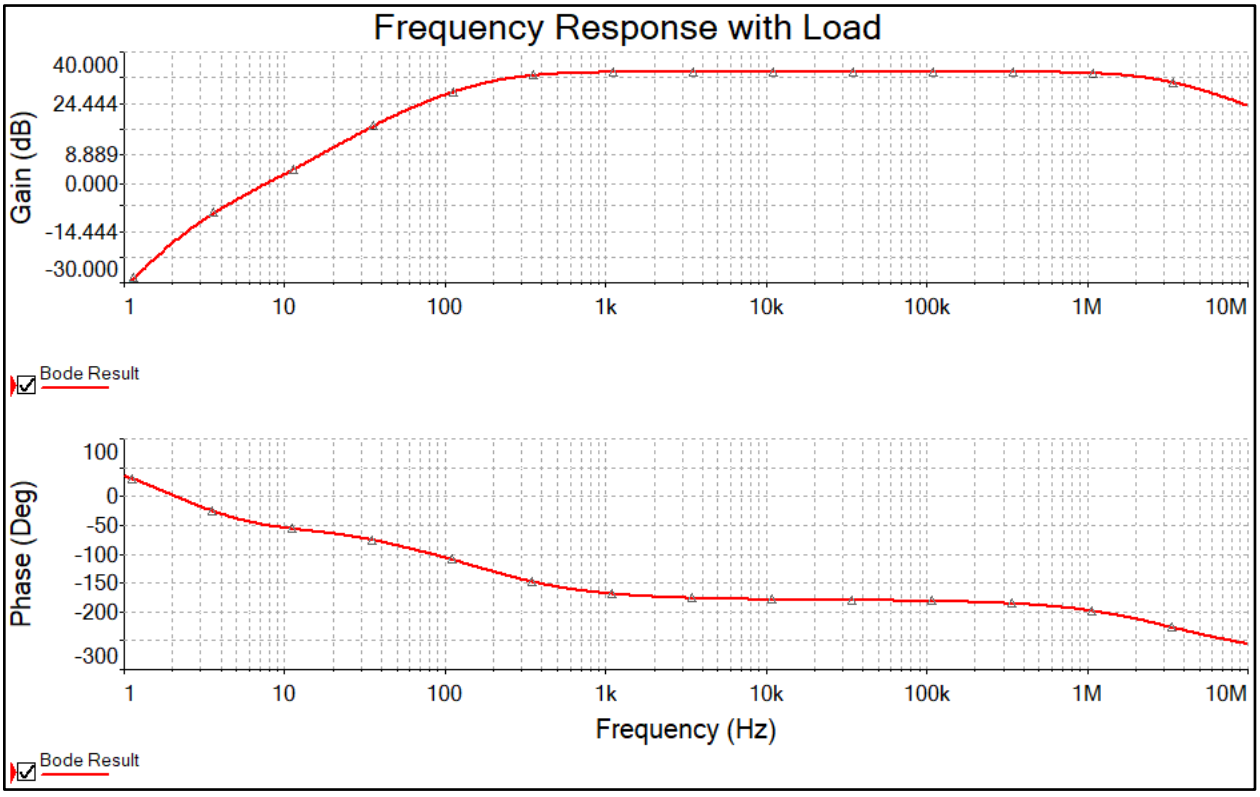


Figure 4. Graph of circuit's frequency response with load

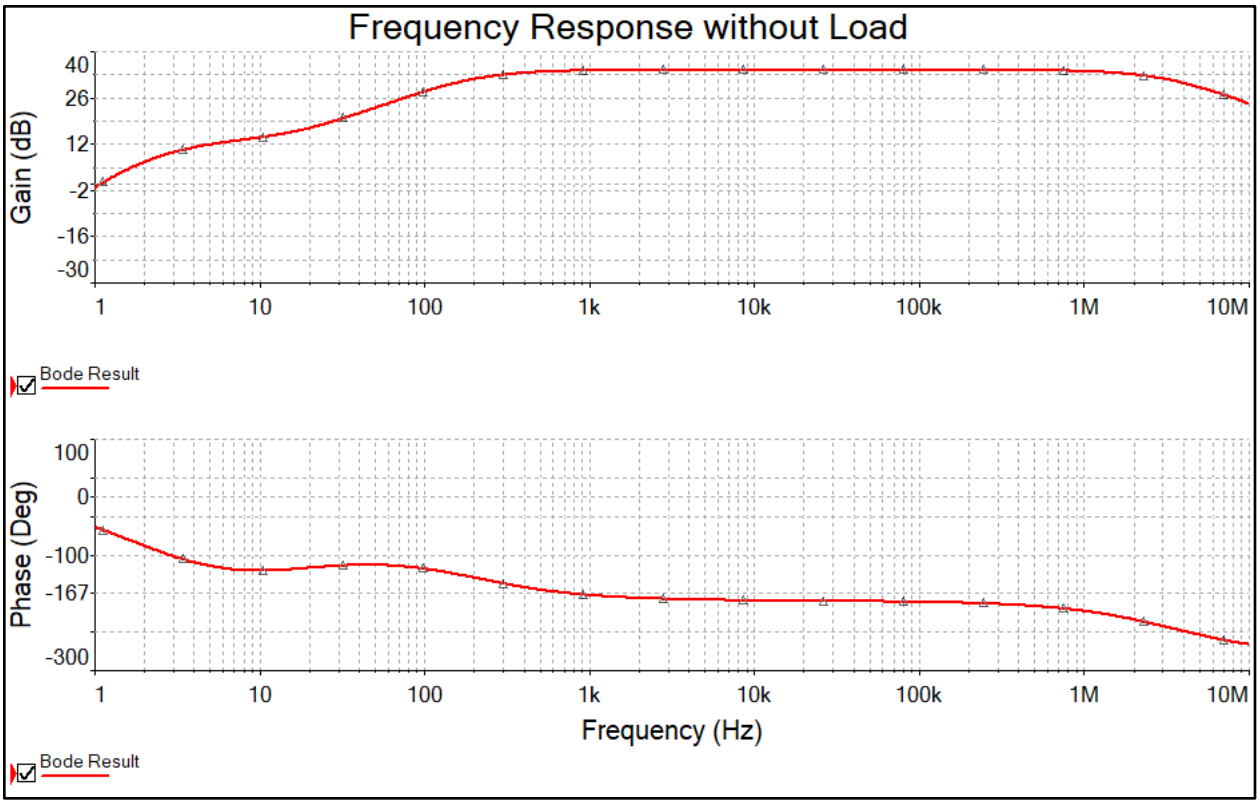


Figure 4.a Graph of circuit's frequency response without load

When testing the circuit without any load, I applied a 80mV input signal and observed a voltage gain of approximately 50. However, when a load was introduced, the voltage gain dropped to around 40 under the same conditions. The calculated Capacitor values gave me the clearest waveform with minimal distortion, therefore I chose them for this final design after the calculation.

Considering the operational limits of amplifier clipping, the circuit has a maximum swing of 8.555 volts peak-to-peak (Vpp) without load, restricting it to a range between +4.275V and -4.275V with clipping. With a load, the maximum swing reduces to 5.388 volts peak-to-peak, limiting it between +2.69V and -2.69V.

Examining its frequency response, the circuit achieves its maximum gain starting from 1kHz onwards up to more than 50kHz. Additionally, the lower cutoff frequency is approximately 100Hz, indicating its operational range in terms of frequency.

The quintessential current drawn from the power supply is the sum of all the current drawn from each stage of the amplifier. For this amplifier configuration of Figure 1.a, the quintessential **current draw is 5.583mA** (PR1 + PR2 + PR3 + PR4 + PR5 = 102uA + 424uA + 106uA + 481uA + 4.51mA = 5.623mA). This lies within the design specification of below 10mA. Frequency response: satisfied **20 Hz to 50 kHz (−3 dB response);**

5. Conclusion and Remarks

This design project was very useful in helping me understand how a single-supply multistage amplifier works and functions. The analysis in the project was long and tedious (with many different tests and trial and error) but it gave me an idea and helped me solidify my BJT transistor knowledge. With this project, I have revised and solidified my knowledge of the DC analysis and the AC analysis of amplifiers like the CE amps and CC amps and I also discovered many new things. Firstly, I learned how to find the voltage gain of a multistage amplifier by multiplying the gains of each section separately. I also discovered how to calculate the input resistance with AC analysis and how to approximate the capacitor values with the impedance formula.

Following the testing of the circuit, it is confirmed that the circuit fulfills the design specifications noted at the top of the report. However, differences in the output waveform were found when testing for the maximum voltage swing. When testing for an input voltage of 0.08V, there is a minor distortion of the bottom half of the wave seen as negative cycle clipping. This distortion can be mitigated by adjusting the DC operating point. This issue and any others may be caused by the use of estimation throughout the manual calculation segment where the components are chosen.

Other than the distortion the circuit performs as expected with all of the specifications being met. The circuit can provide the necessary voltage gain of 50 both with and without load, its quintessential current draw is below 10mA (5.583mA), and the maximum output voltage swing for both with and without load is within specification (approximately 8 Vpp without Load and 4 Vpp with Load), the input resistance is larger than 20kΩ (24.399kΩ), the frequency response covers the range specifies and all components are within specification.

In conclusion, other than the slight distortion and not being able to meet 8Vpp in the output caused by estimations in the calculation segment. My final circuit design on Multisim followed most of the specifications but it was not perfect due to some assumptions that were made which did not work.