Tech Web Hand Book

DC/DC Buck Converter PCB Layout Basics

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Introduction

It goes without saying that circuit configuration and component selection are important in the design of a DC/DC converter, but the layout of the PCB (Printed Circuit Board) is equally or even more important. Even if the circuit drawing and component constants are correct, if the PCB layout is not appropriate, not only will performance not be achieved, but it will not even work. In many cases, the PCB layout is the cause of problems such as I made a prototype, but it doesn't work properly.

In the case of a switching power supply that has a lot of noise but is still working, the power supply may be able to handle the situation, but the noise it emits may cause the S/N of the system to drop, and the system may not meet the specifications.

Common problems caused by PCB layout include noise at the output (including spikes and oscillations), poor regulation, and unstable operation. These can be solved by optimizing the PCB layout, but redoing the PCB design, even for prototyping, is a major loss of time, money, and effort. For a quick and reliable design, it is important to have a high-quality PCB design from the beginning, with the key points of PCB layout.

This document basically describes the PCB layout of a DC/DC buck converter (switching power supply) with diode rectification or synchronous rectification. Although there are parts that can be shared with other methods and topologies, the contents are specific to these buck converter types.

1. What You Need to Know First

The key to designing a board is the layout of the components and wiring, and there are reasons why it is better to do so. Some of the reasons include those specific to switching circuits, electrical characteristics of components, and those related to the materials and structure of the PCB. The following is an overview of the minimum things you should know when designing a PCB.

1.1 Main Principles of PCB Layout

A list of the main principles of PCB layout is given from the beginning. The following explanations are based on these points. I hope you will read this book with these points in mind.

Main principles of buck converter PCB layout

- Input capacitors and output diodes are placed on the same surface as IC pins, and as close to ICs as possible.
- Thermal vias are provided as necessary.
- Inductors minimize radiation noise from switching nodes, and so although while not as important as input capacitors, are arranged close to ICs.
- The copper layer pattern area should not be made larger than necessary.
- Output capacitors are placed close to inductors.
- Feedback paths are wired so as to be kept far from noise sources such as an inductors and diodes.
- Corner wiring is rounded.

1.2 Current Path of DC/DC Buck Converter in Operation

A switching regulator is an analog circuit, but in contrast with circuits that operate mainly in linear modes, current and voltage are switched, that is, turned on and off. Therefore, it is necessary to determine the optimal component placement and current path by considering which node and line will have what nature of voltage and what kind of current will flow.

This means that the size and nature of the voltages and currents in each part of the circuit have a great deal to do with the PCB layout. Therefore, it is important to know the current paths and properties of the buck converter during operation in order to understand what needs to be considered in the PCB layout.

Figure 1 shows a schematic diagram of a diode rectified (asynchronous rectification) DC/DC buck converter circuit: the capacitor on the BOOT pin is for bootstrapping to drive the built-in Nch-MOSOFET, and the resistor and capacitor connected to the COMP pin are for phase compensation. These pins may not be present in some ICs. The other pins and components are basic pins and necessary external components.

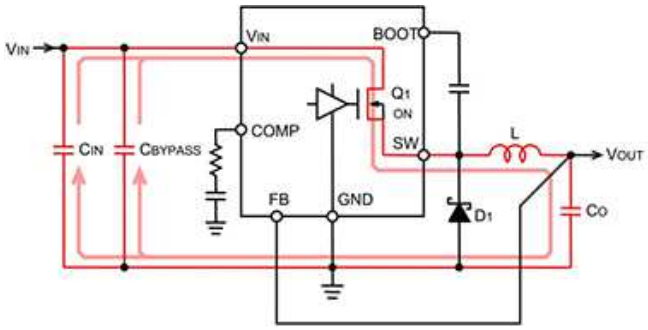


Figure 1. Current paths when the switching element Q_1 is turned on

The red lines in Figure 1 show the paths and directions of the main currents flowing when the switch Q_1 is turned on. C_{BYPASS} is a high-frequency decoupling capacitor, and C_{IN} is a capacitor with a large capacitance.

The instant that the switch Q_1 is turned on, a steeply rising current flows, but most of the current is supplied from C_{BYPASS}, and then from C_{IN}. A gently changing current is supplied from the input power supply.

The red lines in Figure 2 show the current paths when the switch Q_1 is turned off. The diode D_1 is turned on, and energy accumulated in the inductor L is discharged to the output side.

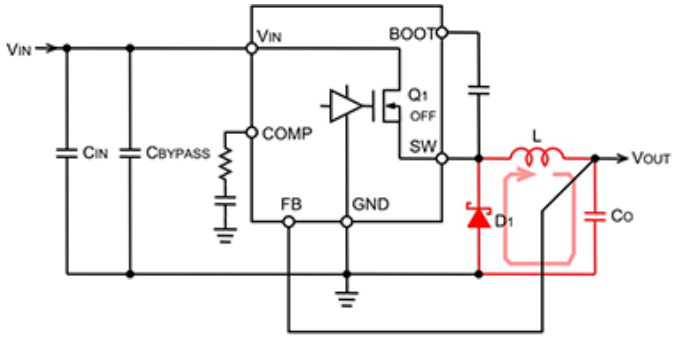


Figure 2. Current paths when the switching element Q1 is turned off

An inductor is inserted in series with the output of the buck converter, and so the current in the output capacitor rises and falls, but is smooth.

The red lines in Figure 3 represent the difference between Figures 1 and 2. Each time the switch Q_1 switches from off to on or from on to off, current flowing in the parts indicated by red lines changes suddenly. Changes in this system are steep, and so the current waveform includes numerous harmonics.

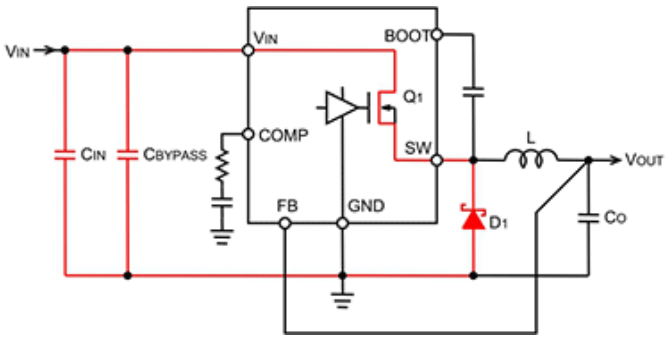


Figure 3. Important places in layout relating to current differences

These different parts are especially important and must be given the greatest amount of attention in the PCB layout process.

In overview, the current flow is the same whether the switching transistor is external or synchronous rectification type where the rectifier diode is replaced by a transistor. The following explanations are based on this current flow, so please make sure you understand this current path.

＜Summary＞

- When engaging in PCB layout (design), it is important to understand the current paths in the step-down converter.
- The sudden on-off of the currents in the switching operation of a switching regulator can adversely affect circuit operation and the like if measures are not taken in an appropriate PCB layout.

1.3 Ringing at Switching Nodes

There are parasitic capacitances and inductances in real PCBs. The effect of these parasitics is unexpectedly large, and when a circuit does not work properly even though there is nothing wrong with it, it is often due to insufficient consideration of parasitics in the layout. When drawing actual wiring patterns, it is necessary to deal with parasitics in many places.

In this section, we will examine the factors that cause ringing using the switching node as an example, which requires the most attention.

Figure 4 shows the parasitic capacitance and inductance in a synchronous rectification type step-down DC/DC converter circuit. C_1 to C_2 and L_1 to L_5, shown in blue, fall under this category. Parasitic capacitance and inductance exist in the circuit on the PCB, causing high-frequency ringing as shown in the figure in the red frame when the

switch is turned on and off.

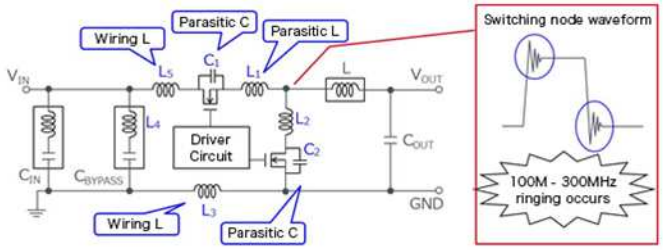


Figure 4. Ringing image of parasitic capacitance, inductance and switching node waveform in the circuit on the PCB

The inductance of printed wiring is of the order 1 nH per millimeter. In other words, if the wiring is unnecessarily long, the wiring inductance increases. Moreover, the rise time (t_r) and fall time (t_f) of a switching MOSFET are generally several nanoseconds. The voltage and current generated due to a parasitic component can be calculated using the following equations.

Basic equations:

$$I = C \times \frac{dV}{dt} \qquad V = L \times \frac{dI}{dt}$$

e.g.: Switching voltage = 5V, C = 1000pF

$$1000\text{pF} \times \frac{5\text{V}}{5\text{ns}} = 1\text{A} \qquad 10\text{nH} \times \frac{1\text{A}}{5\text{ns}} = 2\text{V}$$

The substitution of 10 nH assumes a wiring length of about 10 mm. It seems like a small length, but if a large current flows, we see that a high voltage is generated.

From the equation, if the t_r and t_f of the MOSFET as a switch are short, the current and voltage are both large. If t_r and t_f are fast, transition losses are reduced and efficiency can be improved, but the circuit becomes prone to the occurrence of ringing.

The ringing frequency band can be calculated as f = 1/time. If t_r and t_f are both 5 ns, then the period can be considered to be 10 ns, and so the frequency band is 100 MHz. In general, switching frequencies tend to range from 500 kHz to 1 MHz, and so ringing occurs at frequencies that are 100 to 200 times higher (Figure 5).

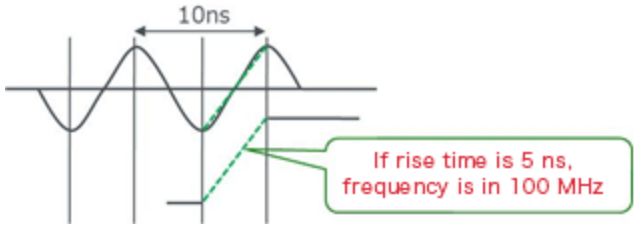


Figure 5. Example of how ringing frequency increases and becomes more sensitive as t_r becomes faster

We will now consider what kind of current flows due to the parasitic components of the circuit model shown in Figure 4. Figure 6 shows the case where the high-side MOSFET is turned on. The parasitic capacitance C_2 is charged, energy is stored in the parasitic inductances L_1 to L_5, and when the voltage at the switching node becomes equal to V_{IN}, the energy stored in L_1 to L_5 causes resonance together with C_2, and large ringing occurs.

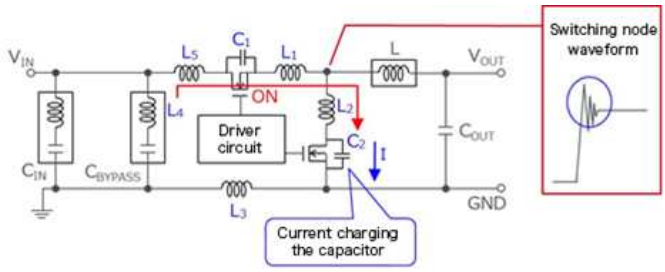


Figure 6. Current path and ringing when the high-side MOSFET is turned on

The energy P_{ON} stored in the parasitic inductance L when the high-side MOSFET is on and the resonant frequency f_{ON} can be calculated by the following equation.

$$P_{ON} = \frac{1}{2} \times (L_1 + L_2 + L_3 + L_4 + L_5) \times I^2$$

$$f_{ON} = \frac{1}{2 \times \pi \times \sqrt{(L_1 + L_2 + L_3 + L_4 + L_5) \times C_2}}$$

Next, the case where the high-side MOSFET is turned off is shown in Figure 7.

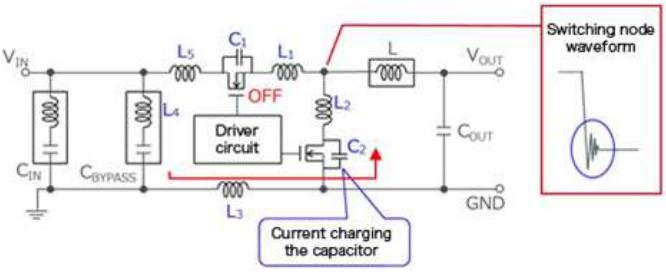


Figure 7. Current path and ringing when the high-side MOSFET is turned off

Even when the high-side MOSFET turns off, the inductor continues to carry current, so the parasitic capacitance C_1 of the high-side MOSFET is charged and the parasitic capacitance C_2 of the low-side MOSFET is discharged, and V_{OUT} decreases. When V_{OUT} falls below the V_F of the parasitic diode of the low-side MOSFET, all the inductor current flows to this diode and the charge of the high-side parasitic capacitance C_1 becomes zero, but the energy accumulated in the parasitic inductance until then causes resonance with C_1, resulting in large ringing. The energy P_{OFF} of the parasitic inductance when it is off and the resonance frequency f_{OFF} can be calculated by the following equation.

$$P_{OFF} = \frac{1}{2} \times (L_1 + L_2) \times I^2$$

$$f_{OFF} = \frac{1}{2 \times \pi \times \sqrt{(L_1 + L_2 + L_3 + L_4 + L_5) \times C_1}}$$

The inductance L_4 is determined by the characteristics of C_{BYPASS}. L_3 and L_5 vary greatly with the PCB layout. This circuit is an example in which a switching transistor is connected externally, but when an IC with an internal switching transistor is used, L_1, L_2 and C_2 are fixed values depending only on the IC, and do not depend on the PCB layout.

In this way, in an actual PCB there are components that do not appear in the circuit diagram, and consequently, for example large ringing may occur at a switching node in conjunction with switching if the PCB layout is not planned carefully, and often this may cause the circuit to not operate properly or to generate considerable noise or the like.

Now you can see why the main principle of PCB layout is to keep the wiring short.

＜Summary＞

- In actual PCBs, there exist parasitic capacitances and inductances that do not appear on circuit diagrams.
- Parasitic components may give rise to such problematic phenomena as ringing.

1.4 PCB Structure and Characteristics

For optimal PCB design, there are things to know not only about the layout but also about the board itself.

Figure 8 is a schematic diagram of a PCB cross section.

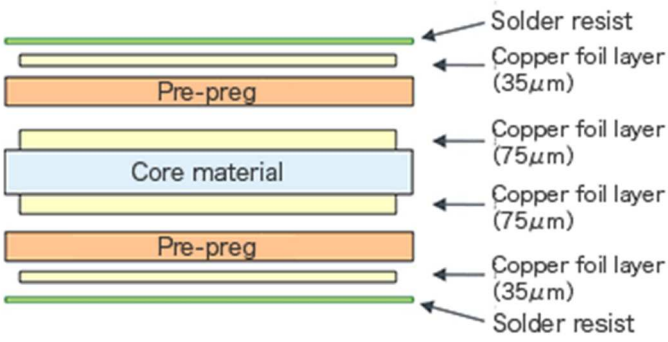


Figure 8. Basic structure of a PCB (cross section)

The basic substrate structure and the characteristics are also shown below.

- The copper foils on the front and back surfaces are often different in thickness from the inner layer.
- The copper foil of the core material is often thicker, which enhances heat dissipation.
- The core material is of general thickness, and the thickness is adjusted by prepreg.
- Depending on the type of core material and prepreg, some materials may cause migration and may not be able to withstand high humidity tests.

1.5 Resistance of Copper Foil

We need to understand not only the substrate, but also the copper foil that is the pattern wiring. Naturally, the copper foil has resistance. Under conditions where large currents flow, large conduction losses, i.e., voltage drops and heat generation, occur, so the resistance of the copper foil needs to be considered.

The resistance of copper foil is described as a value per unit area. Figure 9 indicates the resistance values per unit area of copper foil. The resistance values are for the generally application conditions of a copper foil thickness of 35 μm, width 1 mm, and length 1 mm.

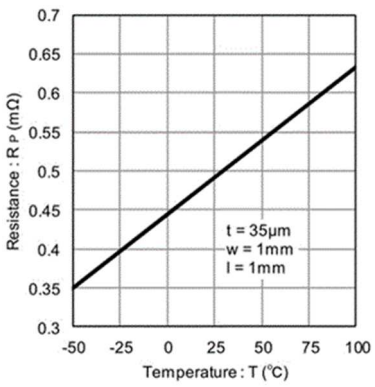


Figure 9. Basic structure of a PCB (cross section)

The following equation is used for general calculations of resistance.

$$R = \frac{\rho \times l}{t \times w} \times 10 \ [m\Omega]$$

l : Conductor length [mm]
w : Conductor width [mm]
t : Copper foil thickness [µm]
ρ : Copper resistivity [µΩcm]

$$\rho(T = 25℃) = 1.72 \ \mu\Omega cm$$

$$\rho(T) = \rho(Ta = 25℃) \times \{1 + 0.00385(T - 25)\} \ [\mu\Omega cm]$$

T : Temperature

The following equation is used for general calculations of resistance.

$$R = R_P \times \frac{l}{w} \times \frac{35}{t} \ [m\Omega]$$

R_P : Resistance value read off from graph [mΩ]

For example, at 25°C, the resistance value of copper foil of width 3 mm and length 50 mm, calculated as follows, is 8.17 mΩ.

$$R = R_P \times \frac{l}{w} \times \frac{35}{t} = 4.9 \times \frac{50}{3} \times \frac{35}{35} = 8.17 \ [m\Omega]$$

From this resistance value, the voltage drop when a 3 A current flows is 24.5 mV. If the temperature rises to 100°C, from the graph we see that the resistance value increases 29%. Hence the voltage drop also increases, to 31.6 mV.

This voltage drop due to the copper foil can be a major problem, depending on circumstances. In essence, the wiring width should be studied in view of the current and temperature conditions.

1.6 Inductance of Copper Foil

As already explained in Section 1.3, "Ringing at Switching Nodes," inductance exists in copper foil. In that sense, there are basically components such as resistance, capacitance, and inductance in almost everything.

The inductance of copper foil is expressed by the following equation.

$$L = 0.2 \times l \times \left(\ln \frac{2 \times l}{W + t} + 0.2235 \times \frac{w + t}{l} + 0.5 \right) \ [nH]$$

l : Conductor length [mm]
w : Conductor width [mm]
t : Copper foil thickness [µm]

From this equation, we see that the inductance of copper foil depends hardly at all on the foil thickness.

Figure 10 is a graph plotting the calculated inductance of the copper foil. As is clear from the graph, there is surprisingly little decrease in the inductance even when the line width is doubled.

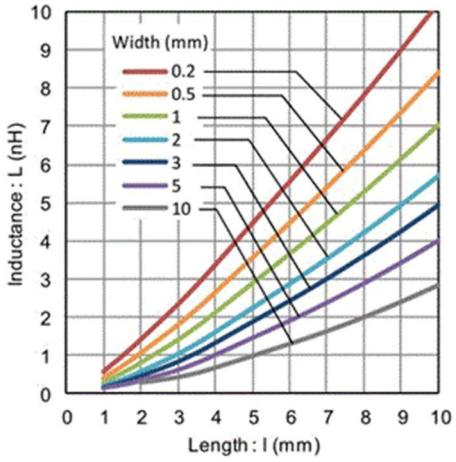


Figure 10. Inductance of copper foil

In order to suppress the effects of parasitic inductance, the best approach is to shorten wiring lengths.

If the current propagating in printed wiring with inductance L (H) changes by i (A) in time t (s), then the following voltage appears across the ends of the printed wiring.

$$|V| = L \times \frac{di}{dt} \ [V]$$

For example, if a 2 A current flows for 10 ns in printed wiring with a parasitic inductance of 6 nH, then the following voltage occurs.

$$|V| = 6 \times 10^{-9} \times \frac{2}{10 \times 10^{-9}} = 1.2 \ [V]$$

Parasitic inductance can also cause large voltages, depending on the circumstances, and not only circuit operation can be affected, but components may be damaged or destroyed, so proper precautions must be taken.

<Summary>

- Understand the basic construction of a printed circuit board.
- The resistance of copper foil layers appears as a voltage drop, and is dependent on temperature.
- The inductance of copper foil layers can in some cases generate high voltages, so care should be exercised.
- Shortening wiring lengths is effective for reducing inductance.

2. PCB Layout Method and Examples of DC/DC Buck Converters

From this point, we explain specific component layout. The PCB layout of the example is based on the circuit used in the explanation of "1.2 Current Path of DC/DC Buck Converter in Operation" (see Figure 11). Please check the following example PCB layout with this circuit in mind.

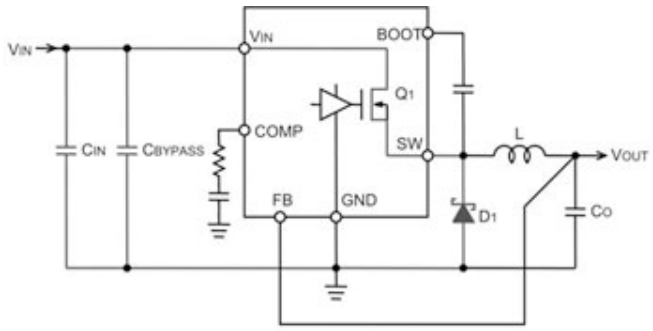


Figure 11. Example base circuit for PCB layout

2.1 Input Capacitors and Diodes

The first step in the layout is to place the most important components, the input capacitors and diodes.

According to "1.1 Main Principles of PCB Layout", "Place input capacitors and diodes on the same side as the IC pins and as close to the IC as possible". This is a very important point.

In the case of a power supply with a small output current ($I_O \leq 1$ A), the input capacitor will also have a small capacitance value, so it may be possible to combine C_{IN} and C_{BYPASS} with a single ceramic capacitor. This is because the ceramic capacitor has better frequency characteristics as the capacitance value becomes smaller. However, since the frequency characteristics vary depending on the type and brand, it is necessary to check the frequency characteristics of the capacitor actually used.

A large-capacitance capacitor used as C_{IN} will not generally have a particularly good frequency characteristic, as indicated below, and so a decoupling capacitor C_{BYPASS} with a good frequency characteristic must be arranged in parallel with C_{IN}. The combination of C_{IN} and C_{BYPASS} results in a frequency response that is a composite of the two capacitors; a surface-mount type multilayer ceramic capacitor (MLCC) should be used for C_{BYPASS}.

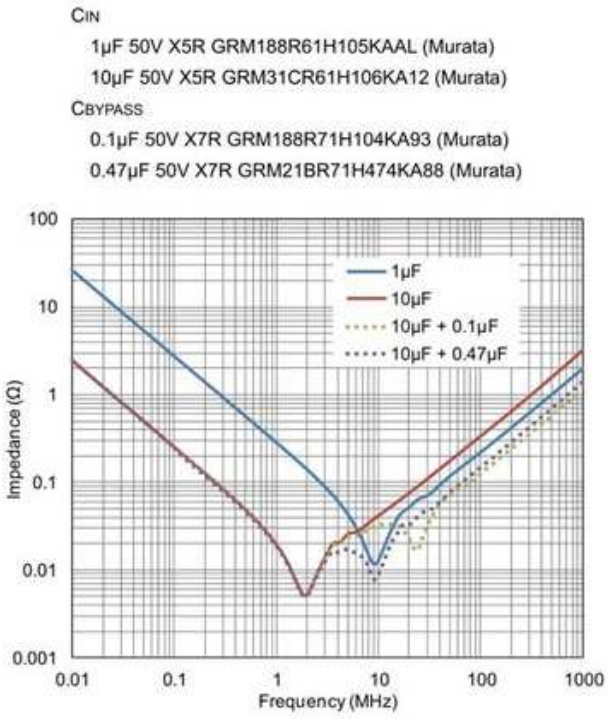


Figure 12. Comparison of frequency response between C_{IN} alone and C_{BYPASS} in combination

Well then, let us describe satisfactory and unsatisfactory examples while indicating the actual layout.

Figure 13 shows an example of a good layout for input capacitors.

C_{BYPASS} is positioned close to the IC pins, on the same board surface.

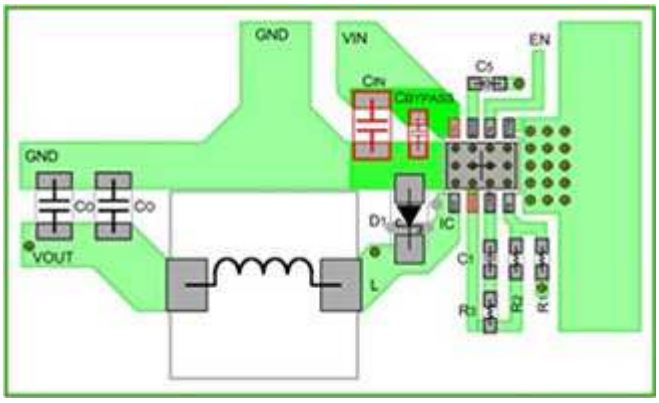


Figure 13. Example of a good layout for input capacitors

On the other hand, Figure 14 is an example in which a compromise is made. In contrast, Figure 14 is a compromise example: since the C_{BYPASS} is placed near the same side as the IC, it can supply most of the pulsed input current. Therefore, the large capacitor C_{IN} should not cause any problem even if it is as far away as 2 cm as shown in Figure 14, but as shown at the beginning, it should be "as close to the IC as possible".

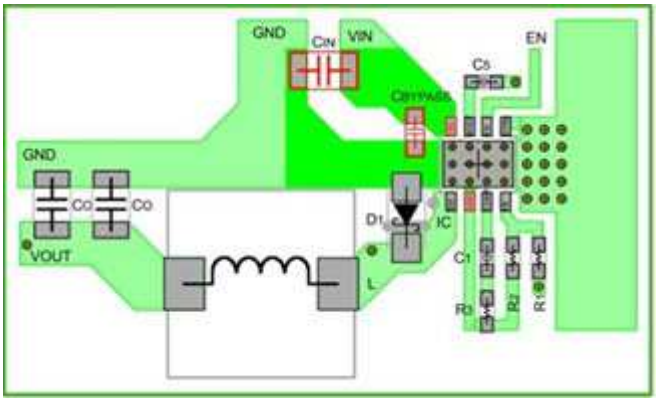


Figure 14. Example of compromise. if the C_{BYPASS} is placed near the same side as the IC, the C_{IN} can be as far as 2 cm away

If the C_{IN} cannot be placed on the same side as the IC due to space issues, it can be placed on the backside via as shown in Figure 15, provided that the C_{BYPASS} is correctly placed as per the requirements.

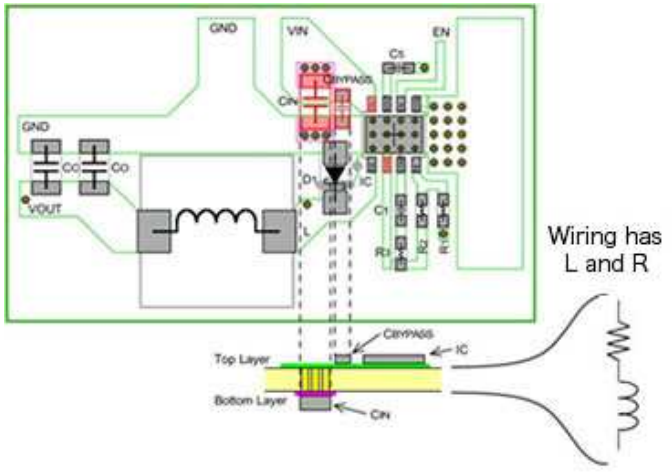


Figure 15. Example of C_{IN} placed on the backside through a via. There is a concern that the ripple voltage will increase

This method may avoid noise increase, but actual confirmation is required because the ripple voltage may increase at high current due to the via resistance.

The following Figure 16 shows the layout with C_{BYPASS} and C_{IN} placed on the backside.

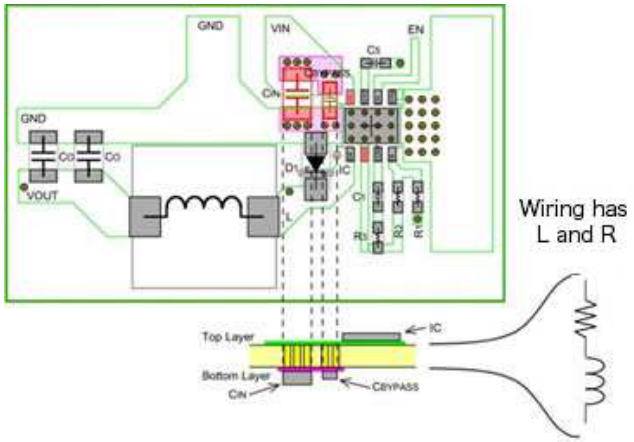


Figure 16. Example of C_{BYPASS} and C_{IN} placed on the backside. Via inductance increases noise

In this layout, the via inductance component causes an increase in voltage noise, and so **this kind of layout must never be used**.

Figure 17 shows a desirable layout for C_{BYPASS}, C_{IN} and the diode D_1.

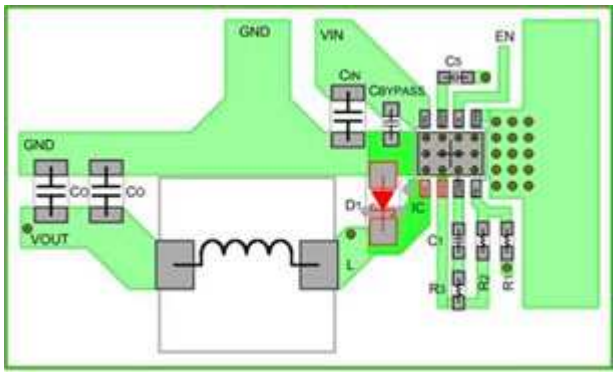


Figure 17: Example of a desirable input capacitors and diode arrangement

It is important that C_{BYPASS} be placed close to the V_{IN} pin and the GND pin of the IC.

However, in the case of a step-down converter, even if C_{BYPASS} is placed very close to the IC, high frequencies in the hundreds of megahertz range are present on the GND side of C_{IN}. For this reason, it is recommended that the ground of C_{IN} and the GND of the output capacitor C_O be separated by 1 to 2 cm.

The diode D_1 is also placed close to the IC pins on the same surface. The shortest and widest wiring must be used to connect the diode directly to the IC switch pin and the GND pin.

If vias are used to place components on the rear surface, the effect of the via inductance cases an increase in noise, and therefore **never take this approach**.

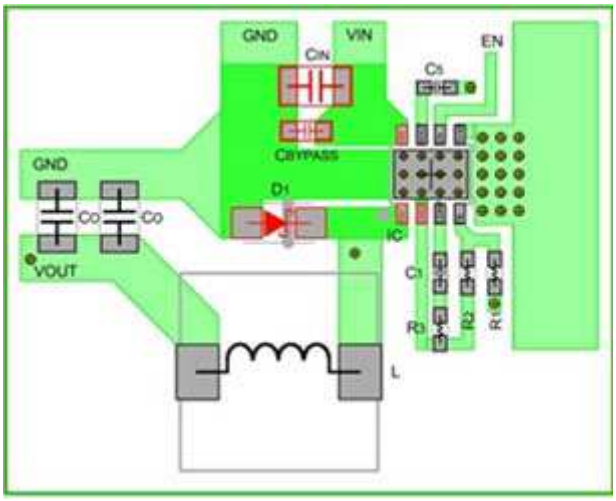
Figure 18 is an example of an unsatisfactory diode layout. Due to the distance between C_{BYPASS} and the V_{IN} and GND pins of the IC, voltage noise and ringing will occur due to the wiring inductance.

And the diode is distant from the IC switch pin and GND pin, and so the wiring inductance increases, spike noise becomes prominent.

Inappropriate placement of C_{BYPASS}, that is, not placing it in proximity, results in increased parasitic inductance due to the wiring length and/or vias. This can cause large ringing accompanying switching (Figure 19).

Moreover, the loop leading to the input capacitor functions as an antenna to radiate noise to the surroundings.

Waveforms of Figure 19 are for cases in which C_{BYPASS} is positioned 2 mm away and 10 mm away. The increase in ringing is clearly visible.



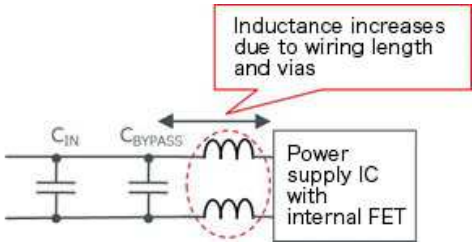


Figure 18. Unsatisfactory diode layout

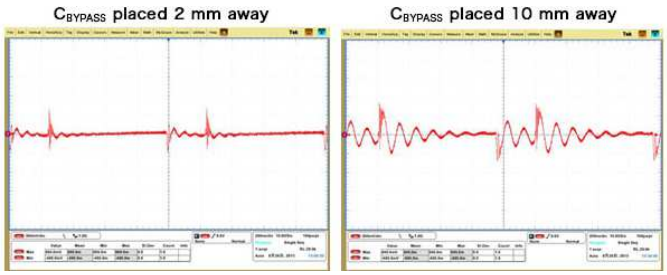


Figure 19. C_{BYPASS} distance and ringing

The effects of layout are very straightforward, and what you do is what you get. In the actual layout process, there will be times when you will have to make compromises, but try to keep them to a minimum and aim for the ideal layout.

<Summary>

- It is a good idea to begin with placement of the input capacitor and diode.
- As an inviolable rule, the input capacitor and diode must always be placed on the same surface as the IC pins, and as close to the IC as possible.
- Parasitic inductance is a cause of noise, and so use of vias should be studied carefully. Places where current is switched require careful attention.

2.2 Thermal Vias

Thermal vias are well known as a way to improve the heat dissipation effect of surface-mounted components using a substrate. However, without correct placement, they are not fully effective.

2.2.1 About Thermal Vias

Thermal vias are a method of increasing the area and volume used for heat dissipation, or in other words, lowering thermal resistance, by creating through holes in the substrate and connecting the copper foil on the surface and back of the substrate in the case of a single layer double-sided substrate.

Surface-mount components assume that by mounting on a PCB (printed circuit board), thermal resistance is reduced. Thermal resistance depends on the area and thickness of the copper foil on the PCB that serves to dissipate heat, as well as on the thickness and material of the board. In essence, the broader and thicker these materials, the greater is the effect in dissipating heat; but the thickness of the copper foil generally conforms to standard specifications, and cannot be made unreasonably thick. Moreover, given that space-saving continues to be a basic design requirement, the PCB area cannot be made as large as one would want, and the thickness of the actual copper foil cannot be described as very great either, so that when a certain area is exceeded, a heat-dissipating effect commensurate with the board area cannot be obtained.

One measure in answer to these issues is the use of thermal vias. In order to effectively use thermal vias, it is important that the thermal vias be located close to heating elements, for example, directly below components. As indicated in Figure 20, the effect of thermal equilibrium is utilized, and so it should be apparent that connecting areas with large temperature differences is a good plan.

The characteristics of thermal vias are summarized below.

- Heat from the heating element travels through the copper foil and dissipates.
- The larger the area, the lower the temperature rise.
- Thermal vias should be placed where there is a large temperature difference (directly under the heating element is preferable).
- Temperature reduction with thermal vias is determined by the area and volume.

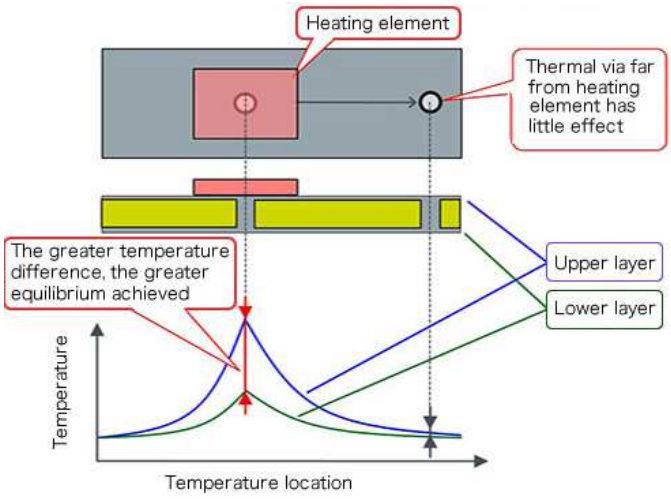
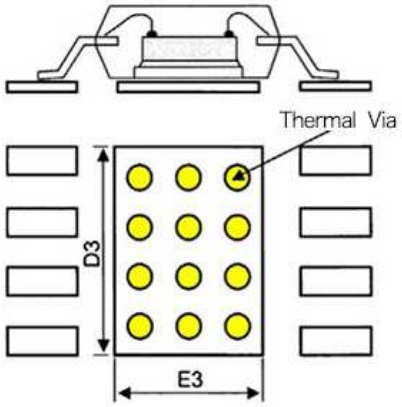


Figure 20. Thermal conduction by thermal vias

2.2.2 Placement of Thermal Vias

An example of a thermal via layout is shown below. Figure 21 is an example of the layout and dimensions of thermal vias for an HTSOP-J8 IC package, a package type in which a heat-dissipating plate is exposed on the bottom surface.

It is recommended that the thermal vias have a small inner diameter of approximately 0.3 mm for filling by plating, in order to heighten thermal conductivity. If the hole diameter is too large, problems with solder suction may occur during the reflow soldering process, so due caution is necessary.



Central land		Thermal via	
Length D3	Width E3	Pitch	Diameter
4.90mm	3.20mm	1.20mm	ϕ0.30

Figure 21. Example of thermal via dimensions and placement for back-sided heat dissipation package

With the interval between thermal vias set to about 1.2 mm, the vias are placed directly below the heat-dissipating plate on the bottom surface of the package. In cases where heat dissipation is insufficient using only vias directly below the bottom heat-dissipating plate, thermal vias are also placed on the periphery of the IC. In this case also, it is important that the vias be positioned as close to the IC as possible.

＜Summary＞

- Thermal vias are a means for causing heat to be conducted through a passage (hole) penetrating a circuit board to the opposite side, where it is dissipated.
- Thermal vias are placed directly below heating elements, or as close to them as possible.

2.3 Inductors

The layout of the inductor must be considered to minimize EMI. In addition, the characteristics of inductors as magnetic components must be well understood and used.

2.3.1 Inductor Characteristics Related to PCB Layout.

We begin with a brief review of the characteristics of inductors relating to PCB layout.

When a current flows in an inductor, magnetic lines of force are generated. When the magnetic lines of force pass through a conductor, such as the copper foil in a PCB, eddy currents are generated in that part of the conductor. That is, if there is an electrically conducting body near the inductor, problems may be caused by eddy currents in the body. The eddy currents flow in a direction so as to cancel the magnetic lines of force, and so the inductance is reduced, and the Q factor falls (losses are increased). Incidentally, Q is one of the parameters that expresses the amount of loss in an inductor, and simply means that "higher Q = less loss". Otherwise, if the copper foil near the inductor is a signal line, eddy currents may cause noise to propagate to the signal, which may adversely affect the circuit operation.

There is another issue to consider as well: an inductor is a component that generates heat. When a current flows in an inductor, heat is generated by the resistive component of the windings and by other losses. When an inductor reaches a high temperature, its parts may be degraded, and it is well known that when a ferrite core is used, if the Curie temperature is exceeded, the inductance will drop sharply. Current ratings and resistance values are indicated in the specifications as guidelines, and in actual implementation, the problem of heat dissipation must be carefully considered.

2.3.2 Placement of Inductors

Although not as important as in the case of an input capacitor, an inductor should be placed as close as possible to the IC in order to minimize radiation noise from the switching node.

If the copper foil area is made too broad in order to reduce wiring resistance and dissipate heat, the copper foil may act as an antenna, which increases EMI, and so the area of the copper foil should not be made any larger than is necessary.

Figure 22 shows a desirable layout designed with the wiring area set considering the effect on EMI, and Figure 23 shows an undesirable layout designed with the wiring area set larger than is necessary.

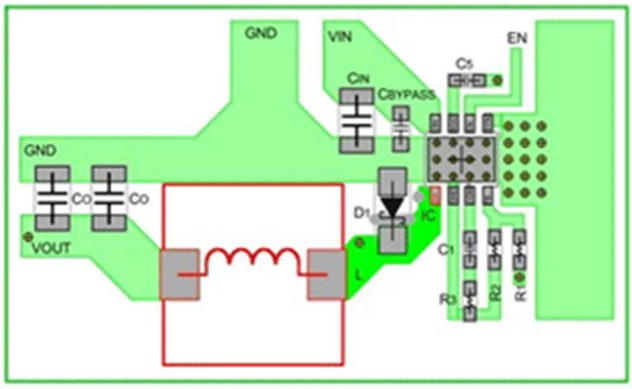


Figure 22. Desired inductor wiring example

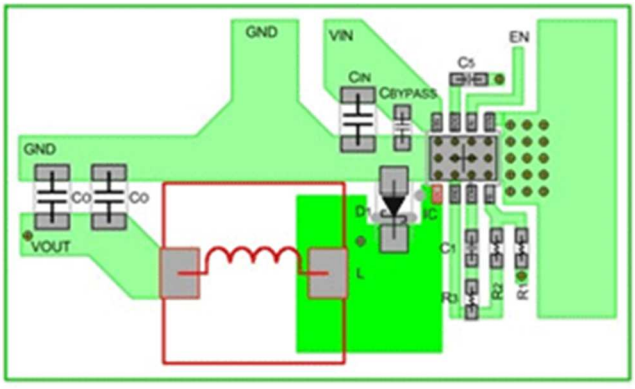


Figure 23. Undesirable wiring example of an inductor that takes up a larger copper foil area than necessary

Current resistance can be used as a guide when deciding on the specific wiring width. Figures 24 and 25 are graphs showing the conductor width and the rise in temperature due to self- heating when a certain current is passed.

For example, when a 2 A current is passed in wiring with a conductor thickness of 35 µm, a conductor width of 0.53 mm is sufficient in order to hold the rise in temperature to no more than 20°C. However, the wiring is affected by heat generated by peripheral components and by the ambient temperature, and so a sufficient margin must be included. For example, for a one-ounce (35 µm) board, a width of 1 mm or greater is recommended, and for a two-ounce (70 µm) board the recommended width is at least 0.7 mm.

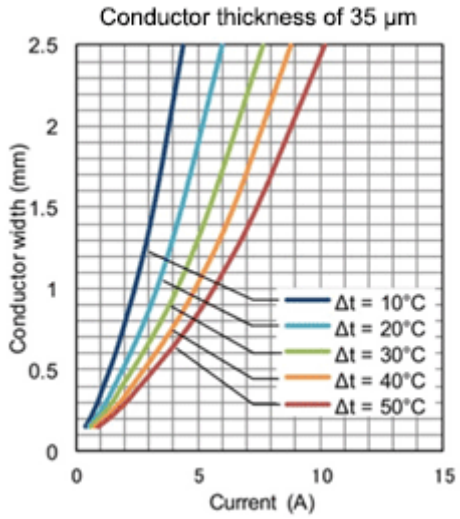


Figure 24. Temperature rise due to 35 µm conductor thickness, width and current

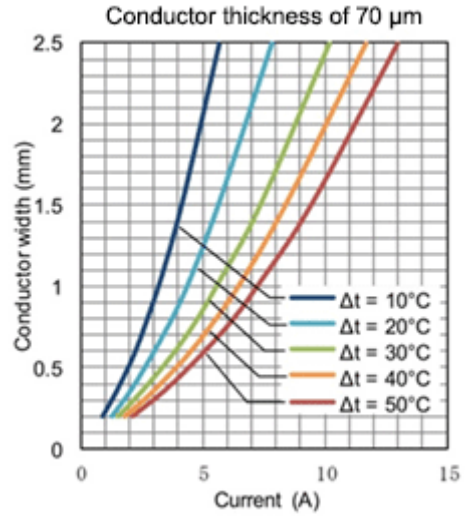


Figure 25. Temperature rise due to 70 µm conductor thickness, width and current

Where wiring in the vicinity of an inductor is concerned, no GND and other wiring can be placed immediately below the inductor (Figure 26). As explained above, this is because magnetic lines of force would pass through the GND layer, which is a conductor, causing eddy currents, and the effect of canceling the magnetic lines of force would cause the inductance to fall and the Q factor to drop (losses would increase).

Signal lines other than GND should likewise not be placed directly below an inductor, because of the possibility of eddy currents causing switching noise to propagate in signals. In a case where a signal line must pass directly below an inductor, the inductor should be a component with a closed magnetic circuit structure, so that leakage of magnetic force lines is minimal. However, actual measurements must always be performed to ensure that no problems occur.

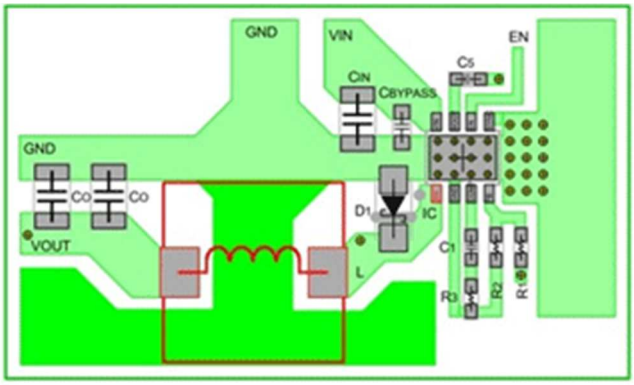


Figure 26. Example of undesirable wiring directly below an inductor

Moreover, attention must also be paid to the spaces between wiring of inductor terminals. If the distance between the wiring of the terminals is short, as in Figure 27, high-frequency signals of the switching node may be induced in the output via stray capacitance.

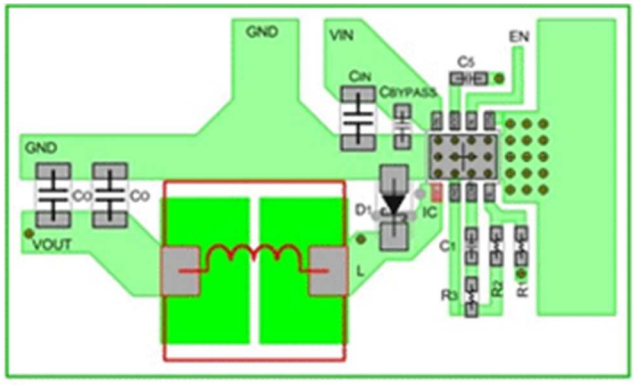


Figure 27. Example of undesirable wiring across terminals of an inductor

<Summary>
- Inductors should be placed as close to ICs as possible.
- Copper foil areas of inductor wiring should not be made broader than is necessary.
- Do not place the GND layer directly below an inductor. Signal lines should also be placed so as not to run under an inductor.
- Do not cause the wiring of inductor pins to approach each other.

2.4 Output Capacitors

The output capacitor, like the input capacitor, is an essential capacitor in a DC/DC buck converter and affects the smoothing, stabilization, and ripple voltage of the output.

2.4.1 Difference Between Output and Input Capacitor Current

We begin now by recalling that there are differences in the currents flowing in an input capacitor C_{IN} and in an output capacitor C_O. In Figure 28, I_{CO} is the current waveform for an output capacitor, and I_{CIN} below it is that for an input capacitor.

In the input capacitor, a comparatively large current repeatedly flows suddenly, but in the output capacitor, smooth charging and discharging is repeated, linked with an output ripple voltage and centered on the output voltage. This is because an inductor is inserted in series into the output line; the inductor L and C_O serve as an output filter.

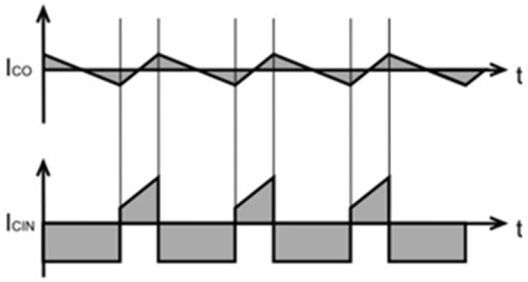


Figure 28. Example of current waveforms for output capacitor (top) and input capacitor (bottom)

2.4.3 Placement of the Output Capacitor

The GND connection of the capacitor C_O should be at a position 1 to 2 cm distant from the GND connection of C_{IN}, and as close to the inductor as possible (Figure 29).

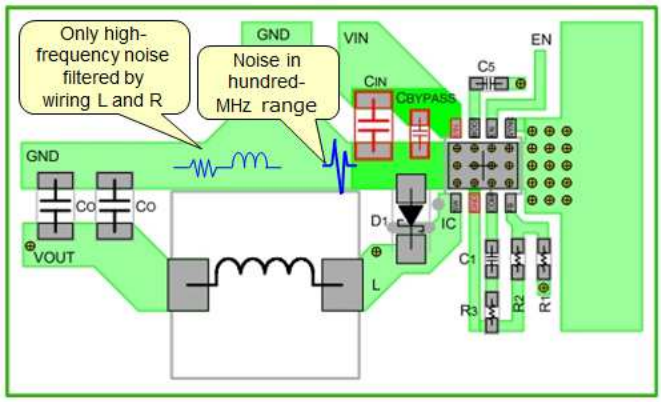


Figure 29. Example of output capacitor C_O placement

As stated above, in the input capacitor, a sharply rising/falling current flows repeatedly, and so a high frequency in the range of several hundred MHz flow into the GND pattern connected to C_{IN}. Of course, the GND pattern to which C_O is connected is the same GND pattern, and so if C_O is placed close to where C_{IN} is connected, there is the possibility that the high-frequency noise in the input may pass through C_O and be conducted to the output. This is shown schematically in Figure 30.

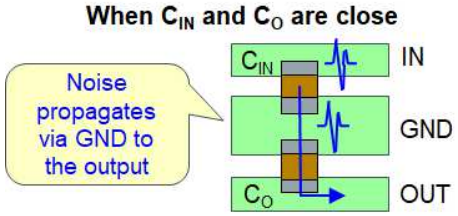


Figure 30. Noise is transmitted through GND when C_{IN} and C_O are close

The reason for separating the GND of C_O from the GND of C_{IN} by 1 to 2 cm is that the inductance and resistance components of the thin film wiring can serve as a filter to reduce high-frequency noise. In other words, this design makes clever use of parasitic components.

<Summary>
- An output capacitor should be placed as close as possible to an inductor.
- In order to reduce the propagation of high-frequency noise, the GND of C_{IN} should be placed 1 to 2 cm distant from the GND of C_O.

2.5 Feedback Path

The feedback path is a path for returning the output voltage to the FB pin of the power supply IC in order to regulate the output. The wiring of the feedback path

requires special attention among the signal wiring.

As the circuit diagram in Figure 31 shows, the output voltage is divided by resistors through the wiring and is returned to the FB pin of the power supply IC = input of the error amplifier. The power supply IC uses this voltage information to regulate the output voltage. The reason why this feedback path is so important is that if noise or fluctuations other than the actual output voltage are sent to the error amplifier, not only will accurate output regulation not be possible, but depending on the conditions, oscillation and other unstable operations may occur. For this reason, care must be taken to ensure that the feedback path returns a clean signal.

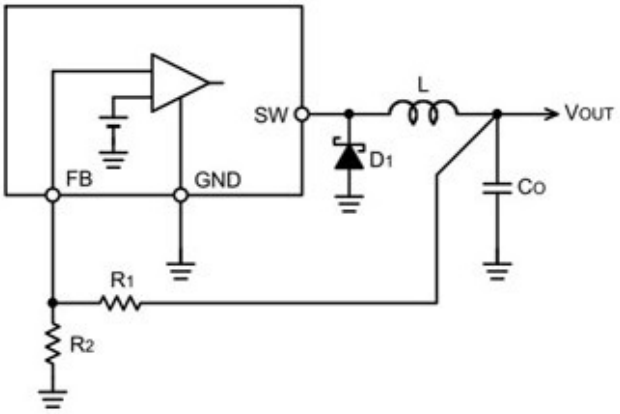


Figure 31. Feedback path (V_{OUT}→R_1/R_2→FB)

The following precautions should be taken when wiring the return path (see Figure 32).

- When feedback signal wiring picks up noise, an error occurs in the output voltage, and in some cases operation becomes unstable.
- The FB pin of the IC, to which the feedback signal is input, has high impedance, and so this pin should be connected to the voltage division node of a resistive voltage-dividing circuit using wiring that is as short as possible: see (a) in Figure 32.
- The place for detecting the output voltage should be either across the terminals of the output capacitor, or past the output capacitor: see (b) in Figure 32.
- Lines from the output to a resistive voltage divider should be parallel and close to each other so as not to easily pick up noise: see (c) in Figure 32.
- Wiring should be laid out far from the switching nodes of inductors and diodes: see (d) in Figure 32.
- Wiring should not be placed immediately below an inductor or diode, or in parallel with wiring of a power switch system (even in multilayer boards).

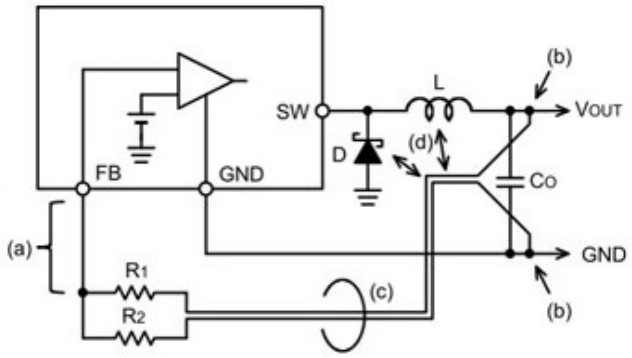


Figure 32. Notes on feedback path wiring

An example of wiring laid out with these points in mind is shown below. Figure 33 is an example of a layout where the wiring is moved to the backside to the feedback path through a via and away from the switching node.

As you can see from the layout, it is not so easy to find a routing that can perfectly clear the above conditions. Although it was not specifically included in the above notes, the basic rule for wiring is "as short as possible". Therefore, it is not a good idea to make the feedback wiring unnecessarily long and separate it from the circuit area. Figure 33 shows an example of how to deal with this problem by expanding the feedback signal wiring to the back side.

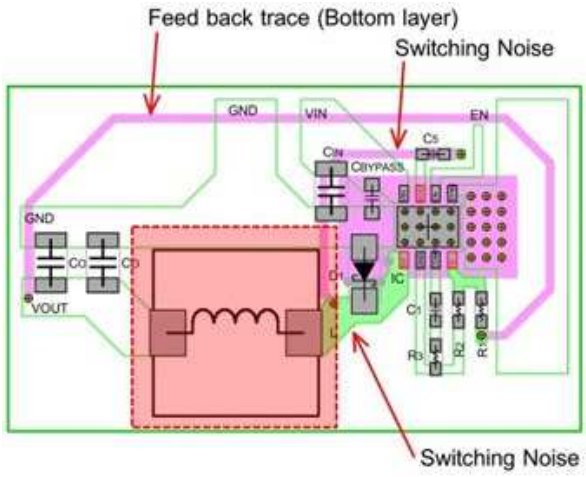


Figure 33. Example layout of the feedback path. Wiring through the back side

Figure 34 is an example of unsuitable wiring. The feedback path is laid out parallel to the inductor, and so the magnetic field generated near the inductor induces noise in the feedback path.

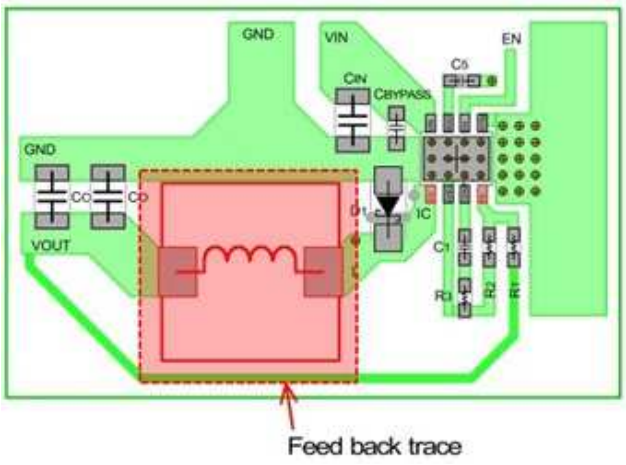


Figure 34. Unsuitable feedback path layout. Wiring beside Inductor

In actuality, due to relationships with other components, there are cases in which the ideal layout and wiring cannot be realized. In such cases, it will be necessary to consider what exactly is the essence of ideal wiring, and to find a compromise that strikes the best possible balance between competing factors.

＜Summary＞

- A feedback signal line from the output should be laid out away from the switching nodes. If the line picks up noise, errors and erroneous operation will result.
- Placing wiring on the bottom layer of the board through a via is another option.

2.6 Ground

Since ground wiring is necessary for each of many components, its layout needs to be carefully considered. In the DC/DC buck converter circuit, it has been explained in each section that it is important to separate the signal system, such as the output voltage feedback leading to the control circuit, and the power system, which switches a large current, and the same applies to the ground wiring.

2.6.1 Analog Small-Signal Ground and Power Ground

Ground potential is the same potential everywhere in the PCB; but in a circuit in which analog signals and digital signals coexist (which, of late, is the case for nearly all circuits), an analog ground and a digital ground are provided separately, and measures are adopted such that noise arising from digital signals is not conducted so as to interfere with minute analog signals. This is the same approach taken in switching power supply circuits. For example, care must be taken to ensure that noise generated at switching nodes has as little effect as possible on feedback paths the line voltage of which directly affects the output precision.

There are a number of terms used, but here, we will refer to a ground used for lines that are susceptible to noise, such as feedback paths, as an analog small-signal ground (AGND), and will use "power ground" (PGND) for a ground that is used for lines that switch large currents, such as a switching nodes.

As the most important issue, AGND and PGND must be separated. They are at the same potential, and ultimately they are connected, but the reasoning is that the ground to which large currents return as a result of switching and the ground for control signals must be separated in order to prevent interference.

Next, PGND is essentially laid out as a single line on the top layer (Figure 35). However, as a result of component arrangement and the like, there are cases in which a single continuous line is not possible. In such cases, PGND may be broken up and connected on the rear surface or by an internal layer, using vias (Figure 36). However, due to the influence of resistance and inductance of the vias, there may be increased losses and the noise level may be worsened, and so actual device should be used for thorough verification.

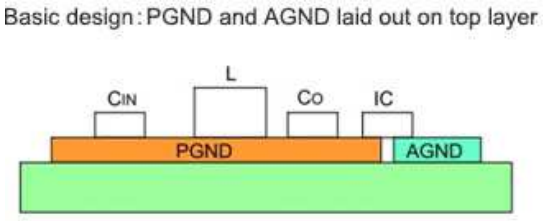


Figure 35. Basic GND layout example

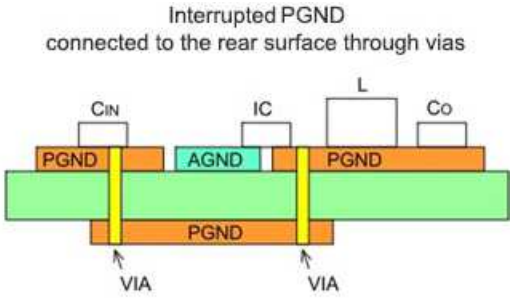


Figure 36. Example of connecting PGND through a via. Noise and loss need to be verified

<Summary>
- AGND and PGND must be separated.
- The basic procedure is to arrange the PGND on the top layer without interruption.
- If the PGND is interrupted and connected on the rear surface using vias, the resistance and inductors of the vias may worsen the loss and noise, so verification is necessary.

2.2.6 Ground Plane

A ground plane is a ground wiring with a certain area, but the purpose of having a ground plane on the backside or inner layer is basically to reduce DC loss, shield, and dissipate heat, and as a ground plane, it is only a supplementary role.

When a ground wiring is provided in an inner layer or on the rear surface of a multilayer board, consideration must be paid to inputs with substantial high-frequency switching noise and to connection of diodes to PGND. As in Figure 37, when there is a common ground in the third layer and a signal ground in the fourth layer, connections of these grounds to PGND should be made close to an output capacitor C_O with little high-frequency switching noise. PGND connections must not be made near the noisy input capacitor C_{IN} or diode D.

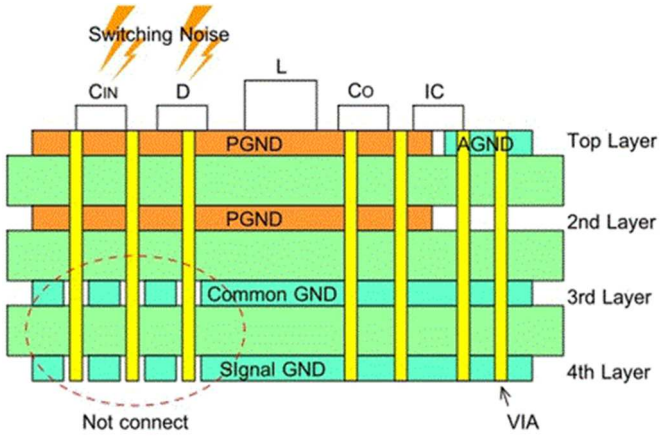


Figure 37. Connection example of PGND and signal GND on a multilayer board and points to note

When there is a PGND plane for DC loss alleviation in the second layer, the top layer PGND and the second layer must be connected by numerous vias, to reduce the PGND impedance.

<Summary>
- When placing ground planes in inner layers or on the rear surface of a multilayer board, care must be taken in connecting the PGND to diodes and inputs with substantial high-frequency switching noise.
- The top layer PGND and inner layer PGND are connected using numerous vias, to reduce impedance and alleviate DC losses.
- Connections of PGND to a common ground or a signal ground are made near an output capacitor with little high-frequency switching noise; PGND connections must not be made near the noisy input capacitor or diode.

By the way, do you know that many DC/DC converter ICs have two GND pins, AGND (SGND) and PGND? This is because, for entirely the same reasons, the signal system and the switching (power) system are kept separate within the IC as well. And the two must similarly be at the same potential, and so ultimately they are connected. It is important that the AGND and the PGND of an IC be connected at a single point. To determine the optimum point for connection, the layout information of the data sheet and other resources should be consulted.

3. Noise Countermeasures in PCB Layout

As we have discussed so far, in switching power supply circuits, it is necessary to minimize noise and ensure stable and clean operation, and at the same time, consider EMI to minimize the impact on other devices in the board layout.

In addition to basic component placement and wiring, there are several other noise countermeasures related to board layout.

3.1 Corner Wiring

Thin-film wiring inevitably requires corners (bends), but the way they are bent can cause EMI to deteriorate. If you have no experience in board layout, you may think this is impossible, but this is one know-how.

Figure 38 illustrates better and worse methods of corner wiring. If the wiring is bent at a right angle in a corner, the impedance changes at the corner. This causes disruption of the current waveform, and waveform disruption known as reflection occurs. In wiring that passes high frequencies, such as at switching nodes, reflection can worsen the circuit EMI.

Figure 38. Corner wiring layout, good and bad

Preferred methods of bending the wiring include using 45-degree bends and arcs instead of right angles. The larger the radius of curvature of a bend, the smaller is the change in impedance.

3.2 Noise Terminal Voltage (conducted emissions)

The noise terminal voltage is noise that is fed back to the input line, and is also called conducted emission noise. The noise bands mainly appear at multiples of the oscillation frequency.

This noise can be suppressed by inserting a ferrite bead or a π filter. Such noise suppression components must be selected to match the noise band to be reduced. Hence the noise must first be confirmed, and the frequency determined. Figure 39 is an example of measured data for the noise terminal voltage.

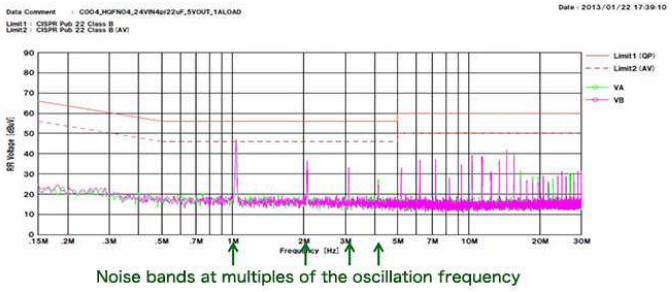


Figure 39. Example of measured data of noise terminal voltage

3.3 Noise Electric Field Intensity (radiated noise)

Another noise type that must be studied is noise electric field intensity (radiated noise). The radiated noise of DC/DC converters is caused by the slope and ringing of the switch on and off waveforms, with a bandwidth of roughly 100MHz to 300MHz.

Ringing during switching signal rising and falling mainly arises from the wiring inductance between a MOSFET and the input capacitor; the magnitude of the inductance affects the noise.

As explained earlier in the discussion of input capacitor placement, by optimizing the input capacitor placement and wiring, the noise level can be reduced.

Measures that can be taken when radiated noise in a DC/DC converter circuit has exceeded a standard that must be met by the equipment in which the converter will be installed include using a more gradual switching waveform, and adding a snubber circuit.

Figure 40 shows an example of measured radiated noise. The noise level limit is shown by the red line, and in this example, the region just below 200MHz shows a slightly severe result.

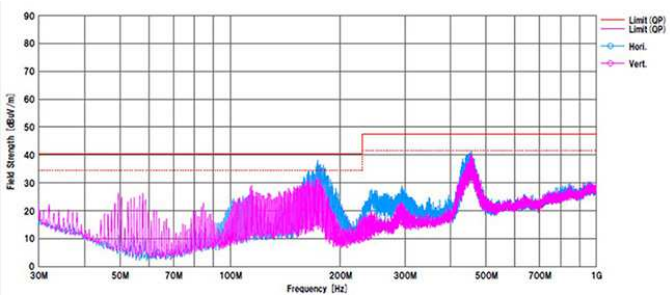


Figure 40. Example of measured data for radiated noise

3.4 Addition of a Snubber Circuit

This section describes one of the countermeasures described in "3.3 Noise Electric Field Intensity (radiated noise)", namely "adding a snubber circuit".

The addition of a snubber circuit is a technique often used to reduce noise. In case of noise reduction in switching node, snubber circuit is added to the output, but for input noise, it is added to the input. In this example, adding an RC to the switching node absorbs the ringing by having the resistor consume the high frequency energy of the ringing caused by switching (see Figure 41).

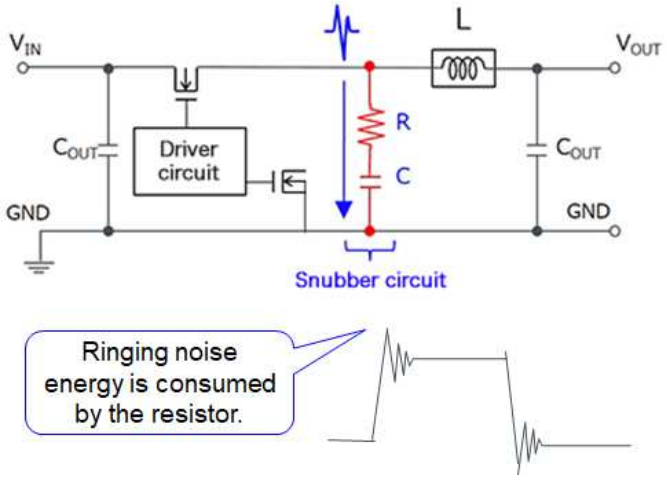


Figure 41. Example of snubber circuit and operation

However, losses may occur depending on the snubber circuit added. If the capacitance of the capacitor is increased to enhance effectiveness, the resistor must be able to handle the power. Below is an example of calculation of snubber losses.

Example of calculation of snubber losses：

Snubber resistor：10Ω
Snubber capacitor：1000pF
V_{IN}：12V

Allowable loss of resistance at oscillation frequency of 1MHz is：

Snubber loss $P = C \times V^2 \times f_{SW}$

1000pF×122×1MHz＝0.144W

* A resistor rated power of MCR18 (3216): 0.25W or higher is necessary

＜Summary＞

- Snubber circuits consume high-frequency energy with the resistor.
- Since snubber loss occurs, pay attention to the allowable loss of the resistor.
- The effect of the snubber circuit is a trade-off with the loss.

3.5 Noise Suppression for Bootstrap Circuits

This is followed by another countermeasure mentioned in "3.3 Noise Electric Field Intensity (radiated noise)": how to slow down the switching waveform. There is one more approach to this, and it will be explained in the next section.

ICs that use Nch MOSFETs as high-side switches often have a BOOT pin. This is a function that feeds the output voltage to a bootstrap circuit to provide sufficient gate drive voltage to the high-side MOSFET.

Since the BOOT pin is connected to the switching node, inserting a resistor here can slow down the rise time when the high-side MOSFET is turned on, thus mitigating the noise at switch-on. The disadvantage is that the switching time becomes slower, so the switching loss of the MOSFET increases (see Figure 42).

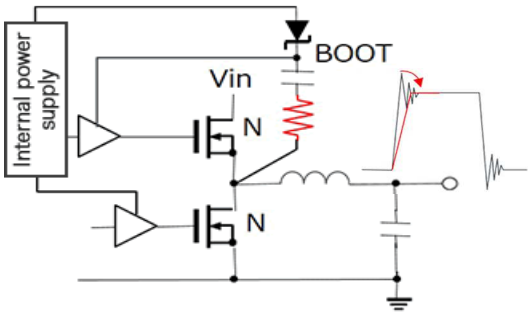


Figure 42. Example of inserting a resistor into a bootstrap circuit

＜Summary＞

- By inserting a resistor to the BOOT pin, the slope of the rising waveform when the high-side MOSFET is turned on can be made gentle to reduce noise.
- Note that the switching loss of the MOSFET will increase.

3.6 Noise Suppression of High-side MOSFET

This is also one of the countermeasures described in "3.3 Noise Electric Field Intensity (radiated noise)", "How to slow down the switching waveform".

This method limits the gate charge by inserting a resistor between the gate driver and the gate of the high-side MOSFET to make both the rise and fall of the high-side MOSFET gentle, thereby reducing noise both on and off (see Figure 43).

The disadvantage is that the switching loss of the MOSFET increases, as does the addition of a bootstrap resistor. Also, this method cannot be used for ICs with built-in switches. This method can only be used in a configuration with a controller IC where the switching is external.

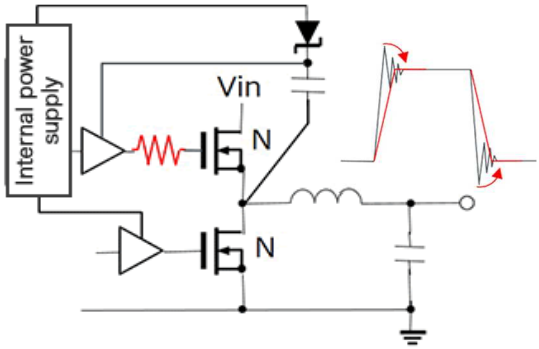


Figure 43. Example of inserting a gate resistor into an external high-side MOSFET

＜Summary＞

- A resistor can be inserted into the gate of the high-side MOSFET to reduce noise by making both on/off slopes milder.
- Note that the switching loss of the MOSFET will increase.
- This countermeasure is not available for ICs with built-in MOSFETs because a resistor cannot be inserted.

4. Conclusion

We have explained the key points regarding the layout of a mounting board for a DC/DC buck converter. The details are explained in each section, but the basics are the seven items described in "1.1 Main principles of PCB layout". The most important thing to keep in mind is to keep the wiring as short as possible.

If you are faced with a problem where the circuit you have designed is correct and the components are in good condition, but when you mount it on the PCB, it does not perform as expected, or worse, it does not work, you should first check if the PCB layout is correct. There are really not a few cases like this.

Above all, it is of utmost importance to minimize rework and redesign from circuit design to board design, prototyping, and mass production. What we need to do is to improve the quality of the design, including the board design.

In actual board layout, there are often restrictions on component placement and wiring routing. However, it is especially important to incorporate the points that should be pressed into the layout design. If the design deviates from the ideal, it is always necessary to take actual measurements to check for problems. In a sense, PCB layout design is a design that requires expanding the image in three dimensions, with multilayer boards and electromagnetic waves. In order to broaden the image, it is important to accumulate the actual design and measurement work.

Revision History

Date	Version	Details
2021.04.22	001	Initial version

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