I/O Ports with Interrupt-on-Change (IOC)

HIGHLIGHTS

This section of the manual contains the following topics:

dsPIC33/PIC24 Family Reference Manual

> **Note:** This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all dsPIC33/PIC24 devices.
>
> Please consult the notes at the beginning of each chapter in the current device data sheet to check whether this document supports the device you are using.
>
> Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com.

1.0 INTRODUCTION

The general purpose I/O pins are the simplest of peripherals. They allow the PIC® MCU to monitor and control other devices. To add flexibility and functionality to a device, some pins are multiplexed with alternate functions and these functions depend on which peripheral features are on the device. In general, when a peripheral is functioning, that multiplexed I/O pin may not be used as a general purpose I/O pin. Many 16-bit devices support the Peripheral Pin Select (PPS) feature. The PPS feature enables users to map certain peripheral functions to a PPS-enabled I/O pin. Each general purpose I/O pin also provides Interrupt-on-Change (IOC) functionality that can notify the user of a change in that Pin's state.

Figure 1-1 shows a block diagram of a typical I/O port. The block diagram does not take into account the peripheral functions that may be multiplexed onto the I/O pin.

Figure 1-1:   Dedicated Port Structure Block Diagram
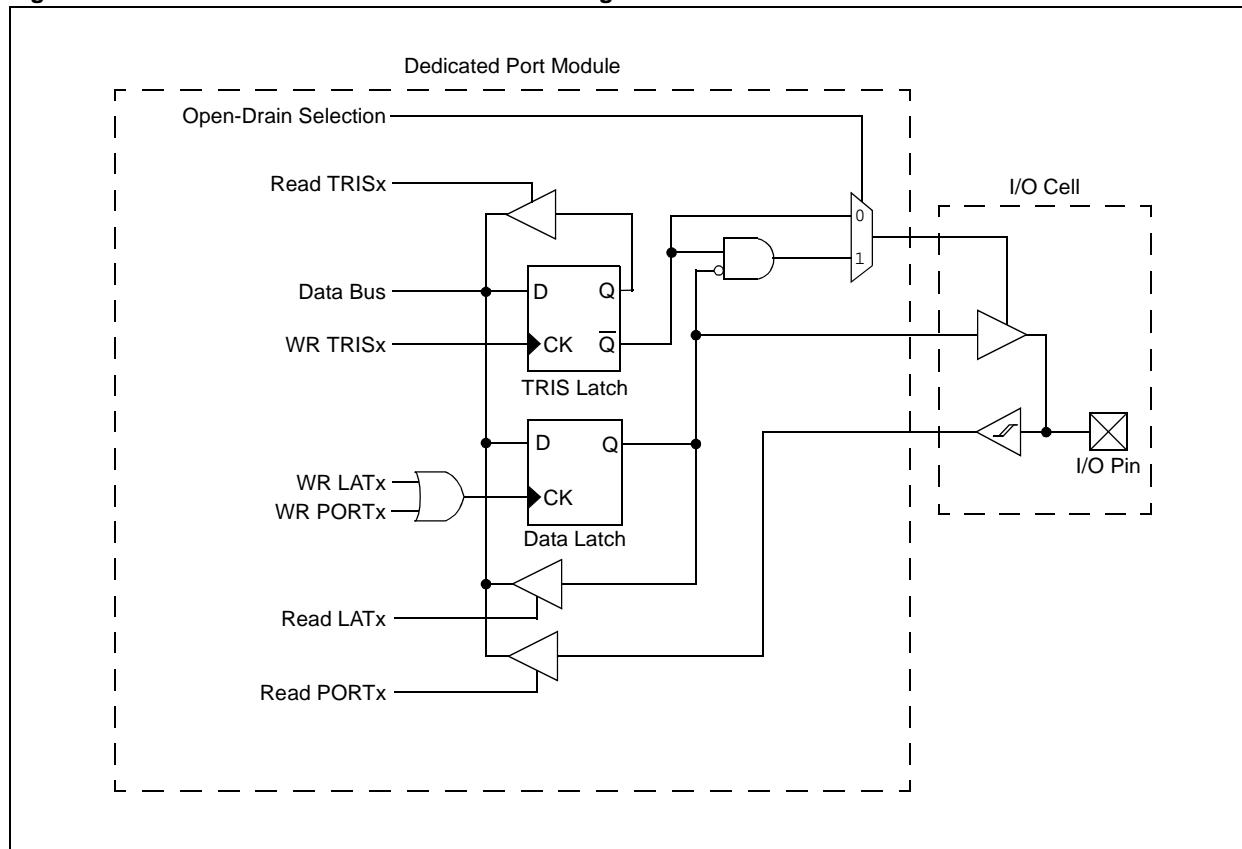
2.0   I/O PORT CONTROL REGISTERS

All I/O ports have up to twelve registers directly associated with the operation of the port. Each I/O pin on the device has an associated bit in each control register. In addition to the per pin control registers, there are two registers that control global I/O functionality. The Pad Configuration register (PADCON) contains a control bit that enables the Interrupt-on-Change (IOC) functionality. The PADCON register may also control other device-specific I/O functionality.

An IOC event occurs on any I/O pin. When an event occurs, the corresponding bit in the IOCxF flag register will be set, where 'x' is the port. The Interrupt-on-Change Status (IOCSTAT) register contains bits that represent the IOC status of entire ports. If an IOCxF register indicates an IOC event on any of the pins on a port, the corresponding bit for that port will be set in the IOCSTAT register.

> **Note:** The total number of ports and available I/O pins will depend on the device variant. In a given device, all bits in a PORTx register may not be implemented. For more information, refer to the specific device data sheet.

Register 2-1:   PADCON: Pad Configuration Register

R/W-0	U-0	U-0	U-0[1]	U-0[1]	U-0[1]	U-0[1]	U-0[1]
IOCON	—	—	—	—	—	—	—

bit 15   bit 8

U-0[1]	U-0[1]	U-0[1]	U-0[1]	U-0[1]	U-0[1]	U-0[1]	U-0[1]
—	—	—	—	—	—	—	—

bit 7   bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 15   **IOCON:** Interrupt-on-Change (IOC) Enable bit

1 = Interrupt-on-Change functionality is enabled
0 = Interrupt-on-Change functionality is disabled

bit 14-0   **Unimplemented:** Read as '0'

Note 1:   Refer to the specific device data sheet for implementation details.

Register 2-2: IOCSTAT: Interrupt-on-Change Status Register

U-0	U-0	U-0	U-0	U-0	U-0	R/HS/HC-0	R/HS/HC-0
—	—	—	—	—	—	IOCPJF[1]	IOCPIF[1]
bit 15							bit 8

R/HS/HC-0	R/HS/HC-0	R/HS/HC-0	R/HS/HC-0	R/HS/HC-0	R/HS/HC-0	R/HS/HC-0	R/HS/HC-0
IOCPHF[1]	IOCPGF[1]	IOCPFF[1]	IOCPEF[1]	IOCPDF[1]	IOCPCF[1]	IOCPBF[1]	IOCPAF[1]
bit 7							bit 0

Legend:		HS = Hardware Settable bit	HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **IOCPJF:IOCPAF:** Interrupt-on-Change (IOC) Status bits[1]

1 = An IOC event was detected on an IOC-enabled pin on the PORTx register; this bit is set when any bit in the IOCFx register is set and this bit is cleared when every bit in the IOCFx register is cleared
0 = No event was detected or all detected events on the PORTx register have been cleared

Note 1: Refer to the specific device data sheet for implementation details.

I/O Ports with Interrupt-on-Change (IOC)

2.1   General Purpose I/O Control Registers

The following general purpose I/O Control registers control the general I/O functionality:

- **TRISx: PORTx Data Direction Control Register**
- **PORTx: I/O PORTx Register**
- **LATx: PORTx Data Latch Register**
- **ODCx: PORTx Open-Drain Control Register**
- **ANSx: Analog Function x Select Register**

Register 2-3:   TRISx: PORTx Data Direction Control Register

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TRISx<15:8>[1]							
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TRISx<7:0>[1]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0   **TRISx<15:0>:** PORTx Data Direction Control bits[1]

　　　　　　1 = The pin is an input
　　　　　　0 = The pin is an output

Note 1:   Refer to the specific device data sheet for the implementation details.

Register 2-4:   PORTx: I/O PORTx Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PORTx<15:8>[1]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PORTx<7:0>[1]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0   **PORTx<15:0>:** I/O Portx bits[1]

　　　　　　1 = The pin data is '1'
　　　　　　0 = The pin data is '0'

Note 1:   Refer to the specific device data sheet for the implementation details.

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Register 2-5:   LATx: PORTx Data Latch Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			LATx<15:8>[1]				
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			LATx<7:0>[1]				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0   **LATx<15:0>:** PORTx Data Latch bits[1]

        1 = The latch content is '1'
        0 = The latch content is '0'

Note 1: Refer to the specific device data sheet for the implementation details.

Register 2-6:   ODCx: PORTx Open-Drain Control Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			ODCx<15:8>[1]				
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			ODCx<7:0>[1]				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0   **ODCx<15:0>:** PORTx Open-Drain Control bits[1]

        1 = The pin acts as an open-drain output pin if TRISx is '0'
        0 = The pin acts as a normal pin

Note 1: Refer to the specific device data sheet for the implementation details.

Register 2-7: **ANSx: Analog Function x Select Register**

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
ANSx<15:8>[1]							
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
ANSx<7:0>[1]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0　　**ANSx<15:0>:** Analog Function x Select bits[1]

　　　　1 = Pin is configured in Analog mode and I/O port operation is disabled; reads from any bit, where ANSx<n> = 1, will read as '0'
　　　　0 = Pin is configured in Digital mode and I/O port operation is enabled

Note 1: Refer to the specific device data sheet for the implementation details.

2.2 Interrupt-on-Change Control Registers

The following IOC Control registers control the Interrupt-on-Change functionality.

- **IOCPx: Interrupt-on-Change x Positive Edge Enable Register**
- **IOCNx: Interrupt-on-Change x Negative Edge Enable Register**
- **IOCFx: Interrupt-on-Change x Flag Register**
- **IOCPUx: Interrupt-on-Change x Pull-up Enable Register**
- **IOCPDx: Interrupt-on-Change x Pull-Down Enable Register**

Register 2-8:   IOCPx: Interrupt-on-Change x Positive Edge Enable Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IOCPx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IOCPx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0   **IOCPx<15:0>:** Interrupt-on-Change x Positive Edge Enable bits
1 = Interrupt-on-Change is enabled on the corresponding pin for a low-to-high transition
0 = Interrupt-on-Change is disabled on the corresponding pin for a low-to-high transition

Register 2-9:   IOCNx: Interrupt-on-Change x Negative Edge Enable Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IOCNx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IOCNx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0   **IOCNx<15:0>:** Interrupt-on-Change x Negative Edge Enable bits
1 = Interrupt-on-Change is enabled on the corresponding pin for a high-to-low transition
0 = Interrupt-on-Change is disabled on the corresponding pin for a high-to-low transition

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Register 2-10:   IOCFx: Interrupt-on-Change x Flag Register

R/C/HS-0	R/C/HS-0	R/C/HS-0	R/C/HS-0	R/C/HS-0	R/C/HS-0	R/C/HS-0	R/C/HS-0
			IOCFx<15:8>				
bit 15							bit 8

R/C/HS-0	R/C/HS-0	R/C/HS-0	R/C/HS-0	R/C/HS-0	R/C/HS-0	R/C/HS-0	R/C/HS-0
			IOCFx<7:0>				
bit 7							bit 0

Legend:		C = Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15-0   **IOCFx<15:0>:** Interrupt-on-Change x Flag bits
> 1 = An Interrupt-on-Change event was detected on the corresponding pin
> 0 = An Interrupt-on-Change event was not detected or a detected change has been cleared

Register 2-11:   IOCPUx: Interrupt-on-Change x Pull-up Enable Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			IOCPUx<15:8>[1]				
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			IOCPUx<7:0>[1]				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0   **IOCPUx<15:0>:** Interrupt-on-Change x Pull-up Enable bits[1]
> 1 = Interrupt-on-Change pull-up is enabled on the corresponding pin
> 0 = Interrupt-on-Change pull-up is disabled unless explicitly enabled by a peripheral controlling the pin

Note 1:   Pull-up functionality can be used even if Interrupt-on-Change functionality is disabled.

Register 2-12: IOCPDx: Interrupt-on-Change x Pull-Down Enable Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			IOCPDx<15:8>[1]				
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			IOCPDx<7:0>[1]				
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **IOCPDx<15:0>:** Interrupt-on-Change x Pull-Down Enable bits[1]

1 = Interrupt-on-Change pull-down is enabled on the corresponding pin
0 = Interrupt-on-Change pull-down is disabled unless explicitly enabled by a peripheral controlling the pin

Note 1: Pull-down functionality can be used even if the Interrupt-on-Change functionality is disabled.

2.3 Slew Rate Control Registers

The following Slew Rate Control registers control the slew rate of the corresponding port pin:

- **SR1x: Slew Rate 1 Configuration x Register (High Bit)**
- **SR0x: Slew Rate 0 Configuration x Register (Low Bit)**

> **Note:** The slew rate functionality may not be implemented on all devices. For more information, refer to the specific device data sheet.

Register 2-13: SR1x: Slew Rate 1 Configuration x Register (High Bit)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SR1x<15:8>[1,2]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SR1x<7:0>[1,2]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **If SR1x is Implemented:**
SR1x<15:0>:SR0x<15:0>: Slew Rate Configuration bits[1,2]

11 = Slew rate control is enabled (slowest edge rate)
10 = Slew rate control is enabled (low edge rate)
01 = Slew rate control is enabled (medium edge rate)
00 = Slew rate control is disabled (fastest edge rate)

Note 1: Exact slew control rates are device-dependent. The SR1x bits may not be implemented.

2: The slew rate configuration setting is determined by the concatenated bits in the SR1x and the SR0x registers. For example, the slew rate for the PORTB register, bit 0, will be set by the values of SR1B<0> and SR0B<0>.

Register 2-14: **SR0x: Slew Rate 0 Configuration x Register (Low Bit)**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SR0x<15:8>[1,2]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SR0x<7:0>[1,2]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **If SR1x is Implemented:**
SR1x<15:0>:SR0x<15:0>: Slew Rate Configuration bits[1,2]

11 = Slew rate control is enabled (slowest edge rate)
10 = Slew rate control is enabled (low edge rate)
01 = Slew rate control is enabled (medium edge rate)
00 = Slew rate control is disabled (fastest edge rate)

If SR1x is Not Implemented:
SR0x<15:0>: Slew Rate Configuration bits[1,2]

1 = Slew rate control is enabled (slowest edge rate)
0 = Slew rate control is disabled (fastest edge rate)

Note 1: Exact slew control rates are device-dependent.

2: The Slew Rate configuration setting is determined by the concatenated bits in the SR1x and the SR0x registers. For example, the slew rate for the PORTB register, bit 0, will be set by the values of SR1B<0> and SR0B<0>.

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3.0 GENERAL I/O FUNCTIONALITY

3.1 TRIS Registers

The TRISx register control bits determine whether each pin associated with the I/O port is an input or an output. If the TRISx bit for an I/O pin is a value of '1', then the pin is an input. If the TRISx bit for an I/O pin is a value of '0', then the pin is configured as an output. An easy way to remember this is that a '1' looks like an I (Input) and a '0' looks like an O (Output). All port pins are defined as inputs after a Reset.

3.2 PORT Registers

Data on an I/O pin is accessed through a PORTx register. A read to the PORTx register reads the value of the I/O pin, while a write to the PORTx register writes the value to the port data latch. This will also be reflected on the PORTx pins if the TRISx is configured as an output and the multiplexed peripherals are disabled.

The BSET and BCLR instructions are Read-Modify-Write (RMW) operations. Therefore, a write to a port implies that the port pins are read, the value is modified and then written back to the port data latch. When Read-Modify-Write instructions are used on the PORTx registers, some I/O pins associated with the port are configured as inputs. If an I/O pin configured as an input is changed to an output, at a given time, an unexpected value may be output on the I/O pin. To avoid this, first write to the associated PORTx bit and then change the direction of the pin as an output.

In addition, if Read-Modify-Write instructions are used on the PORTx registers while the I/O pins are configured as outputs, unintended I/O behavior may occur based on the device speed and I/O capacitive loading. Figure 3-1 shows the unintended behavior that occurs if the user application attempts to set I/O bits 0 and 1 on the PORTA register, with two consecutive Read-Modify-Write instructions on the PORTA register. The unintended result of the example code at high CPU speed and high capacitive loading on the I/O pins is that I/O bit 1 is set high.

Figure 3-1: Example of Unintended I/O Behavior
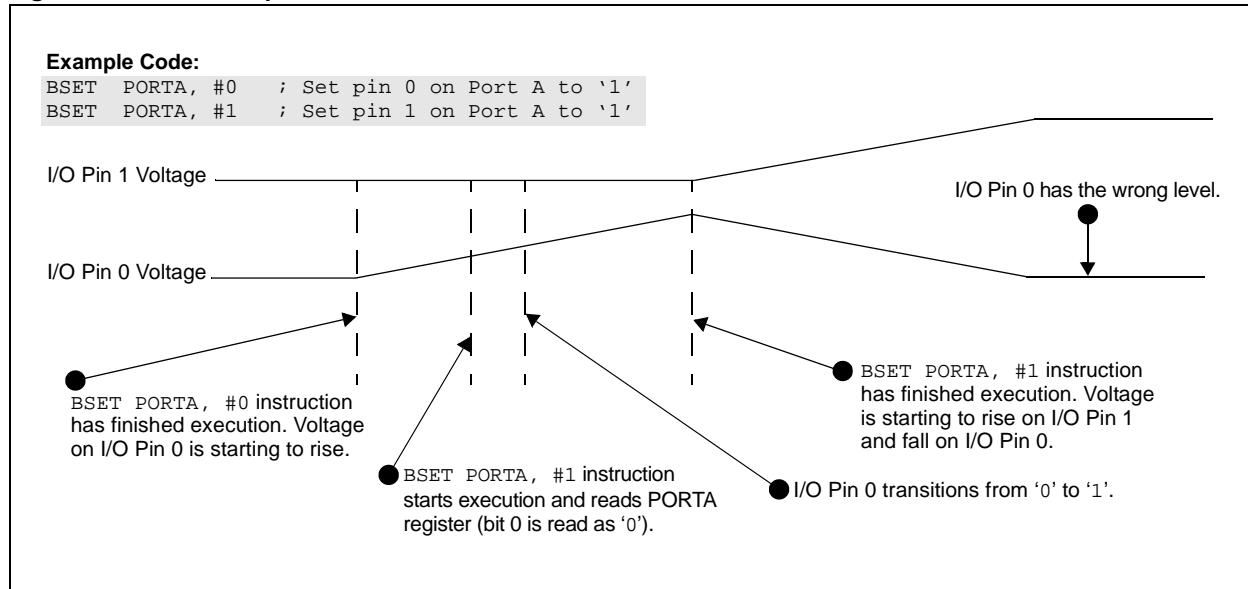
3.3   LAT Registers

The LATx register associated with an I/O pin eliminates the problems that may occur with Read-Modify-Write instructions. A read of the LATx register returns the values held in the port output latches instead of the values on the I/O pins. A Read-Modify-Write operation on the LATx register, associated with an I/O port, avoids the possibility of writing the input pin values into the port latches. A write to the LATx register has the same effect as a write to the PORTx register.

The differences between the PORTx and LATx registers can be summarized as follows:

- A write to the PORTx register writes the data value to the port latch
- A write to the LATx register writes the data value to the port latch
- A read of the PORTx register reads the data value on the I/O pin
- A read of the LATx register reads the data value held in the port latch

Any bit, and its associated data and control registers, that are not valid for a particular device will be disabled. That means the corresponding LATx and TRISx registers, and the port pin will be read as '0'.

3.4   ODC Registers

Each I/O pin can be individually configured for either normal digital output or open-drain output. This is controlled by the PORTx and Open-Drain Control (ODCx) registers associated with each I/O pin. If the ODCx bit for an I/O pin is '1', then the pin acts as an open-drain output. If the ODCx bit or an I/O pin is '0', then the pin is configured for a normal digital output (the ODCx bits are valid only for output pins). After a Reset, the bits in the ODCx register are set to '0'.

The open-drain feature allows a load to be connected to a voltage, higher or lower than V_{DD}, to any desired digital only pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum V_{IH} specification and the minimum is V_{SS}. The ODCx register settings effect all the I/O modes, allowing the output to behave as an open-drain output even if a peripheral is controlling the pin. The user may achieve the same effect by manipulating the corresponding LATx and TRISx bits, but this procedure will not allow the peripheral to operate in an Open-Drain mode (except for the default operation of the I^{2}C™ pins). Since I^{2}C pins are already open-drain pins, the ODCx register settings do not affect the I^{2}C pins or the JTAG output characteristics, as the JTAG scan cells are inserted between the ODCx logic and the I/O.

> **Note:**   The maximum V_{IH} specification for the PIC24FXXKXXXX family is limited to V_{DD}. This limits open-drain capability for higher voltage generation, but it can still be connected to a lower voltage than V_{DD}.

3.5   ANS Registers

Some I/O pins may be multiplexed with analog functions, such as A/D Converter input channels (see **Section 4.0 "Peripheral Multiplexing"**). In this case, the analog functionality on these pins has a higher priority than the digital functionality. This will prevent the use of digital functions, such as port I/Os, as long as the analog functionality is enabled. The ANSx bits configure the I/O pins in Analog or Digital mode. To use the digital I/O functionality on an analog multiplexed pin, its ANSx bit must be set to '0'. After a Reset, all the ANSx bits will be set to '1', configuring each pin with analog functionality in Analog mode.

If the I/O pin is configured as an analog input (ANSx bit = 1), the corresponding bit in the PORTx register will be read as zero. Also, any digital peripheral using this pin will read zero from this I/O pin.

4.0   PERIPHERAL MULTIPLEXING

The I/O pins can also be configured as digital inputs or outputs, and analog inputs or outputs. When configured as digital inputs, the I/O pins are either TTL buffers or Schmitt Triggers. When configured as digital outputs, the I/O pins are either CMOS drivers or open-drain outputs.

Many I/O pins support one or more peripheral modules. When configured to operate with a peripheral, a pin may not be used for general input or output. In many cases, a pin must be configured for input or output, although some peripherals override the TRISx configuration. Figure 4-1 shows how ports are shared with other peripherals and the associated I/O pins to which they are connected. For some dsPIC33/PIC24 devices, multiple peripheral functions may be multiplexed on each I/O pin. The priority of the peripheral function depends on the order of the pin description in the pin diagram of the specific product data sheet.

Figure 4-1:   **Structure of Port Shared with Non-PPS Peripherals**

Legend: R = Input buffer type depends on the peripheral. For more information, refer to the specific product data sheet.
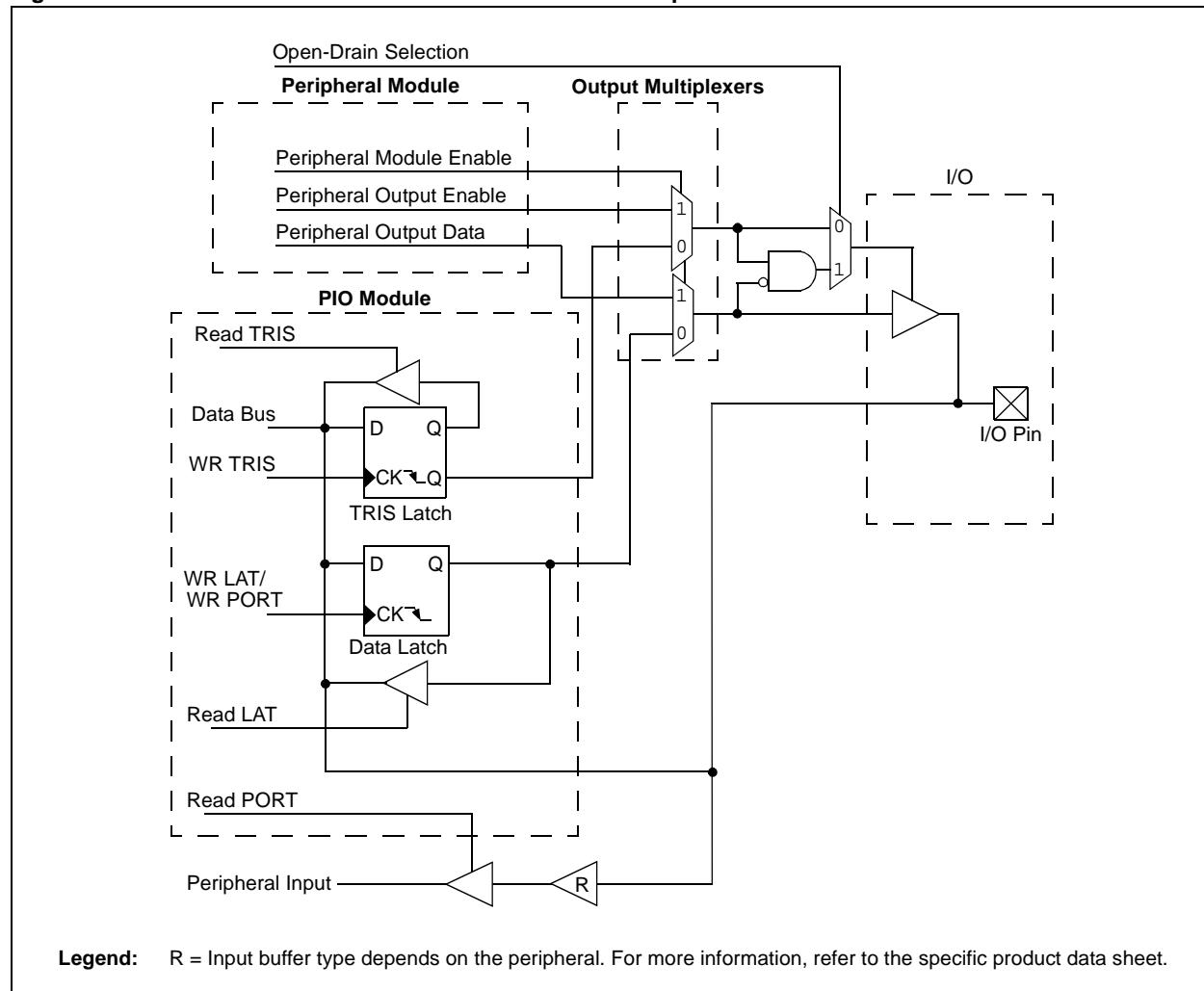
4.1　Multiplexing a Digital Input Peripheral

• The peripheral does not control the TRISx register.
• The PORTx data input path is unaffected. On reading the PORTx register, the status of the pin will be read.
• The peripheral input path is independent of the I/O input path with a special input buffer.

4.2　Multiplexing a Digital Output Peripheral

• The peripheral controls output data and the PORTx register has no effect.
• The PORTx register can read the pin value.
• If an output has an automatic tri-state feature (e.g., PWM outputs), the peripheral has the ability to tri-state the pin.

4.3　Multiplexing a Digital Bidirectional Peripheral

• The peripheral can automatically configure the pin as an output, but not as an input. The user needs to configure the pin as an input by setting the associated TRISx bit.
• The peripherals control output data and the PORTx register has no effect.
• The PORTx register can read the pin value.

4.4　Multiplexing an Analog Input Peripheral

• All digital port input buffers are disabled and the PORTx registers read '0' to prevent crowbar current.

4.5　Multiplexing an Analog Output Peripheral

• All digital port input buffers are disabled and the PORTx registers read '0' to prevent crowbar current.
• Analog output is driven onto the pin independent of the associated TRISx bit setting.

4.6　Software Input Pin Control

Some of the functions assigned to an I/O pin may be input functions that do not take control of the pin output driver. An example of one such peripheral is the input capture module. If the I/O pin associated with the input capture module is configured as an output, using the appropriate TRISx control bit, the user can manually affect the state of the input capture pin through its corresponding LATx register. This behavior can be useful in some situations, especially for testing purposes, when no external signal is connected to the input pin.

As shown in Figure 4-1, the organization of the peripheral multiplexers will determine if the peripheral input pin can be manipulated in software using the PORTx register. The conceptual peripherals shown in this figure disconnect the port data from the I/O pin when the peripheral function is enabled.

In general, the following peripherals allow their input pins to be controlled manually through the PORTx registers:

• External Interrupt Pins
• Timer Clock Input Pins
• Input Capture Pins
• PWM Fault Pins

Most serial communication peripherals, when enabled, take full control of the I/O pin, so that the input pins associated with the peripheral cannot be effected through the corresponding PORTx registers. These peripherals include the following:

• SPI
• I^{2}C™
• UART

5.0   PERIPHERAL PIN SELECT (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin count devices. In an application, where more than one peripheral is needed to be assigned to a single pin, an inconvenient work around in application code or a complete redesign may be the only option.

The Peripheral Pin Select configuration provides an alternative to these choices by allowing users to select which peripheral functions are available, on which pins, for a wide range of peripherals and pins. By increasing the pinout options available on a particular device, users can better tailor the microcontroller to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to any one of these I/O pins. The PPS is performed in software and generally does not require the device to be reprogrammed. The hardware safeguards are included, that prevent accidental or spurious changes to the peripheral mapping, once it has been established.

> **Note:**   Some devices do not have the PPS feature. For more information, refer to the specific device data sheet.

5.1   Available Pins

The PPS feature is used with a range of I/O pins. The number of available I/O pins is dependent on the particular device and its pin count. The pins that support the PPS feature include the designation, "RPn", in their full pin designation, where "RP" designates a remappable peripheral and "n" is the remappable pin number. If the pin supports only the input function PPS feature, then it will be designated as "RPIn". For more information, refer to the device pinout in the respective device data sheet.

5.2   Available Peripherals

The peripherals managed by the PPS are all digital only peripherals. These include the general serial communications (UART and SPI), the general purpose timer clock inputs, the timer related peripherals (input capture and output compare) and the external interrupt inputs.

In comparison, some digital only peripheral modules are not currently included in the PPS feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I^2C, specialty communications (Ethernet and USB), Real-Time Clock and Calendar (RTCC) alarm output and all modules with analog inputs, such as the Analog-to-Digital Converter.

A key difference between the remappable and non-remappable peripherals is that the remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, the non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. The priority is given regardless of the type of peripheral that is mapped. The remappable peripherals never take priority over any analog functions associated with the pin. Figure 5-1 shows the structure of the port shared with PPS peripherals.

Figure 5-1: **Structure of Port Shared with PPS Peripherals**
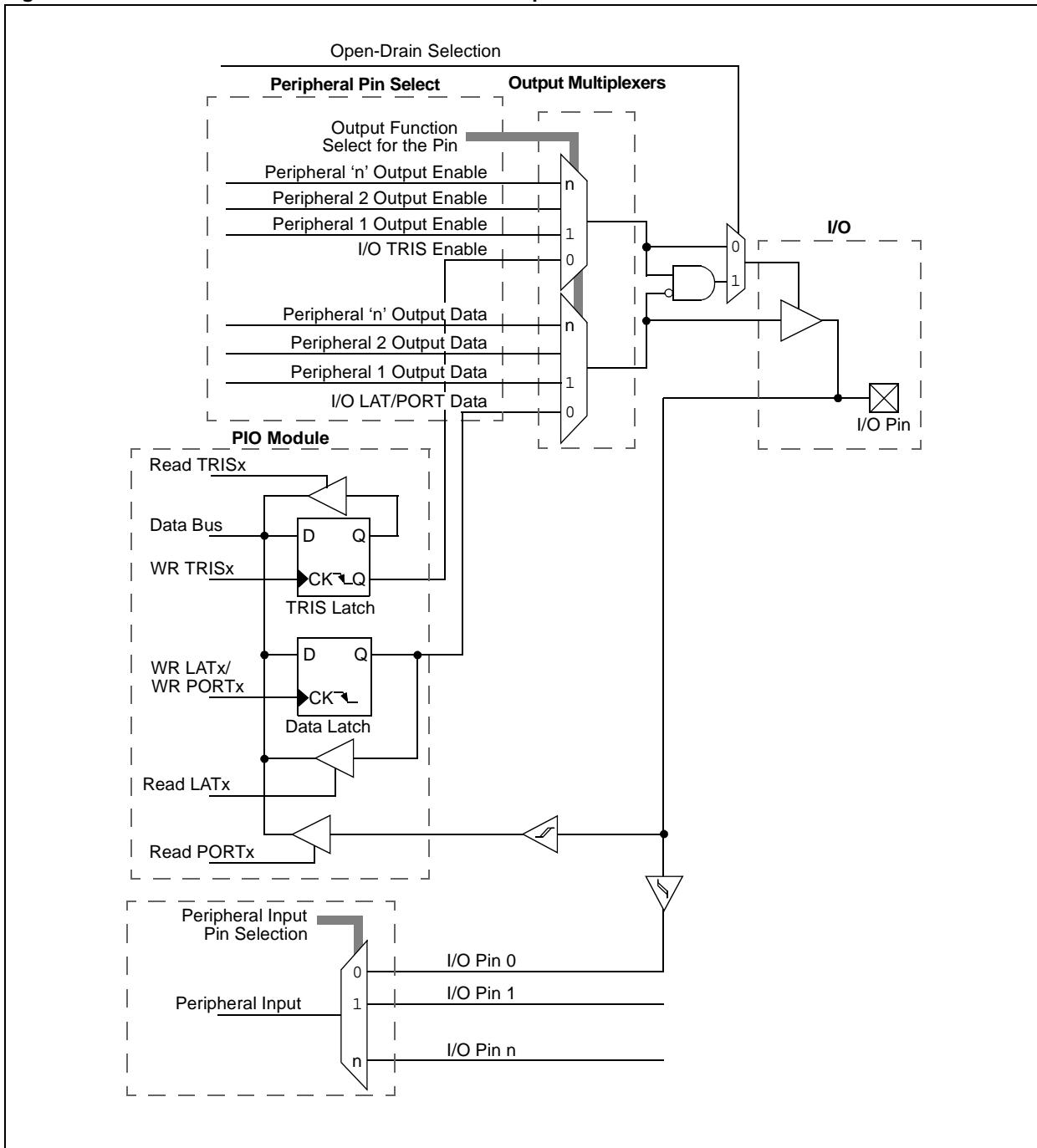
5.3   Controlling Peripheral Pin Select

The Peripheral Pin Select features are controlled through two sets of Special Function Registers (SFRs): one to map peripheral inputs and one to map peripheral outputs. As they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on if an input or output is being mapped.

5.3.1   INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral; that is, a bit field associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers (see Register 5-1 and Table 5-1) contain sets of 6-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an RPn or RPIn value maps the RPn or RPIn pin to that peripheral. For any given device, the valid range of values for any of the bit fields corresponds to the maximum number of Peripheral Pin Selections supported by the device.

The peripheral inputs that support the Peripheral Pin Selection have no default pins. Since the implemented bit fields of the RPINRx register reset to all '1's, the inputs are all tied to VSS in the device's default (Reset) state.

For example, assigning the RPINR18<5:0> register bits to 0x2 selects RP2 as the U1RX input. Figure 5-2 shows the remappable pin selection for the U1RX input.

Figure 5-2:   Remappable Input for U1RX
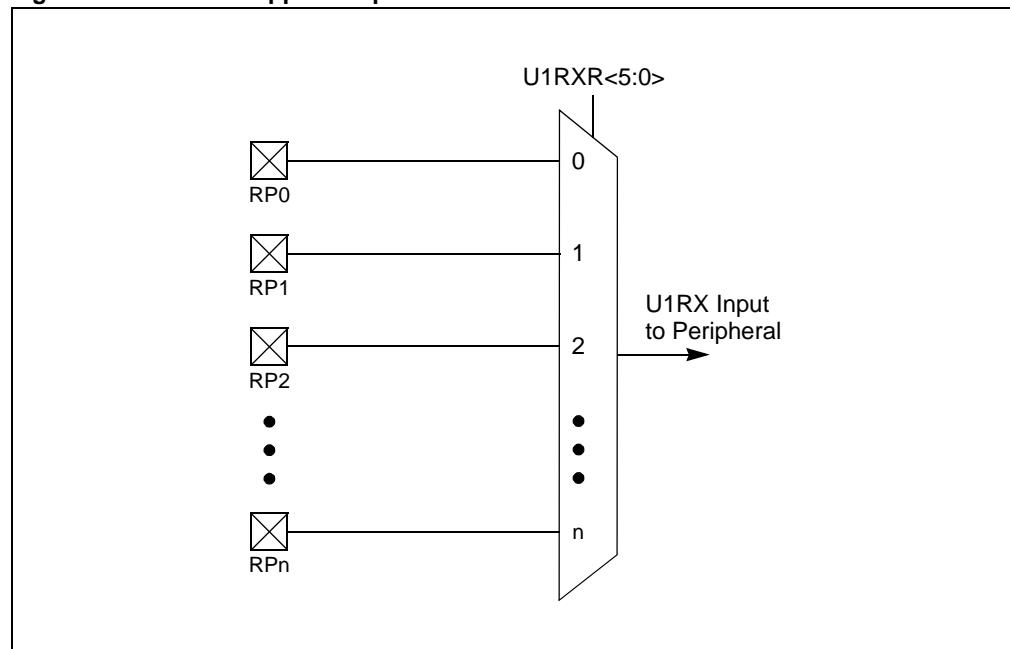
dsPIC33/PIC24 Family Reference Manual

Table 5-1: Selectable Input Sources Example (Maps Input to Function)

Input Name[1]	Function Name	Register Bits	Configuration Bits
External Interrupt 1	INT1	RPINR0<13:8>	INT1R<5:0>
External Interrupt 2	INT2	RPINR1<5:0>	INT2R<5:0>
External Interrupt 3	INT3	RPINR1<13:8>	INT3R<5:0>
External Interrupt 4	INT4	RPINR2<5:0>	INT4R<5:0>
Timer2 External Clock	T2CK	RPINR3<5:0>	T2CKR<5:0>
Timer3 External Clock	T3CK	RPINR3<13:8>	T3CKR<5:0>
Timer4 External Clock	T4CK	RPINR4<5:0>	T4CKR<5:0>
Timer5 External Clock	T5CK	RPINR4<13:8>	T5CKR<5:0>
Input Capture 1	IC1	RPINR7<5:0>	IC1R<5:0>
Input Capture 2	IC2	RPINR7<13:8>	IC2R<5:0>
Input Capture 3	IC3	RPINR8<5:0>	IC3R<5:0>
Input Capture 4	IC4	RPINR8<13:8>	IC4R<5:0>
Input Capture 5	IC5	RPINR9<5:0>	IC5R<5:0>
Output Compare Fault A	OCFA	RPINR11<5:0>	OCFAR<5:0>
Output Compare Fault B	OCFB	RPINR11<13:8>	OCFBR<5:0>
UART1 Receive	U1RX	RPINR18<5:0>	U1RXR<5:0>
UART1 Clear-To-Send	U1CTS	RPINR18<13:8>	U1CTSR<5:0>
UART2 Receive	U2RX	RPINR19<5:0>	U2RXR<5:0>
UART2 Clear-To-Send	U2CTS	RPINR19<13:8>	U2CTSR<5:0>
SPI1 Data Input	SDI1	RPINR20<5:0>	SDI1R<5:0>
SPI1 Clock Input	SCK1	RPINR20<13:8>	SCK1R<5:0>
SPI1 Slave Select Input	SS1	RPINR21<5:0>	SS1R<5:0>
SPI2 Data Input	SDI2	RPINR22<5:0>	SDI2R<5:0>
SPI2 Clock Input	SCK2	RPINR22<13:8>	SCK2R<5:0>
SPI2 Slave Select Input	SS2	RPINR23<5:0>	SS2R<5:0>

Note 1: Available PPS input sources vary between devices depending on which peripherals are available. For more information, refer to the specific device data sheet.

5.3.2   OUTPUT MAPPING

In contrast to inputs, the outputs of the Peripheral Pin Select options are mapped on the basis of the pin. In this case, a bit field associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers contain sets of 6-bit fields, with each set associated with one RPn pin (see Register 5-2). The value of the bit field corresponds to one of the peripherals and that peripheral's output is mapped to the pin (see Table 5-2 and Figure 5-3).

The peripheral outputs that support the Peripheral Pin Selection have no default pins. Since, the RPORx registers reset to all '0's, the outputs are all disconnected in the device's default (Reset) state,

The list of peripherals for output mapping also includes a null value of, '000000', because of the mapping technique. This permits any given pin to remain unconnected from the output of any of the pin-selectable peripherals.

Figure 5-3:   Multiplexing of Remappable Output for RPn
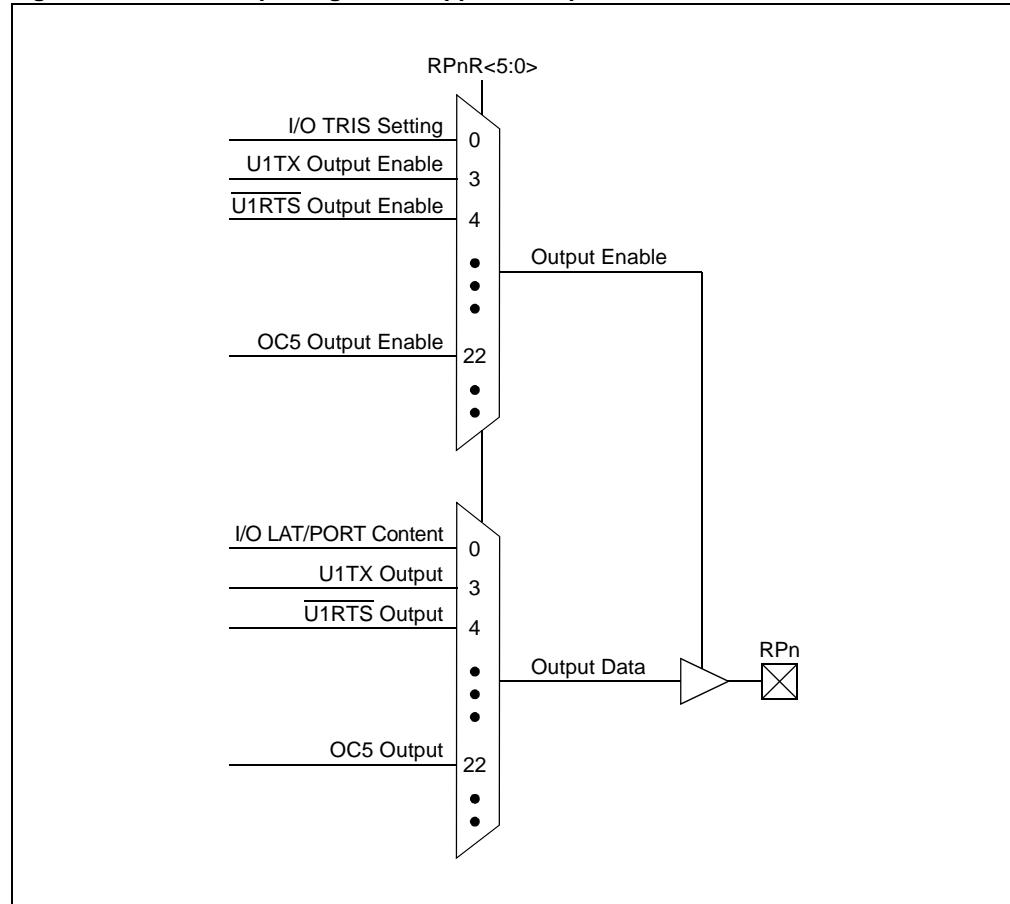
Table 5-2: Output Selection for Remappable Pin Example (RPn)

Function[1]	RPnR<5:0> Bits	Output Name
NULL	0	This pin is an I/O Port Pin.
C1OUT	1	RPn is tied to Comparator 1 Output.
C2OUT	2	RPn is tied to Comparator 2 Output.
U1TX	3	RPn is tied to UART1 Transmit.
U1RTS	4	RPn is tied to UART1 Ready-To-Send.
U2TX	5	RPn is tied to UART2 Transmit.
U2RTS	6	RPn is tied to UART2 Ready-To-Send.
SDO1	7	RPn is tied to SPI1 Data Output.
SCK1OUT	8	RPn is tied to SPI1 Clock Output.
SS1OUT	9	RPn is tied to SPI1 Slave Select Output.
SDO2	10	RPn is tied to SPI2 Data Output.
SCK2OUT	11	RPn is tied to SPI2 Clock Output.
SS2OUT	12	RPn is tied to SPI2 Slave Select Output.
OC1	18	RPn is tied to Output Compare 1.
OC2	19	RPn is tied to Output Compare 2.
OC3	20	RPn is tied to Output Compare 3.
OC4	21	RPn is tied to Output Compare 4.
OC5	22	RPn is tied to Output Compare 5.

Note 1: Available PPS output functions vary between devices depending on which peripherals are available. For more information, refer to the specific device data sheet.

Table 5-3: Registers Associated with Output Function on RPn Pin

Pins	Registers	Associated Bits
RP0	RPOR0<5:0>	RP0R<5:0>
RP1	RPOR0<13:8>	RP1R<5:0>
RP2	RPOR1<5:0>	RP2R<5:0>
RPn	RPORn/2<5:0>	RPnR<5:0>
RPn + 1	RPORn/2<13:8>	RPn + 1R<5:0>

Legend: n = 0, 2, 4,..., etc.

5.3.3   MAPPING LIMITATIONS

The control schema of the peripheral select pins is not limited to a small range of fixed peripheral configurations. There are no mutual or hardware enforced lockouts between any of the peripheral mapping SFRs. Literally, any combination of peripheral mappings across any or all of the RPn pins is possible. This includes both many-to-one and one-to-many mappings of peripheral inputs, and outputs to pins. While such mappings may be technically possible from a configuration point of view, the user must ensure the selected configurations are supportable from an electrical point of view.

5.4   Controlling Configuration Changes

As peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. The dsPIC33/PIC24 devices include three features to prevent alterations to the peripheral map:

• Control register lock sequence
• Continuous state monitoring
• Configuration bit remapping lock

5.4.1   CONTROL REGISTER LOCK

Under normal operation, writes to the RPINRx and the RPORx registers are not allowed; attempted writes will appear to execute normally, but the contents of the registers will remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK bit (OSCCON<6>). Setting the IOLOCK bit prevents writes to the control registers; clearing IOLOCK allows writes.

To set or clear the IOLOCK bit, a specific command sequence must be executed:

1.   Write 46h to OSCCON<7:0>.
2.   Write 57h to OSCCON<7:0>.
3.   Clear (or set) IOLOCK as a single operation.

The unlock/lock sequence must be executed as an assembly language routine in the same manner as changes to the oscillator configuration, because the unlock sequence is timing-critical. If the bulk of the application is written in 'C' language, or other high-level language, the unlock sequence should be performed by writing inline assembly, or using built-in functions provided by the MPLAB® XC16 C Compiler.

The IOLOCK bit remains in one state until changed. This allows all of the Peripheral Pin Selects to be configured with a single unlock sequence, followed by an update to all control registers, then locked with a second lock sequence.

> **Note:**   MPLAB® XC16 C Compiler provides built-in 'C' language functions for unlocking the OSCCON register:
> ```
> __builtin_write_OSCCONL(value)
> __builtin_write_OSCCONH(value)
> ```
> See the *"MPLAB® XC16 C Compiler User's Guide"* (DS50002071)for more information.

5.4.2   CONTINUOUS STATE MONITORING

In addition to being protected from direct writes, the contents of the RPINRx and RPORx registers are constantly monitored in hardware by Shadow registers. If an unexpected change in any of the registers occurs, such as cell disturbances caused by ESD or other external events, a Configuration Mismatch (CM) Reset will be triggered.

5.4.3   CONFIGURATION BIT PIN SELECT LOCK

As an additional level of safety, the device can be configured to prevent more than one write in the session to the RPINRx and RPORx registers. The IOL1WAY Configuration bit (FOSC<5>) blocks the IOLOCK bit from being cleared after it has been set once.

In the default (unprogrammed) state, the IOL1WAY bit is set, restricting users to one write session. Programming the IOL1WAY Configuration bit allows users unlimited access (with the proper use of the unlock sequence) to the PPS registers.

5.5   Considerations for Peripheral Pin Selection

The ability to control the Peripheral Pin Selection introduces several considerations into application design that must be considered. This is particularly true for several common peripherals which are only available as remappable peripherals.

Before any other application code is executed, the user must initialize the device with the proper peripheral configuration. Since the IOLOCK bit resets in the unlocked state, it is not necessary to execute the unlock sequence after the device has come out of Reset. For the sake of application safety, however, it is always a good idea to set the IOLOCK bit and lock the configuration after writing to the control registers.

Choosing the configuration requires a review of all Peripheral Pin Selects and their pin assignments, especially those that will not be used in the application. In all cases, unused pin-selectable peripherals must be disabled. The unused peripherals must have their inputs assigned to Vss. The I/O pins with unused RPn functions should be configured with the NULL ('0') peripheral output.

The assignment of an RPn pin to the peripheral input or output depends on the peripheral and its use in the application. It is better to assign the pin immediately following a device Reset and before the peripheral configuration.

The assignment of a peripheral output to a particular pin does not automatically perform any other configuration of the pin's I/O circuitry. This means adding a pin-selectable output to a pin may result in inadvertently driving an existing peripheral input when the output is driven. The users must be familiar with the behavior of other fixed peripherals that share a remappable pin. To be safe, fixed digital peripherals that share the same pin should be disabled when not in use.

Configuring a remappable pin for a specific peripheral input does not automatically turn that feature on. The peripheral must be specifically configured for operation and enabled, as if it were tied to a fixed pin.

A final consideration is that, the PPS functions neither override analog inputs nor reconfigure pins with analog functions for digital I/Os. If a pin is configured as an analog input on a device Reset, it must be explicitly reconfigured as a digital I/O when used with a Peripheral Pin Select.

5.5.1   BASIC STEPS TO USE PERIPHERAL PIN SELECTION

The following are the basic steps to use the PPS feature:

1. Disable any fixed digital peripherals on the pins to be used.
2. Switch pins to be used for digital functionality (if they have analog functionality) using the ANSx register.
3. Unlock the OSCCON register and clear the IOLOCK bit (the bit is not required after device Reset).
4. Set the RPINRx and the RPORx registers appropriately.
5. Unlock the OSCCON register and set the IOLOCK bit to '1'.
6. Configure and enable the newly mapped PPS peripherals.

Example 5-1 shows a configuration for bidirectional communication with flow control using UART1. The following input and output functions are used:

- Input Functions: U1RX, $\overline{\text{U1CTS}}$
- Output Functions: U1TX, $\overline{\text{U1RTS}}$

Example 5-1: **Configuring UART1 Input and Output Functions**

```
//**************************************************************
// Unlock Registers
//**************************************************************
__builtin_write_OSCCONL(OSCCON & 0xbf)   //clear the bit 6 of OSCCONL to
                                         //unlock Pin Re-map
//********************************************************************
//This code is used when interested in inline assembly. If this code is
//used then the above two lines should not be used for unlocking.
//********************************************************************
/*
asm volatile    ("push   w1                 \n"
                "push   w2                 \n"
                "push   w3                 \n"
                "mov    #OSCCON, w1        \n"
                "mov    #0x46, w2          \n"
                "mov    #0x57, w3          \n"
                "mov.b  w2, [w1]           \n"
                "mov.b  w3, [w1]           \n"
                "bclr   OSCCON, #6         \n"
                "pop    w3                 \n"
                "pop    w2                 \n"
                "pop    w1");
*/
//**************************************************************
// Configure Input Functions
//**************************************************************
    //**************************
    // Assign U1Rx To Pin RP0
    //**************************
    RPINR18bits.U1RXR = 0;                   //'0' represents RP0

    //**************************
    // Assign U1CTS To Pin RP1
    //**************************
    RPINR18bits.U1CTSR = 1;                  //'1' represents RP1

//**************************************************************
// Configure Output Functions
//**************************************************************
    //**************************
    // Assign U1Tx To Pin RP2
    //**************************
    RPOR1bits.RP2R = 3;                      //'3' represents U1TX

    //**************************
    // Assign U1RTS To Pin RP3
    //**************************
    RPOR1bits.RP3R = 4;                      //'4' represents U1RTS

//**************************************************************
// Lock Registers
//**************************************************************
__builtin_write_OSCCONL(OSCCON | 0x40)   //set the bit 6 of OSCCONL to
                                         //lock Pin Re-map
//********************************************************************
//This code is used when interested in inline assembly. If this code is //
used then the above two lines should not be used for locking.
//********************************************************************
/*
asm volatile    ("push   w1                 \n"
                "push   w2                 \n"
                "push   w3                 \n"
                "mov    #OSCCON, w1        \n"
                "mov    #0x46, w2          \n"
                "mov    #0x57, w3          \n"
                "mov.b  w2, [w1]           \n"
                "mov.b  w3, [w1]           \n"
                "bset   OSCCON, #6         \n"
                "pop    w3                 \n"
                "pop    w2                 \n"
                "pop    w1";
*/
```

5.6 Peripheral Pin Select Registers

The following PPS registers are used to configure input and output functionality of the dsPIC33/PIC24 device pins.

- **RPINRx:** Peripheral Pin Select Input Register x
- **RPORy:** Peripheral Pin Select Output Register y

Register 5-1: RPINRx: Peripheral Pin Select Input Register x[2]

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	Input Function bits<5:0>[1]					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	Input Function bits<5:0>[1]					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14   **Unimplemented:** Read as '0'

bit 13-8   **Input Function Bits<5:0>:** Assign Peripheral to corresponding RPn pin bits[1]

bit 7-6   **Unimplemented:** Read as '0'

bit 5-0   **Input Function Bits<5:0>:** Assign Peripheral to corresponding RPn pin bits[1]

Note 1: Here, 'n' represents the peripheral select input pin number.

    2: Here, 'x' represents the Peripheral Pin Select Input register number and it varies from device to device.

Register 5-2: **RPORy: Peripheral Pin Select Output Register y[2]**

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RPnR<5:0>[1]					

bit 15   bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RPnR<5:0>[1]					

bit 7   bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14   **Unimplemented:** Read as '0'

bit 13-8   **RPnR<5:0>:** Peripheral Output Function is assigned to RPn pin bits[1]
(see Table 5-2 for peripheral function numbers)

bit 7-6   **Unimplemented:** Read as '0'

bit 5-0   **RPnR<5:0>:** Peripheral Output Function is assigned to RPn pin bits[1]
(see Table 5-2 for peripheral function numbers)

Note 1:   Here, 'n' represents the Peripheral Pin Select output pin number.

     2:   Here, 'y' represents the Peripheral Pin Select Output register number and it varies from device to device.

5.7   Virtual Connections

The virtual connections provide a simple method for inter-peripheral connection without using a physical pin. Some devices may implement peripherals that generate outputs that will be useful as inputs to other peripherals that normally accept inputs from pins that are determined by PPS configuration. In this case, these devices may implement those outputs as virtual output pins (RPVx). These virtual output pins correspond to the actual PPS-addressable pins (RPy). The value of one of these corresponding pins can be used to configure any of the PPS Input registers. For example, a device can assign the output of a comparator peripheral to RPV0, a virtual pin which can correspond to RP84. The user can then configure any PPS input field in any RPINRx register with the value of 84 to use that comparator output as an input to another peripheral.

6.0   INTERRUPT-ON-CHANGE

The Interrupt-on-Change function of the I/O ports allows a device to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature is capable of detecting input COS, even in Sleep mode when the clocks are disabled. To use any Interrupt-on-Change functionality, the IOCON bit (PADCON<15>) must be set.

Interrupt-on-Change functionality is enabled on a pin by setting the IOCPx and/or IOCNx register bit for that pin. Setting a value of '1' in the IOCPx register bit enables interrupts for low-to-high transitions, while setting a value of '1' in the IOCNx register bit enables interrupts for high-to-low transitions. Setting a value of '1' in both register bits will enable interrupts for either case (a pulse on the pin will generate two interrupts).

When an interrupt request is generated for a pin, the corresponding status flag (IOCFx register bit) will be set, indicating that a COS occurred on that pin. The IOCFx register bit will remain set until cleared by writing a zero to it. When any IOC bit in a given port is set, the corresponding IOCPxF bit in the IOCSTAT register will be set. This flag indicates that a change was detected on one of the bits on the given port. The IOCPxF flag will be cleared when all of the IOCFx<15:0> bits are cleared. Multiple individual status flags can be cleared by writing a zero to one or more bits using a Read-Modify-Write operation. If another edge is detected on a pin whose status bit is being cleared during the Read-Modify-Write sequence, the associated change flag will still be set at the end of the Read-Modify-Write sequence.

The user should use the instruction sequence (or equivalent) shown in Example 6-1 to clear the Interrupt Status registers. At the end of this sequence, the W0 register will contain a zero for each bit for which the port pin had a change detected. In this way, any indication of a pin changing will not be lost.

Example 6-1:   IOC Status Read/Clear in Assembly

```
MOV     #0xFFFF, W0     ;Initial mask value 0xFFFF -> W0
XOR     IOCFx, W0       ;W0 has '0' for each bit set in IOCFx
AND     IOCFx           ;IOCFx & W0 -> IOCFx
```

Due to the asynchronous and real-time nature of the IOC, the value read on the port pins may not indicate the state of the port when the change was detected, as a second change can occur during the interval between clearing the flag and reading the port. It is up to user code to handle this case if it should be a possibility in their application. To keep this interval to a minimum, it is recommended that any code modifying the IOCFx registers be run either in the interrupt handler or with interrupts disabled.

Each IOC pin has both a weak pull-up and a weak pull-down connected to it. The pull-ups act as a current source connected to the pin, while the pull-downs act as a current sink connected to the pin. These eliminate the need for external resistors when push button or keypad devices are connected. The pull-ups and pull-downs are separately enabled using the IOCPUx registers (for pull-ups) and the IOCPDx registers (for pull-downs). Each IOC pin has individual control bits for its pull-up and pull-down. Setting a control bit enables the weak pull-up or pull-down for the corresponding pin.

> **Note:**   Pull-ups and pull-downs on pins must always be disabled whenever the pin is configured as a digital output.

I/O Ports with Interrupt-on-Change (IOC)

Figure 6-1 shows the IOC logic functionality per pin.

Figure 6-1: **IOC Logic Functionality Per Pin**
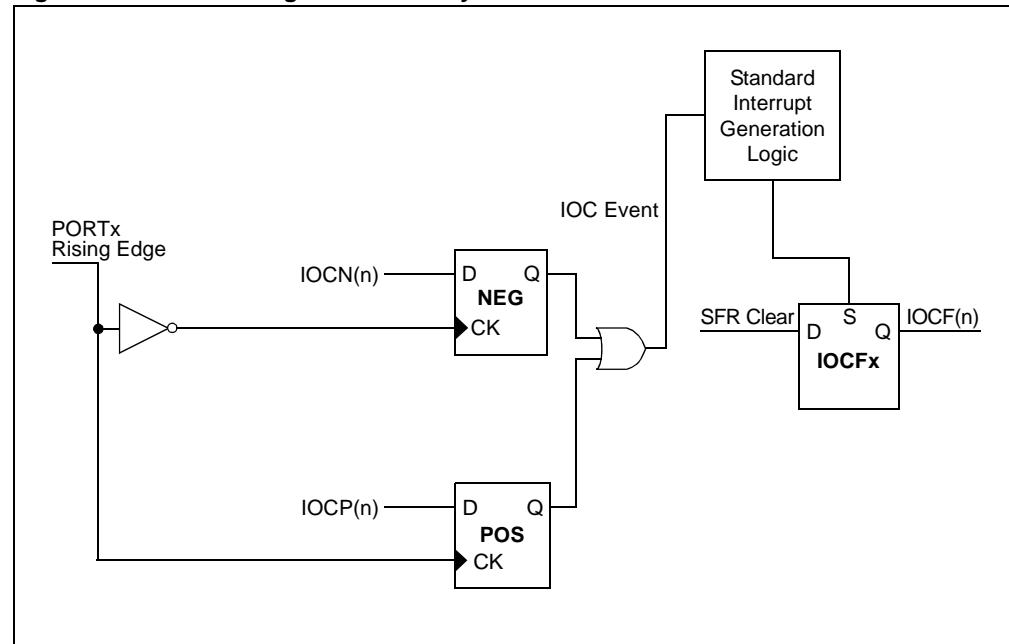
6.1   IOC Configuration and Operation

The IOC pins are configured as follows:

1. Enable Interrupt-on-Change functionality by setting the IOCON bit in the PADCON register.
2. Ensure that the IOC pin is configured as a digital input by setting the associated bits in the ANSx and the TRISx registers.
3. Enable interrupts for the selected IOC pins and edge types by setting the appropriate bits in the IOCPx and IOCNx registers.
4. Turn on weak pull-ups or pull-downs for the selected IOC pins by setting the appropriate bits in the IOCPUx and IOCPDx registers.
5. Clear the IOCFx register bits and the IOCIF interrupt flag.
6. Set the desired interrupt priority level for IOC interrupts using the IOCIP<2:0> control bits.
7. Enable IOC interrupts using the IOCIE control bit.

When an IOC interrupt occurs, the user should read the IOCPxF bits in the IOCSTAT register to determine which ports have experienced IOC events. The user should then read the corresponding IOCFx registers for those ports to determine which pins have experienced IOC events.

6.2   IOC Operation in Sleep and Idle Modes

The IOC module continues to operate in Sleep or Idle mode. If one of the enabled IOC pins changes state, the IOCIF interrupt flag will be set. If the IOCIE bit is set, the device will wake from Sleep or Idle mode and resume operation.

If the assigned priority level of the IOC interrupt is equal to or less than the current CPU priority level, device execution will continue from the instruction immediately following the `SLEEP` or `IDLE` instruction.

If the assigned priority level of the IOC interrupt is greater than the current CPU priority level, device execution will continue from the IOC interrupt vector address.

7.0 REGISTER MAP

A summary of the registers associated with the dsPIC33/PIC24 I/O ports is provided in Table 7-1.

Table 7-1: Special Function Registers Associated with I/O Ports[1]

Register Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISx	TRISx<15:0>																FFFF
LATx	LATx<15:0>																xxxx
PORTx	PORTx<15:0>																xxxx
ODCx	ODCx<15:0>																0000
ANSx	ANSx<15:0>																FFFF
IOCPx	IOCPx<15:0>																FFFF
IOCNx	IOCNx<15:0>																xxxx
IOCFx	IOCFx<15:0>																xxxx
IOCPUx	IOCPUx<15:0>																0000
IOCPDx	IOCPDx<15:0>																0000
SR1x	SR1x<15:0>																0000
SR0x	SR0x<15:0>																0000
PADCON	IOCON	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IOCSTAT	—	—	—	—	—	—	IOCPJF	IOCPIF	IOCPHF	IOCPGF	IOCPFF	IOCPEF	IOCPDF	IOCPCF	IOCPBF	IOCPAF	0000

Note 1: Refer to the specific device data sheet for the I/O Ports register map details.

8.0   RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33/PIC24 device families, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the I/O Ports with Interrupt-on-Change (IOC) are:

Title	Application Note #
No related application notes are available at this time.	N/A

Note:	Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the dsPIC33/PIC24 device families.

9.0   REVISION HISTORY

Revision A (May 2014)

This is the initial released revision of this document.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.

- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.

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