Digital System

A Report
Presented to
The Department of Building Engineering

COEN 313

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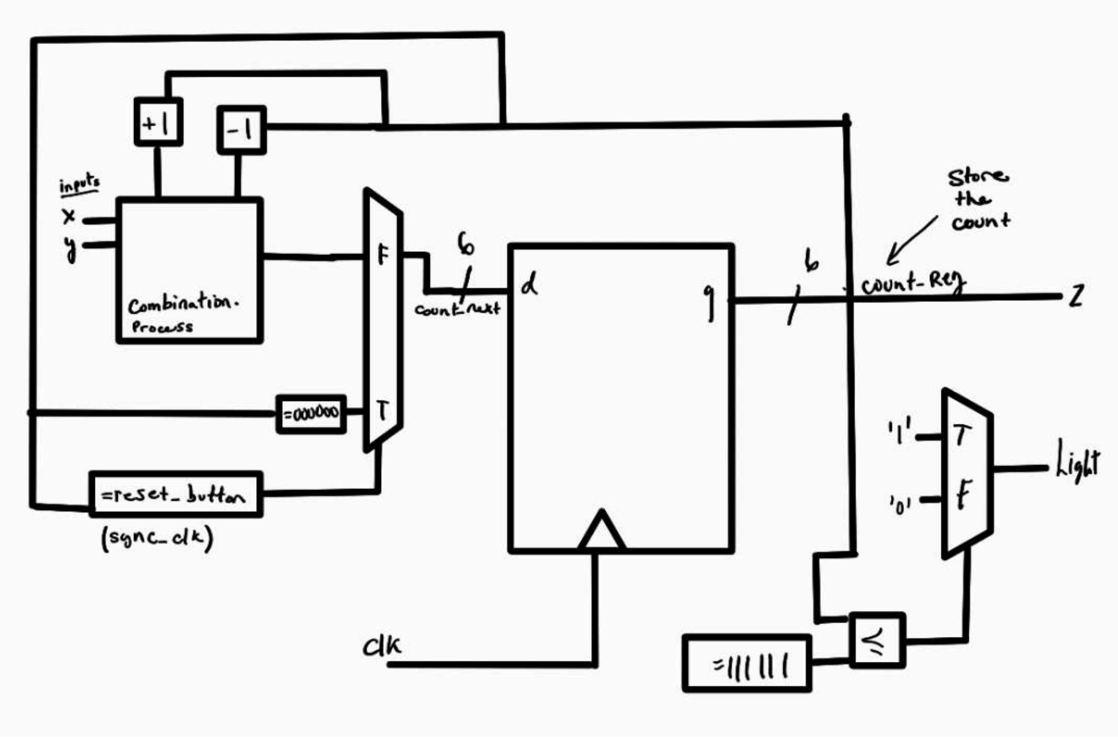
Abstract

The job demanded for this project was to build a digital system from scratch. This digital system had to complete the task of counting the amount of people in a room. To do this project, we had to take into account that someone entering the room activated a photocell that sends a X signal, and a Y signal for someone leaving the room. Also, the room has a max occupancy of 63 people. When that limit is reached, the room emits a red light. The system needs a synchronous reset system to reset the count of people to zero. To begin the project, we have to draw a conceptual diagram of this system using all the knowledge and conditions mentioned previously. After drawing a conceptual diagram, we have to implement this drawing into a VHDL code. To make sure the VHDL code of the system works, we need to do test benches of multiple situations that could happen. Finally, with the code, we need to generate an RTL diagram using Vivado.

Results

1. Conceptual diagram

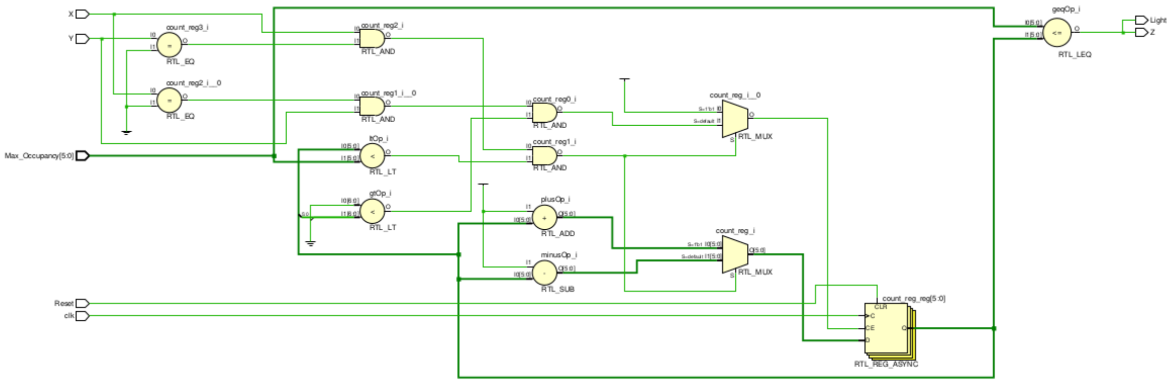


2. VHDL code for the project

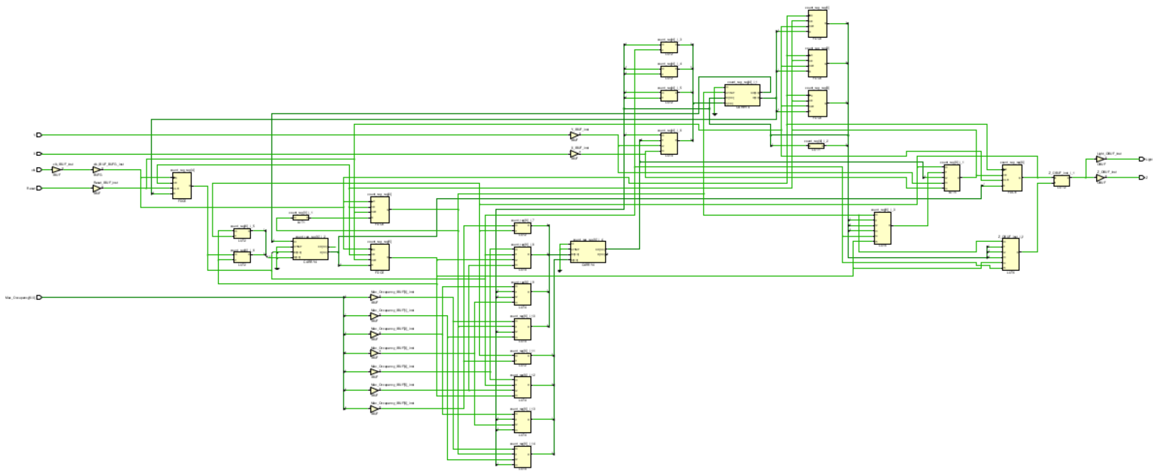
```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity PeopleCounter is
    port (
    X: in std_logic; -- enters
    Y: in std_logic; -- exits
    Max_Occupancy: in std_logic_vector(5 downto 0); -- maximum occupancy
    Reset: in std_logic; -- synchronous
    clk: in std_logic;
    Z: out std_logic;
    Light: out std_logic -- red light output
    );
end PeopleCounter;

architecture Project of PeopleCounter is
    signal count_reg:std_logic_vector  (5 downto 0) := (others => '0');
    signal count_next: std_logic_vector (5 downto 0) := (others => '0');
    signal count_comb: std_logic_vector (5 downto 0) := (others => '0'); -- combinational process signal
    signal Light_reg:  std_logic := '0'; -- signal for red light state
begin

    process (clk, Reset, count_reg)
    begin
    if Reset = '1' then -- synchronous reset
    count_reg <= (others => '0'); -- reset count_reg to “000000”
    Light_reg <= '0'; -- reset light state
    elsif (clk'event and clk ='1') then
    count_comb <= count_reg;

    if X = '1' and Y = '0' and count_reg < Max_Occupancy then
    count_reg <= count_reg + 1; -- increment
    elsif X = '0' and Y = '1' and count_reg > 0 then
    count_reg <= count_reg - 1; --decrement
    end if;
    end if;
    end process;

    Z <= '1' when count_reg >= Max_Occupancy else '0';

    -- Update red light state
    process (count_reg)
    begin
    if count_reg >= Max_Occupancy then
    Light <= '1'; -- turn on light
    else
    Light <= '0'; -- turn off light
    end if;
    end process;


end Project;
```

3. RTL elaborated and synthesis diagram

3.1 Elaborated diagram



3.2 Synthesis diagram



Analysis

Conceptual Diagram

My conceptual diagram starts with a D-FlipFlop that inputs a clock called CLK. The D of the flip flop outputs a signal called count_next that goes to count_comb. The count_comb is the updated signal of the count_next after it goes through a combinational process. This combinational process checks for the presence of an X signal or a Y signal emitted by the photocells when the clock is ‘0’. If the signal emitted is a X signal, the process will increment (+1) count_reg by 1. On the other hand, if the signal emitted is a Y signal, the process will decrement (-1) count_reg by 1. In fact, count_reg is the register where the number of people is stored. Before and after the conceptual process, there are two mux that play different roles in the program. One of them is a synchronous reset, the other one is a maximum occupancy detector. The synchronous reset, unlike the asynchronous one, resets the count_reg to “000000” when it is at its rising edge and when it is not at its rising edge, it does nothing and continues to the combinational process. The other mux is used to detect when the maximum occupancy is reached (63 people). When count_reg is bigger or equal to the max_occupancy, the mux will send a signal to the red light to activate it. Also, when the maximum occupancy is reached, the Z output becomes 1.

Test Bench (Do files)

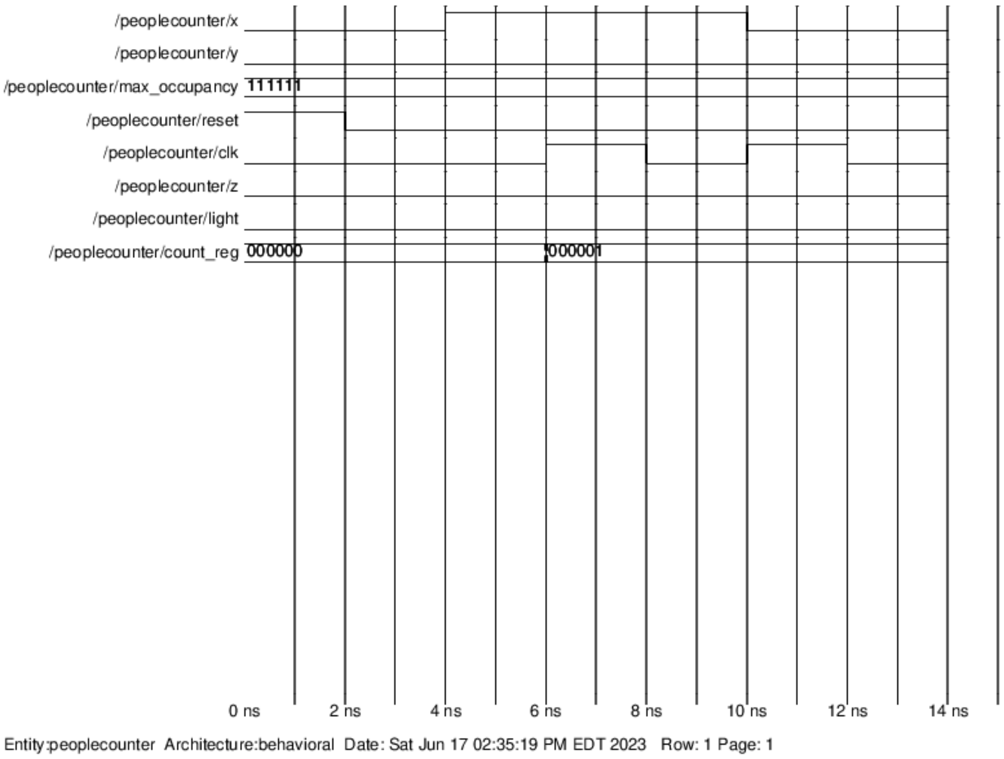
There are multiple situations that can be tested for this task to make sure that it works well or to update it and make it better. However, instead of test benches, I used Do files. Do files list all the actions that the digital system will do. To begin the Do file, I resetted the count to make sure it starts at zero, initialized X and Y to zero too and initialized the max_occupancy signal to “111111” (63) .

For the first situation, I want to test what will happen when one person enters the room and activates one X signal. To do that, the X and clk signals are going to be forced to ‘1’ to show that someone was in front of the photocell. After passing the photocell, the X signal will be zero and so is the clk. That will count for one person entering the room, so count_reg will be “000001” or one. Therefore, the wave chart of the simulation proves that the digital system is functional because the final count_reg is 1 and one person entered the room, so the total number of people in the room should be 1.

1. Do file for the first situation

```
add wave *

force clk 0
force X 0
force Y 0
force Max_Occupancy 111111


force reset 1
run 2
force reset 0
run 2

force X 1
run 2
force clk 1
run 2
force clk 0
run 2
force X 0
force clk 1
run 2
force clk 0
run 2
```

2. Wave graph for the first situation



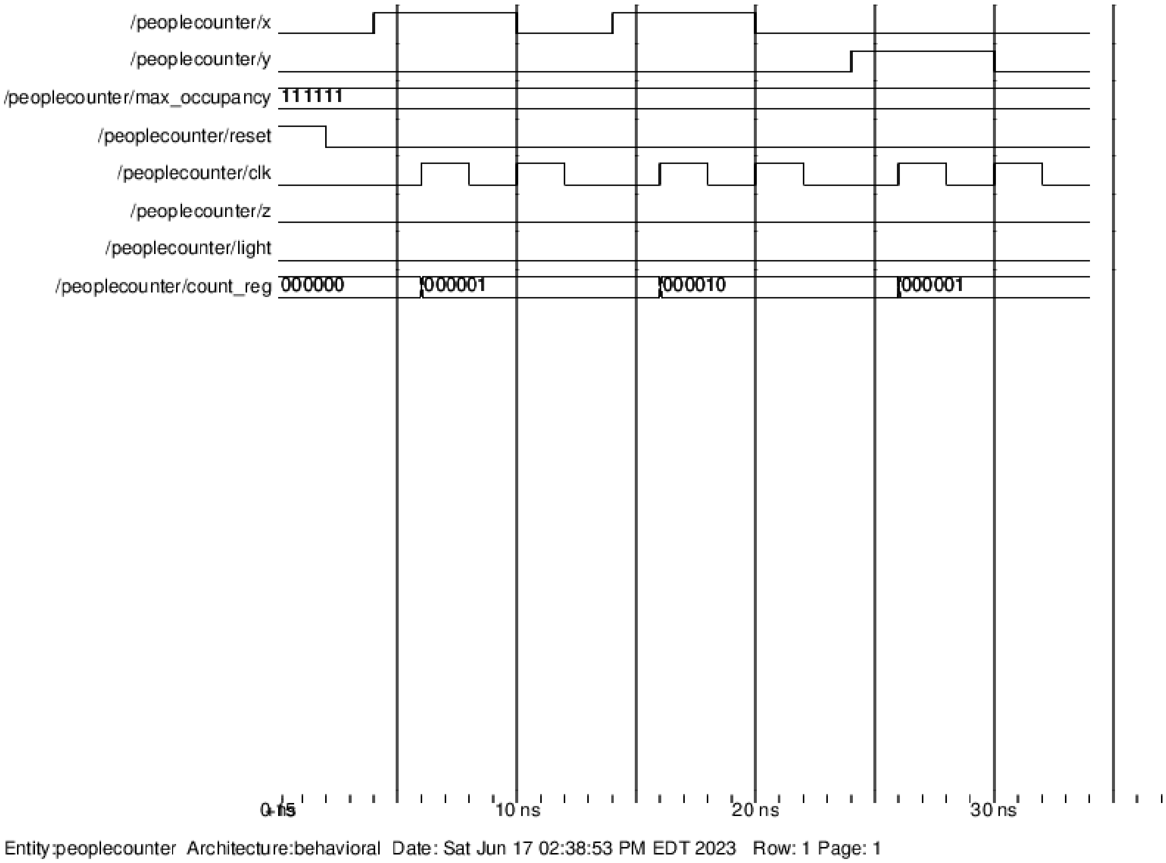
For the second situation, I want to test what will happen when one person leaves the room and activates one Y signal when there are two people in the room. To do that, the Y and clk signals are going to be forced to ‘1’ to show that someone was in front of the photocell. After passing the photocell, the Y and clk signals are going to be set back to ‘0’. However, it will decrement the count_reg that was “000010” will now be “000001”. Therefore, the wave chart of the simulation proves that the digital system works because when someone leaves the room, the system needs to update the count_reg and remove one person. If there were two people in the room and one of them leaves, only one person will remain and that is what the digital system shows.

3. Do file for the second situation

```
add wave *

force clk 0
force X 0
force Y 0
force Max_Occupancy 111111


force reset 1
run 2
force reset 0
run 2

force X 1
run 2
force clk 1
run 2
force clk 0
run 2
force X 0
force clk 1
run 2
force clk 0
run 2

force X 1
run 2
force clk 1
run 2
force clk 0
run 2
force X 0
force clk 1
run 2
force clk 0
run 2

force Y 1
run 2
force clk 1
```

```
run 2
force clk 0
run 2
force Y 0
force clk 1
run 2
force clk 0
run 2
```

4. Wave graph for the second situation



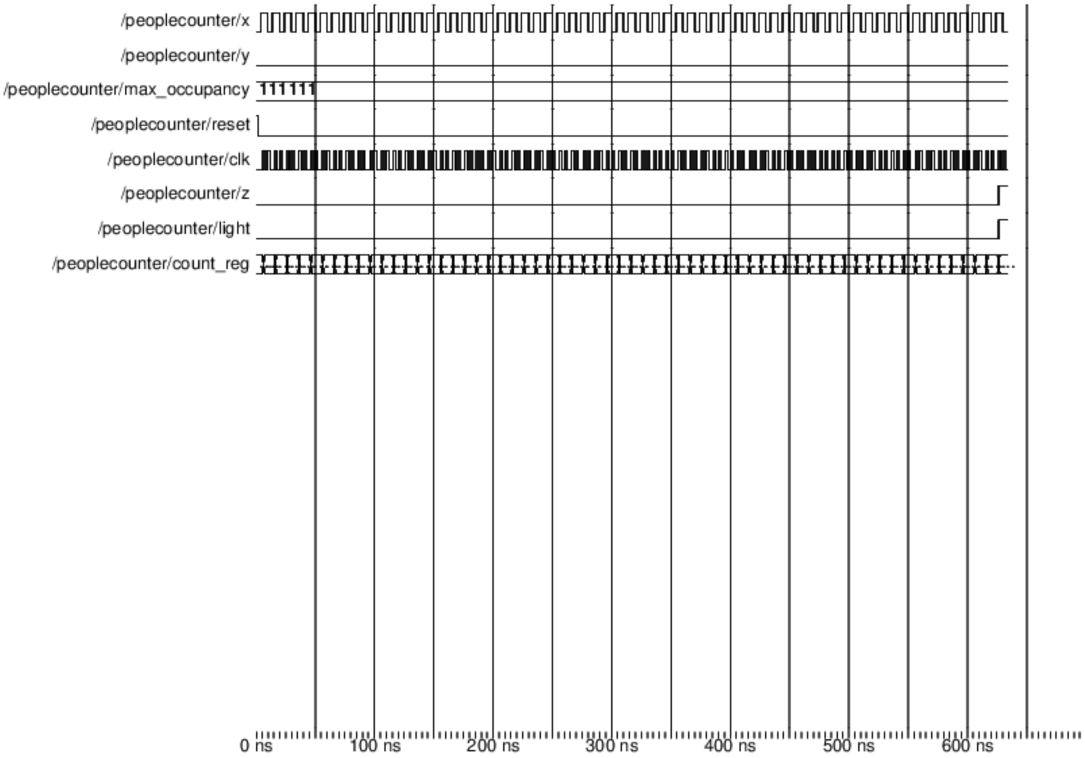
For the third situation, I want to test what will happen when the max_occupancy limit has been reached. To do that, the sequence of the first situation will be repeated 63 times to represent 63 people entering the room and none of them leaving. When 63 or more people enter the room, the red light should be activated. The wave chart of the simulation proves that the digital system works because the light signal rises to ‘1’ when the max_occupancy and the count_reg are equal or over “111111”. That means that when there are more than 63 people in the room the red light opens.

5. Do file for the third situation

```
add wave *

force clk 0
force X 0
force Y 0
force Max_Occupancy 111111


force reset 1
run 2
force reset 0
run 2

force X 1
run 2
force clk 1
run 2
force clk 0
run 2
force X 0
force clk 1
run 2
force clk 0
run 2

force X 1
run 2
force clk 1
run 2
force clk 0
run 2
force X 0
force clk 1
run 2
force clk 0
run 2

force X 1
run 2
force clk 1
run 2
force clk 0
run 2
force X 0
force clk 1
run 2
force clk 0
run 2
```

[...] – 63 times

6. Wave graph for the third situation



Entity:peoplecounter Architecture:behavioral Date: Sat Jun 17 02:44:40 PM EDT 2023 Row: 1 Page: 1

For the fourth situation, I want to test what will happen when more people enter the room after the max_occupancy limit has been reached. To do that, just like in the third situation, the sequence of the first situation will be repeated 63 times. After that, I will add more people in the room and observe what will happen. According to the wave chart of the simulation, the light will be activated but the count_reg will remain at "111111". Therefore, the number of people that are going to be added after the max occupancy will not be recorded.

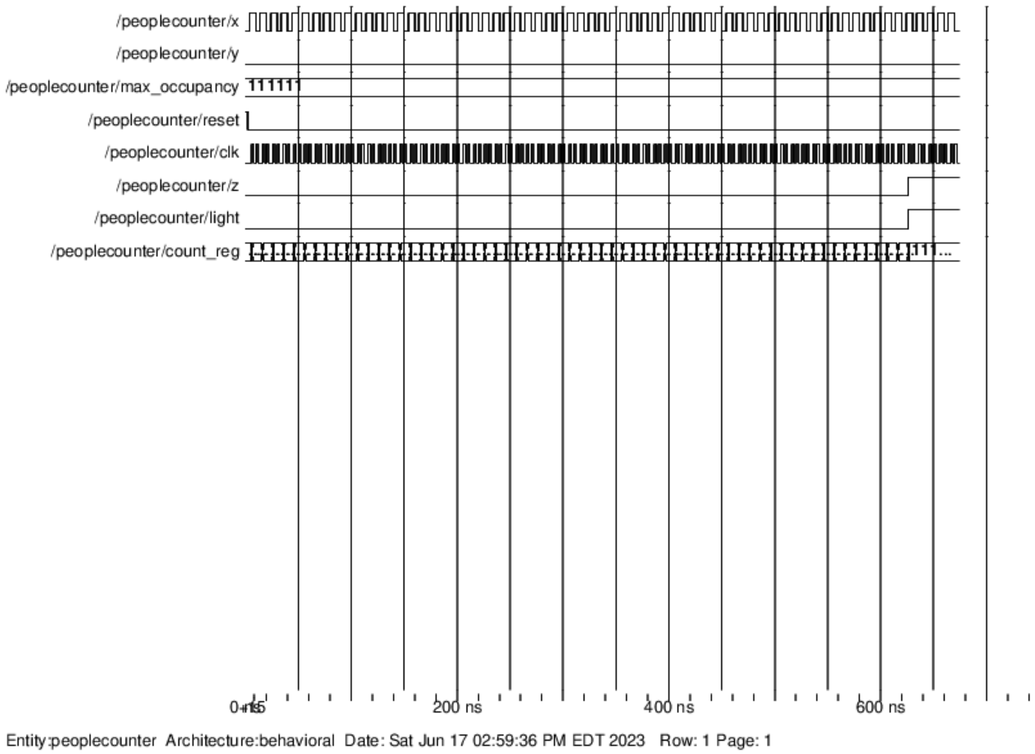
7. Do file for the fourth situation

```
add wave *

force clk 0
force X 0
force Y 0
force Max_Occupancy 111111


force reset 1
run 2
force reset 0
run 2
```

```
force X 1
run 2
force clk 1
run 2
force clk 0
run 2
force X 0
force clk 1
run 2
force clk 0
run 2

force X 1
run 2
force clk 1
run 2
force clk 0
run 2
force X 0
force clk 1
run 2
force clk 0
run 2

force X 1
run 2
force clk 1
run 2
force clk 0
run 2
force X 0
force clk 1
run 2
force clk 0
run 2
```

[...] – 67 times

8. Wave graph for the fourth situation



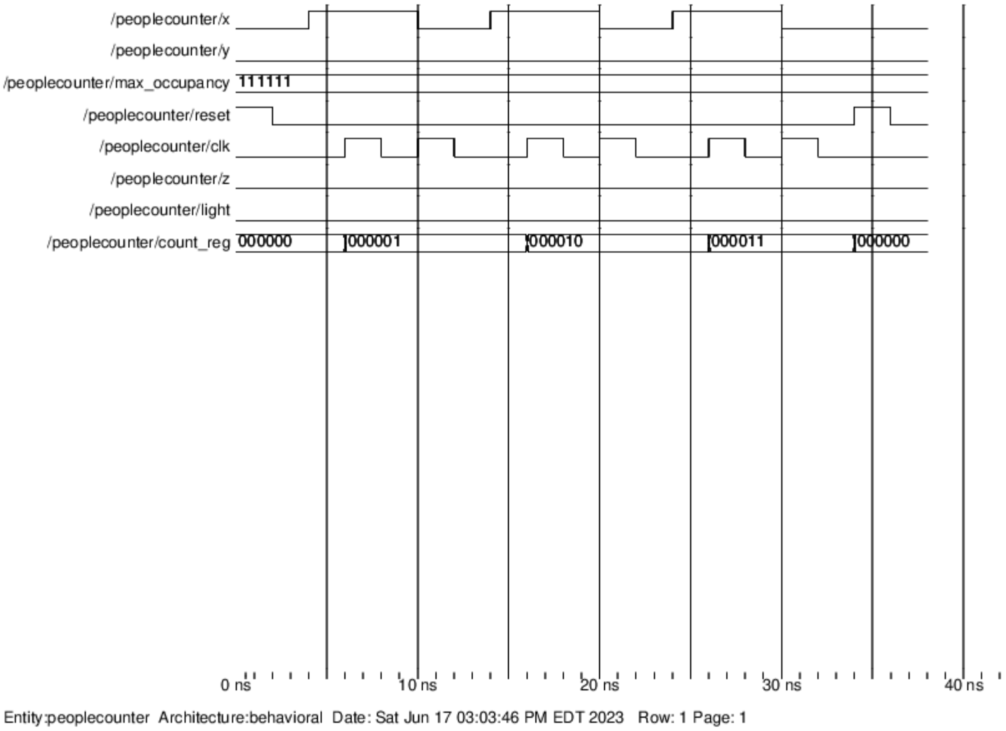
For the fifth situation, I will test the synchronous reset button. To do that, I will add some people in the room. Then, I will force the reset to ‘1’, this is like pressing the button reset. After activating the reset, it should reset the count_reg to “000000”. The wave chart of the simulation proves that the reset button does work. In fact, the count_reg at the end is “000000”, showing that the number of people is zero.

9. Do file for the fifth situation

```
add wave *

force clk 0
force X 0
force Y 0
force Max_Occupancy 111111


force reset 1
run 2
force reset 0
run 2

force X 1
run 2
```

```
force clk 1
run 2
force clk 0
run 2
force X 0
force clk 1
run 2
force clk 0
run 2

force X 1
run 2
force clk 1
run 2
force clk 0
run 2
force X 0
force clk 1
run 2
force clk 0
run 2

force X 1
run 2
force clk 1
run 2
force clk 0
run 2
force X 0
force clk 1
run 2
force clk 0
run 2

force reset 1
run 2
force reset 0
run 2
```

10. Wave graph for the fifth situation



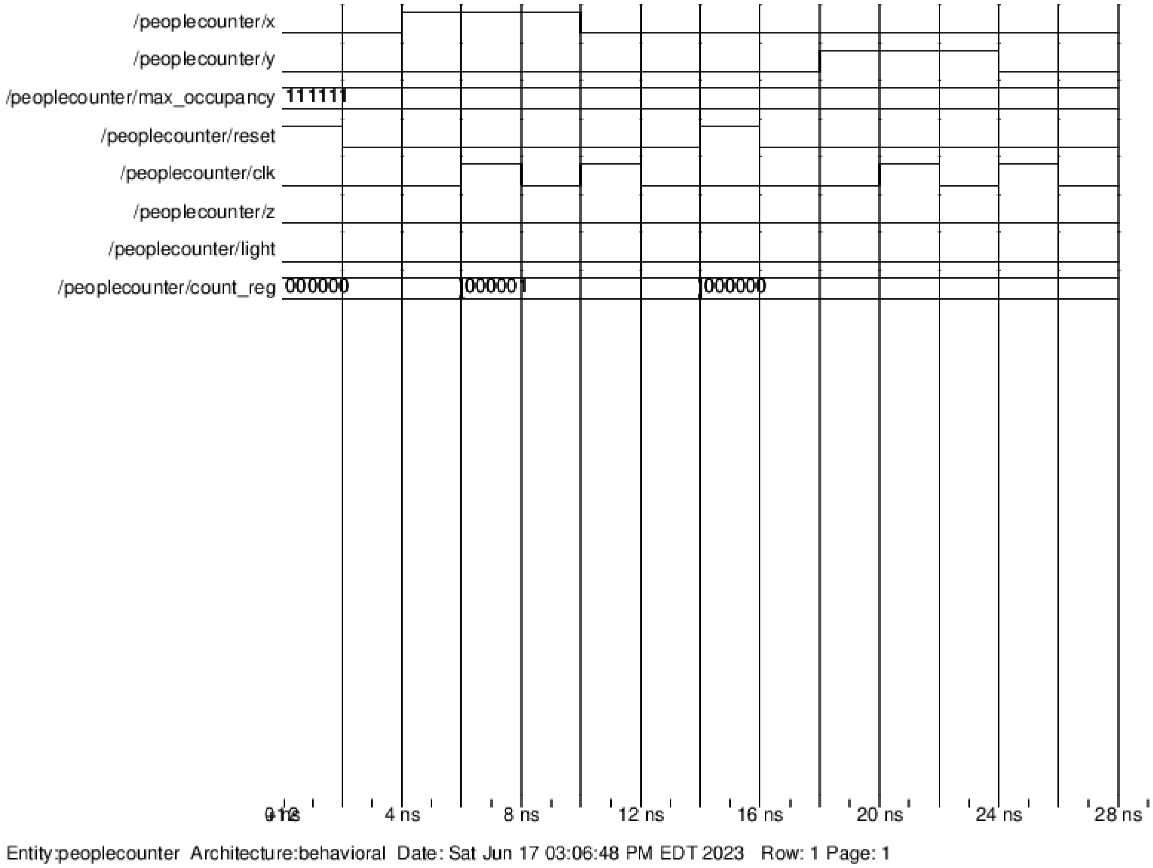
For the sixth situation, I want to test what will happen when the count_reg is "000000" and the Y signal gets activated. That situation could happen if two people enter the room in a way that the X signal gets activated only once or someone resetted count_reg when there were still people in the room. To do that, the synchronous reset will be activated to make sure count_reg is zero. Then, just like in the second situation, activate the Y signal to decrement count_reg. The wave chart of the simulation shows that count_reg remains at "000000" even after removing someone. That is good because it is impossible to have '-1' person in a room.

11. Do file for the sixth situation

```
add wave *

force clk 0
force X 0
force Y 0
force Max_Occupancy 111111


force reset 1
run 2
force reset 0
run 2

force X 1
run 2
```

```
force clk 1
run 2
force clk 0
run 2
force X 0
force clk 1
run 2
force clk 0
run 2

force reset 1
run 2
force reset 0
run 2

force Y 1
run 2
force clk 1
run 2
force clk 0
run 2
force Y 0
force clk 1
run 2
force clk 0
run 2
```

12. Wave graph for the sixth situation



Improvements

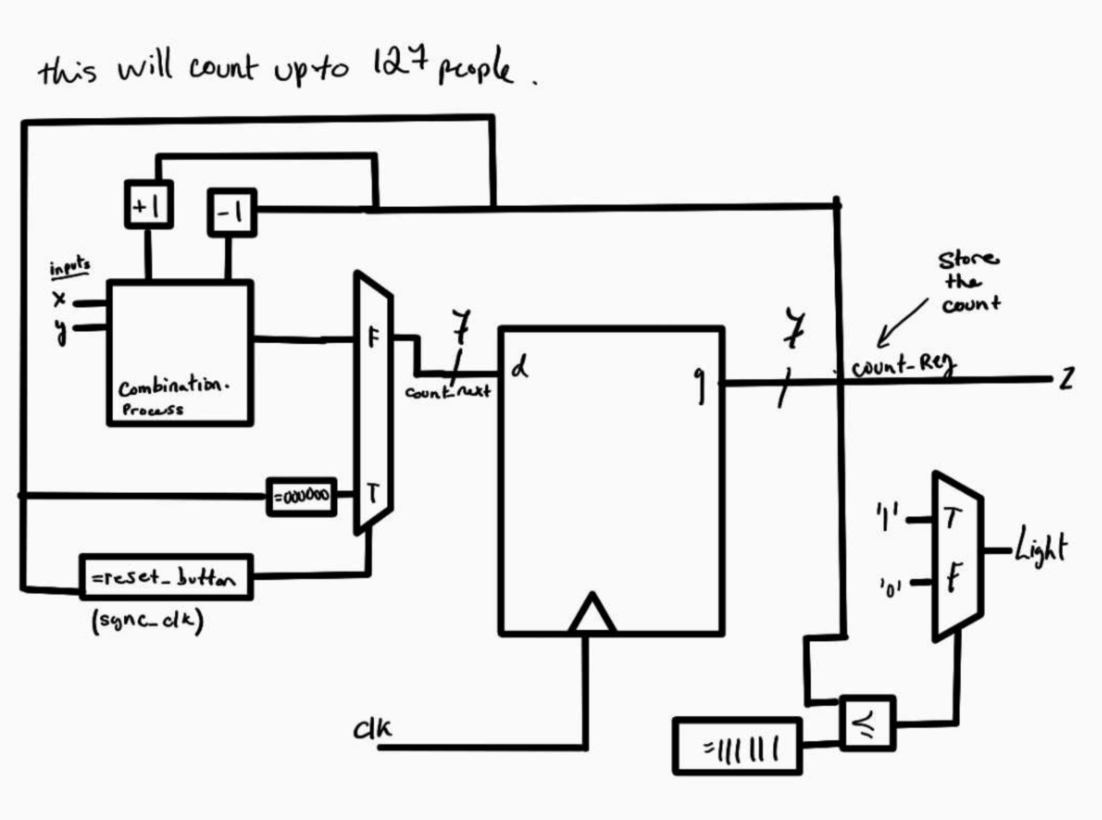
In conclusion, the digital system created to count the amount of people in a room with some constraints works. It accomplishes its tasks to increment when someone enters, decrement when someone leaves, and open a red light when the max occupancy is reached and reset the count whenever someone presses the reset button. However, there are many improvements that can be made to my project. In fact, as mentioned in the fourth test, the digital system doesn't count the amount of people that enter the room after the max occupancy is reached. To fix that, I could increase the amount of bits from 6 bits and keep the max_occupancy mux that will activate the light. Count_reg will continue to update itself even after 63 people in the room.

1. VHDL CODE

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
```

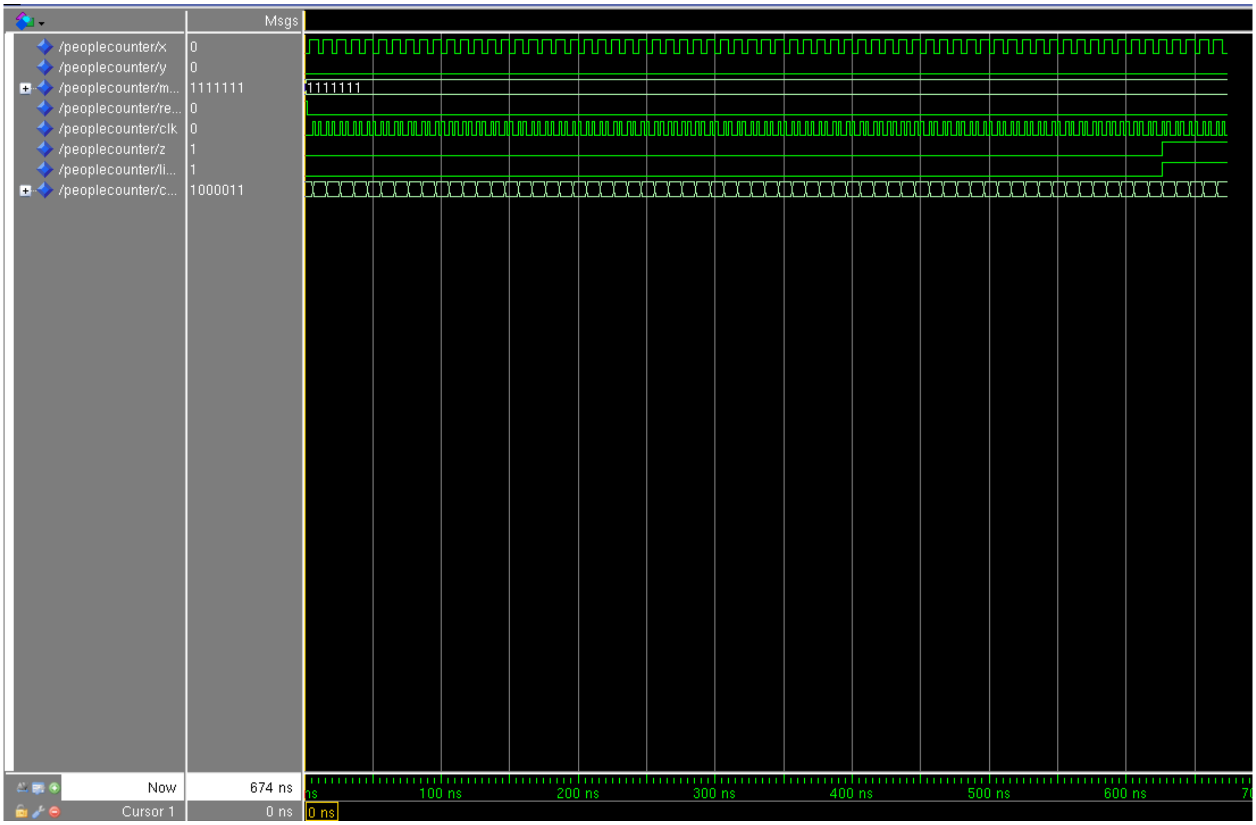
```
entity PeopleCounter is
    port (
    X: in std_logic; -- enters
    Y: in std_logic; -- exits
    Max_Occupancy: in std_logic_vector(6 downto 0); -- maximum occupancy
    Reset: in std_logic; -- synchronous
    clk: in std_logic;
    Z: out std_logic;
    Light: out std_logic -- red light output
    );
end PeopleCounter;

architecture Project of PeopleCounter is
    signal count_reg:std_logic_vector  (6 downto 0) := (others => '0');
    signal count_next: std_logic_vector (6 downto 0) := (others => '0');
    signal count_comb: std_logic_vector (6 downto 0) := (others => '0');
--combinational process signal
    signal Light_reg:  std_logic := '0'; -- signal for red light state
begin

    process (clk, Reset, count_reg)
    begin
    if Reset = '1' then -- synchronous reset
    count_reg <= (others => '0'); -- reset count_reg to “0000000”
    Light_reg <= '0'; -- reset red light state
    elsif (clk'event and clk ='1') then
    count_comb <= count_reg;

    if X = '1' and Y = '0' and count_reg < Max_Occupancy then
        count_reg <= count_reg + 1; -- increment
    elsif X = '0' and Y = '1' and count_reg > 0 then
        count_reg <= count_reg - 1; --decrement
    end if;
    end if;
    end process;

    Z <= '1' when count_reg >= "0111111"  else '0';

    -- Update red light state
    process (count_reg)
    begin
    if count_reg >= "0111111" then
    Light <= '1'; -- turn on red light
    else
    Light <= '0'; -- turn off red light
    end if;
    end process;
end Project;
```

2. Conceptual diagram



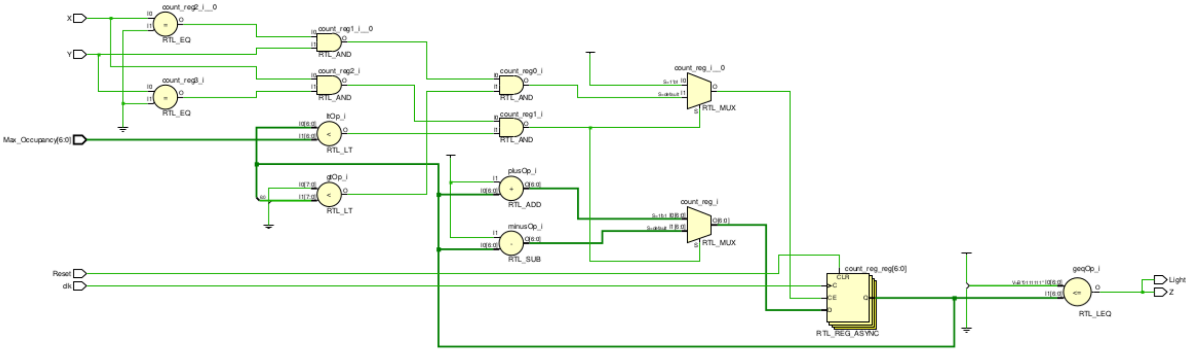
this will count upto 127 people.

3. Wave graph of the new VHDL code



	Msgs
/peoplecounter/x	0
/peoplecounter/y	0
/peoplecounter/m...	1111111
/peoplecounter/re...	0
/peoplecounter/clk	0
/peoplecounter/z	1
/peoplecounter/li...	1
/peoplecounter/c...	1000011
Now	674 ns
Cursor 1	0 ns

4. RTL diagram for the updated VHDL code



REFERENCES

[1] Pong P. Chu., “RTL Hardware Design using VHDL, Coding for Efficiency, Portability, and Scalability” John Wiley & Sons, Inc., 2006.

LOG FILE

```
*** Running vivado
    with args -log PeopleCounter.vds -m64 -product Vivado -mode batch -messageDb vivado.pb -notrace -source
PeopleCounter.tcl


****** Vivado v2018.2 (64-bit)
  **** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018
  **** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

source PeopleCounter.tcl -notrace
Command: synth_design -top PeopleCounter -part xc7a100tcsg324-1
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100t'
INFO: Launching helper process for spawning children vivado processes
INFO: Helper process launched with PID 26806
---------------------------------------------------------------------------------
Starting RTL Elaboration : Time (s): cpu = 00:00:01 ; elapsed = 00:00:02 . Memory (MB): peak = 1401.586 ; gain = 85.828 ; free
physical = 9632 ; free virtual = 21703
---------------------------------------------------------------------------------
INFO: [Synth 8-638] synthesizing module 'PeopleCounter' [/nfs/home/c/c_minhtu/COEN313/Project/Code/project.vhdl:17]
WARNING: [Synth 8-6014] Unused sequential element count_comb_reg was removed.
[/nfs/home/c/c_minhtu/COEN313/Project/Code/project.vhdl:30]
INFO: [Synth 8-256] done synthesizing module 'PeopleCounter' (1#1)
[/nfs/home/c/c_minhtu/COEN313/Project/Code/project.vhdl:17]
---------------------------------------------------------------------------------
Finished RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1446.227 ; gain = 130.469 ; free
physical = 9643 ; free virtual = 21714
---------------------------------------------------------------------------------

Report Check Netlist:
+------+------------------+-------+---------+-------+------------------+
|      |Item              |Errors |Warnings |Status |Description       |
+------+------------------+-------+---------+-------+------------------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |
+------+------------------+-------+---------+-------+------------------+
---------------------------------------------------------------------------------
Start Handling Custom Attributes
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1446.227 ; gain =
130.469 ; free physical = 9642 ; free virtual = 21713
```

```
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1446.227 ; gain =
130.469 ; free physical = 9642 ; free virtual = 21713
---------------------------------------------------------------------------------
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints
Initializing timing engine
Parsing XDC File [/nfs/home/c/c_minhtu/COEN313/Project/Code/projectyes.xdc]
Finished Parsing XDC File [/nfs/home/c/c_minhtu/COEN313/Project/Code/projectyes.xdc]
INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file
[/nfs/home/c/c_minhtu/COEN313/Project/Code/projectyes.xdc]. These constraints will be ignored for synthesis but will be used in
implementation. Impacted constraints are listed in the file [.Xil/PeopleCounter_propImpl.xdc].
Resolution: To avoid this warning, move constraints listed in [.Xil/PeopleCounter_propImpl.xdc] to another XDC file and exclude this
new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1809.973 ; gain = 0.000 ; free
physical = 9314 ; free virtual = 21385
---------------------------------------------------------------------------------
Finished Constraint Validation : Time (s): cpu = 00:00:09 ; elapsed = 00:00:37 . Memory (MB): peak = 1809.973 ; gain = 494.215 ;
free physical = 9453 ; free virtual = 21525
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Loading Part and Timing Information
---------------------------------------------------------------------------------
Loading part: xc7a100tcsg324-1
---------------------------------------------------------------------------------
Finished Loading Part and Timing Information : Time (s): cpu = 00:00:09 ; elapsed = 00:00:37 . Memory (MB): peak = 1809.973 ;
gain = 494.215 ; free physical = 9453 ; free virtual = 21525
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Applying 'set_property' XDC Constraints
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:09 ; elapsed = 00:00:37 . Memory (MB): peak = 1809.973 ;
gain = 494.215 ; free physical = 9455 ; free virtual = 21526
---------------------------------------------------------------------------------
INFO: [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on
the output of the operator [/nfs/home/c/c_minhtu/COEN313/Project/Code/project.vhdl:32]
---------------------------------------------------------------------------------
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:10 ; elapsed = 00:00:37 . Memory (MB): peak = 1809.973 ; gain =
494.215 ; free physical = 9445 ; free virtual = 21517
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start RTL Component Statistics
---------------------------------------------------------------------------------
Detailed RTL Component Info :
+---Adders :
	   2 Input      7 Bit       Adders := 1
+---Registers :
	                7 Bit    Registers := 1
```

```
+---Muxes :
	   2 Input      2 Bit        Muxes := 1
	   2 Input      1 Bit        Muxes := 1
---------------------------------------------------------------------------------
Finished RTL Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
Hierarchical RTL Component report
Module PeopleCounter
Detailed RTL Component Info :
+---Adders :
	   2 Input      7 Bit       Adders := 1
+---Registers :
	                7 Bit    Registers := 1
+---Muxes :
	   2 Input      2 Bit        Muxes := 1
	   2 Input      1 Bit        Muxes := 1
---------------------------------------------------------------------------------
Finished RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Part Resource Summary
---------------------------------------------------------------------------------
Part Resources:
DSPs: 240 (col length:80)
BRAMs: 270 (col length: RAMB18 80 RAMB36 40)
---------------------------------------------------------------------------------
Finished Part Resource Summary
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Cross Boundary and Area Optimization
---------------------------------------------------------------------------------
Warning: Parallel synthesis criteria is not met
---------------------------------------------------------------------------------
Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:10 ; elapsed = 00:00:37 . Memory (MB): peak = 1809.973 ; gain = 494.215 ; free physical = 9433 ; free virtual = 21506
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start Applying XDC Timing Constraints
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:14 ; elapsed = 00:00:47 . Memory (MB): peak = 1809.973 ; gain = 494.215 ; free physical = 9313 ; free virtual = 21386
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Timing Optimization
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Timing Optimization : Time (s): cpu = 00:00:14 ; elapsed = 00:00:47 . Memory (MB): peak = 1809.973 ; gain = 494.215 ; free physical = 9313 ; free virtual = 21386
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start Technology Mapping
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Technology Mapping : Time (s): cpu = 00:00:14 ; elapsed = 00:00:47 . Memory (MB): peak = 1809.973 ; gain = 494.215 ;
free physical = 9313 ; free virtual = 21386
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start IO Insertion
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Flattening Before IO Insertion
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Flattening Before IO Insertion
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Final Netlist Cleanup
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Final Netlist Cleanup
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished IO Insertion : Time (s): cpu = 00:00:15 ; elapsed = 00:00:48 . Memory (MB): peak = 1809.973 ; gain = 494.215 ; free
physical = 9312 ; free virtual = 21385
---------------------------------------------------------------------------------

Report Check Netlist:
+------+------------------+-------+---------+-------+------------------+
|      |Item              |Errors |Warnings |Status |Description       |
+------+------------------+-------+---------+-------+------------------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |
+------+------------------+-------+---------+-------+------------------+
---------------------------------------------------------------------------------
Start Renaming Generated Instances
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Renaming Generated Instances : Time (s): cpu = 00:00:15 ; elapsed = 00:00:48 . Memory (MB): peak = 1809.973 ; gain =
494.215 ; free physical = 9312 ; free virtual = 21385
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start Rebuilding User Hierarchy
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:15 ; elapsed = 00:00:48 . Memory (MB): peak = 1809.973 ; gain =
494.215 ; free physical = 9312 ; free virtual = 21385
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Renaming Generated Ports
```

```
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Renaming Generated Ports : Time (s): cpu = 00:00:15 ; elapsed = 00:00:48 . Memory (MB): peak = 1809.973 ; gain =
494.215 ; free physical = 9312 ; free virtual = 21385
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Handling Custom Attributes
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:15 ; elapsed = 00:00:48 . Memory (MB): peak = 1809.973 ; gain =
494.215 ; free physical = 9312 ; free virtual = 21385
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Renaming Generated Nets
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Renaming Generated Nets : Time (s): cpu = 00:00:15 ; elapsed = 00:00:48 . Memory (MB): peak = 1809.973 ; gain =
494.215 ; free physical = 9312 ; free virtual = 21385
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Writing Synthesis Report
---------------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-------+------+
|      |Cell   |Count |
+------+-------+------+
|1     |BUFG   |     1|
|2     |CARRY4 |     3|
|3     |LUT1   |     2|
|4     |LUT2   |     8|
|5     |LUT4   |     7|
|6     |LUT5   |     1|
|7     |LUT6   |     2|
|8     |FDCE   |     7|
|9     |IBUF   |    11|
|10    |OBUF   |     2|
+------+-------+------+

Report Instance Areas:
+------+---------+-------+------+
|      |Instance |Module |Cells |
+------+---------+-------+------+
|1     |top      |       |    44|
+------+---------+-------+------+
---------------------------------------------------------------------------------
Finished Writing Synthesis Report : Time (s): cpu = 00:00:15 ; elapsed = 00:00:48 . Memory (MB): peak = 1809.973 ; gain = 494.215
; free physical = 9312 ; free virtual = 21385
---------------------------------------------------------------------------------
Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:09 ; elapsed = 00:00:18 . Memory (MB): peak = 1809.973 ; gain = 130.469 ;
free physical = 9367 ; free virtual = 21440
Synthesis Optimization Complete : Time (s): cpu = 00:00:15 ; elapsed = 00:00:48 . Memory (MB): peak = 1809.973 ; gain = 494.215
; free physical = 9377 ; free virtual = 21450
INFO: [Project 1-571] Translating synthesized netlist
INFO: [Netlist 29-17] Analyzing 14 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
```

```
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis
15 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:16 ; elapsed = 00:00:49 . Memory (MB): peak = 1809.973 ; gain = 506.840 ; free physical =
9364 ; free virtual = 21437
WARNING: [Constraints 18-5210] No constraint will be written out.
INFO: [Common 17-1381] The checkpoint
'/nfs/home/c/c_minhtu/COEN313/Project/Code/project_1/project_1.runs/synth_1/PeopleCounter.dcp' has been generated.
INFO: [runtcl-4] Executing : report_utilization -file PeopleCounter_utilization_synth.rpt -pb PeopleCounter_utilization_synth.pb
report_utilization: Time (s): cpu = 00:00:00.05 ; elapsed = 00:00:00.10 . Memory (MB): peak = 1809.973 ; gain = 0.000 ; free
physical = 9365 ; free virtual = 21438
INFO: [Common 17-206] Exiting Vivado at Sat Jun 17 16:16:57 2023...
```