Title: Schematic and Layout Design of a CMOS Logic Gate Using Universal Gates

Abstract: This report presents the schematic and layout design of a CMOS logic gate implementing the function F={(S1′·OP1·S2′)·OP2·S3′}′ F ={(S1′·OP1·S2′)·OP2·S3′}′ using universal gates, specifically NAND gates. The design and verification processes were conducted using the Cadence EDA tool suite. The report demonstrates the successful completion of the design, layout, and verification, including Design Rule Check (DRC) and Layout versus Schematic (LVS), validating the effective use of universal gates in implementing complex logical functions.

Introduction: Universal gates, such as NAND and NOR, are fundamental in digital logic design due to their ability to implement any logic function. This experiment involves designing the logical function F={(S1′·OP1·S2′)·OP2·S3′}′ F={(S1′·OP1·S2′)·OP2·S3′}′ using NAND gates in CMOS technology. By leveraging the universality of NAND gates, the function is efficiently realized with minimal components, optimized for performance in VLSI circuits.

Theory: The target logic function FFF consists of AND and OR operations combined with NOT operations on inputs S1S_1S1, OP1OP_1OP1, S2S_2S2, OP2OP_2OP2, and S3S_3S3. The use of NAND gates to implement the entire function underscores their versatility in CMOS technology. NAND gates, which consist of complementary NMOS and PMOS transistors, can perform all the required logic operations when arranged appropriately.

In CMOS logic:

- Pull-down network: NMOS transistors in series provide the AND functionality.
- Pull-up network: PMOS transistors in parallel implement the OR and NOT functions. NAND gates are used to create the necessary logic for the function, simplifying the design process while maintaining efficiency.

Apparatus:

- Cadence Virtuoso Schematic Editor XL
- Cadence Virtuoso Layout Editor XL
- 45nm CMOS technology node

Methodology:

1. Schematic Design:
    - The function F={(S1′·OP1·S2′) ·OP2·S3′}′ F={(S1′·OP1·S2′)·OP2·S3′}′ is implemented using CMOS NAND gates in the Cadence Virtuoso Schematic Editor.
    - Inputs S1S_1S1, OP1OP_1OP1, S2S_2S2, OP2OP_2OP2, and S3S_3S3 are connected following the Boolean expression.
    - Proper transistor sizing is applied to the NMOS and PMOS transistors to ensure optimal performance.
2. Stick Diagram:
    - A stick diagram is created to visualize the layout design, using the following color scheme:
        - Green for polysilicon,
        - Brown for p-diffusion,
        - Dark brown for n-diffusion,
        - Light blue for Metal1,
        - Dark blue for Metal2,
        - Black cross for contacts and vias.
    - The source and drain terminals for both NMOS and PMOS transistors are labeled to simplify the layout design process.
3. Layout Design:
    - A layout cell is created for the function FFF using Cadence Virtuoso Layout Editor.
    - NMOS and PMOS transistors are placed in accordance with the stick diagram and the schematic.
    - Metal1 is used for vertical routing, while Metal2 handles horizontal connections, ensuring a compact design.
    - Design Rule Check (DRC) is run to ensure that the layout meets the technology's design rules for metal width and spacing.

4. Verification:
    - Design Rule Check (DRC): Ensures compliance with technology-specific design rules.
    - Layout versus Schematic (LVS): Verifies that the layout matches the schematic's netlist.
    - Transient Simulation: The function is simulated under different input conditions to confirm the expected logic behavior and evaluate performance metrics like delay and power.

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Simulation and Results:

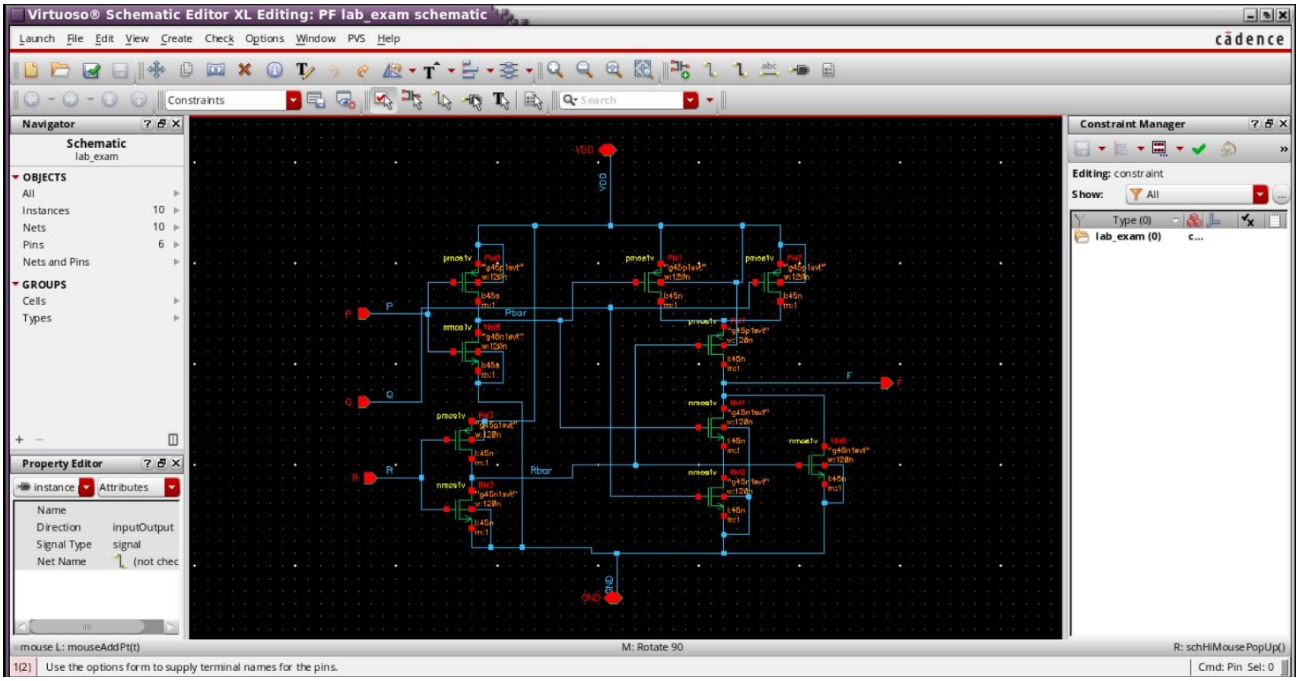

Figure-01: Schematic Diagram

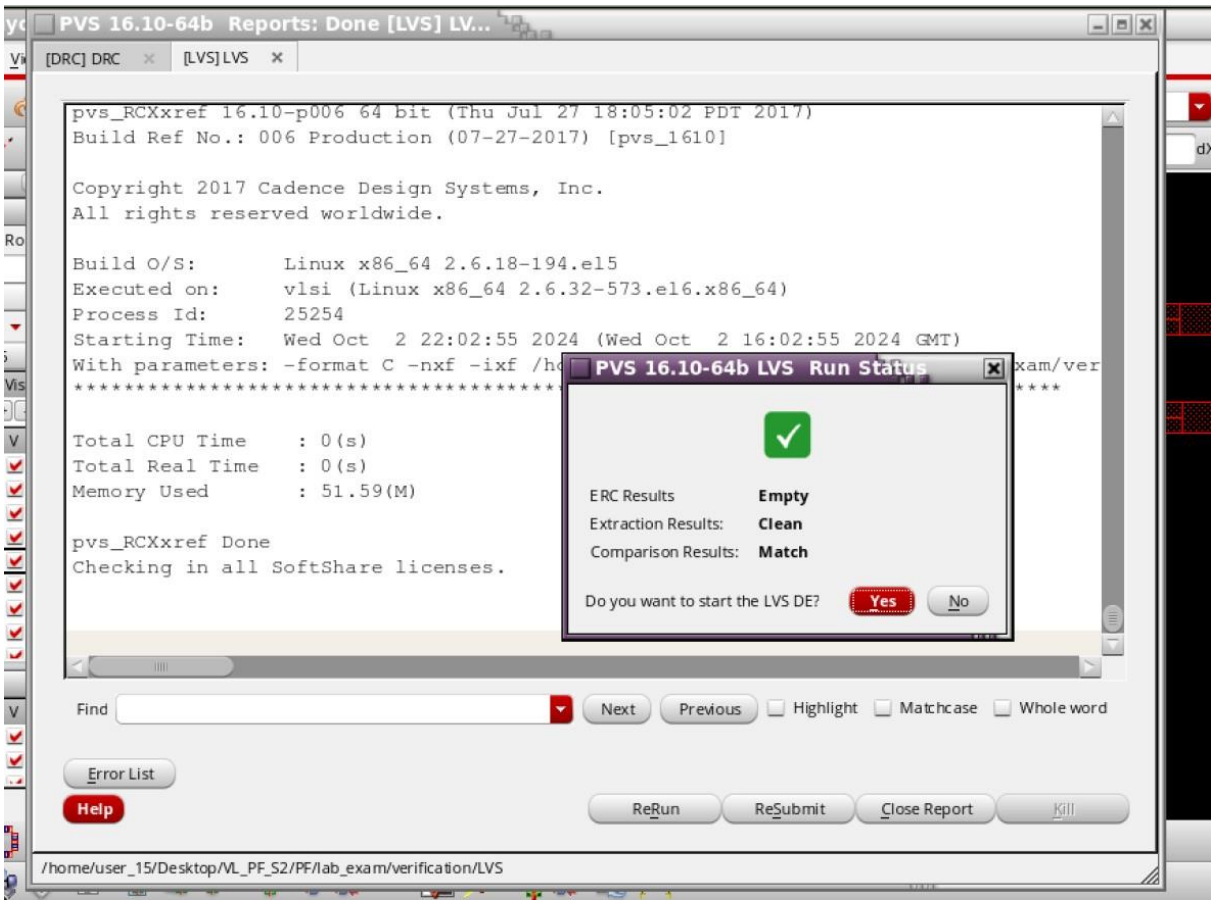

Figure-03: LVS Verification

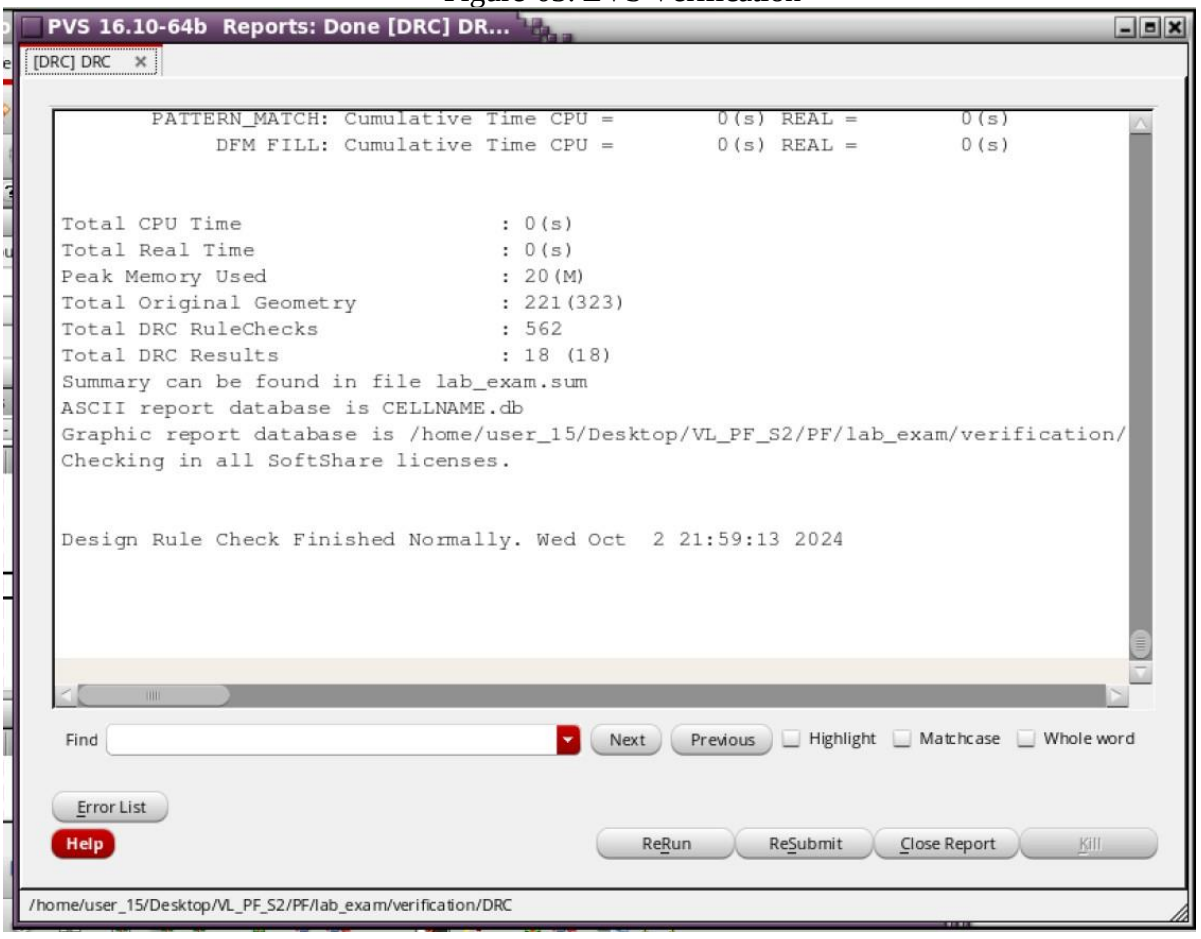

Figure-04: DRC Verification

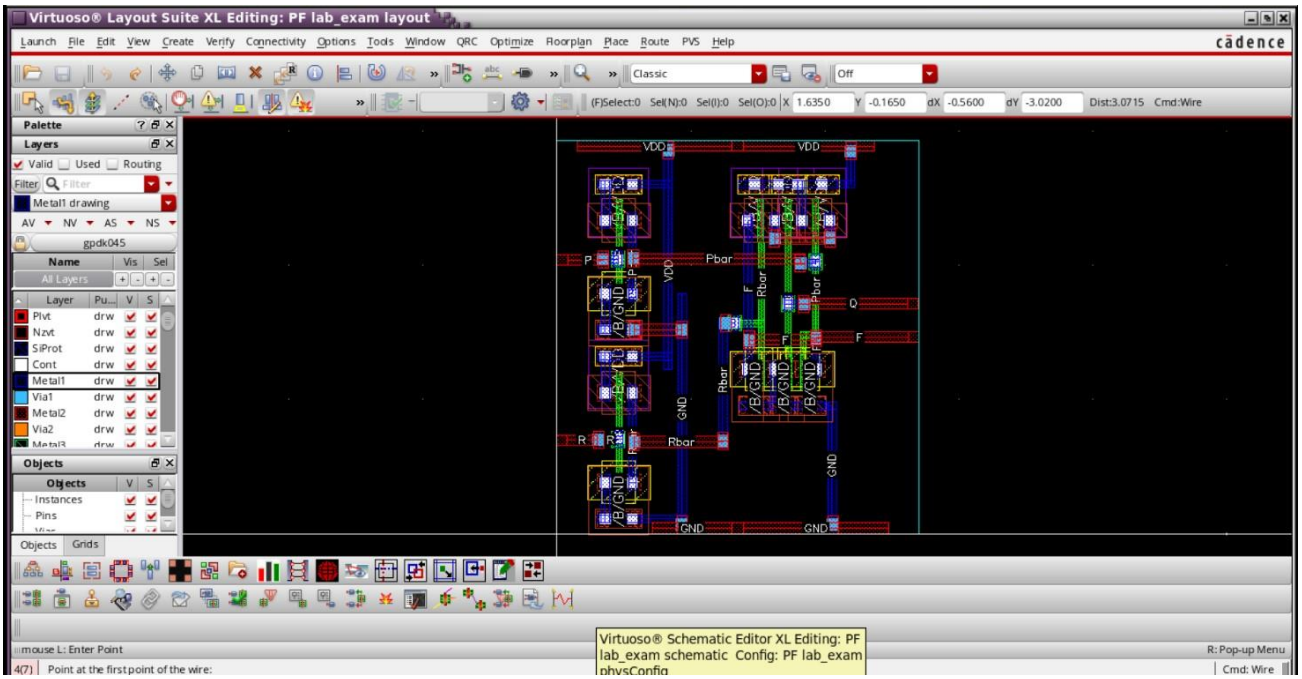

Figure-05: Physical Layout

Conclusion:

The function F={(S1′·OP1·S2′)·OP2·S3′}F={(S1′·OP1·S2′)·OP2·S3′}′ was successfully designed and verified using CMOS NAND gates. The DRC and LVS results confirm that the layout adheres to the required design rules, while transient simulation validates the correct functionality of the logic gate. This report demonstrates the effectiveness of universal gates in implementing complex logic functions in VLSI design.

References:

1. Rabaey, J. M., Chandrakasan, A., & Nikolic, B. (2003). *Digital Integrated Circuits: A Design Perspective*. Prentice Hall.
2. Weste, N. H. E., & Harris, D. (2010). *CMOS VLSI Design: A Circuits and Systems Perspective*. Addison-Wesley.