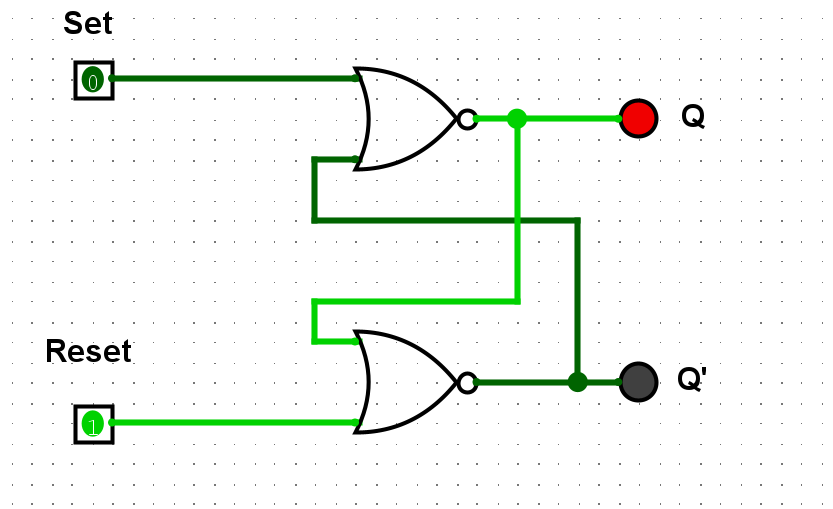
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Unit: Computer System Cos10004

Part 1:

6. S-R Flip-Flop



|  |  |  |  |
| --- | --- | --- | --- |
| Set | Reset | Q | Q’ |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 |

7. When one of the inputs is 1, the circuit produces the same answer as the D\_Flipflop. However, because of using the NOR gate, the circuit will follow the pin 0. This is useful because the other pin is able to change without changing the result.

8. When both the Set and the Reset are 1, the S\_R Flipflop will be undefined state. This eventually becomes the issue when flipflop mission is to complement each other.

10. D-Flipflop

Diagram, schematic

Description automatically generated

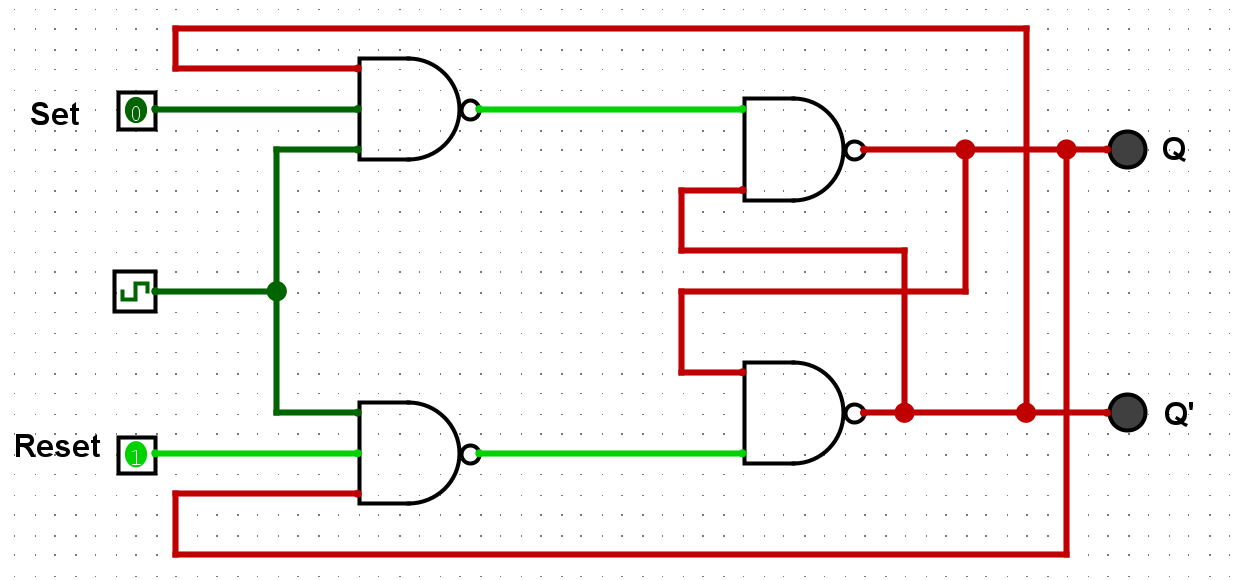
|  |  |  |  |
| --- | --- | --- | --- |
| Clock | Pin | Q | Q’ |
| 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |

11. The D\_Flipflop only uses one data input and one clock. The output Q is set up to be on when the data input is on.

12. The clock is used to control the whole operation. When the clock is LOW, there will be no effect to the output Q. When the clock is HIGH, it acts like a data pin and have an effect on the output Q.

13. The D Flipflop only has one input pin while the S-R Flipflop has two input pins. Also, the S-R can have two outputs LOW at the same time, which is not safe.

15.

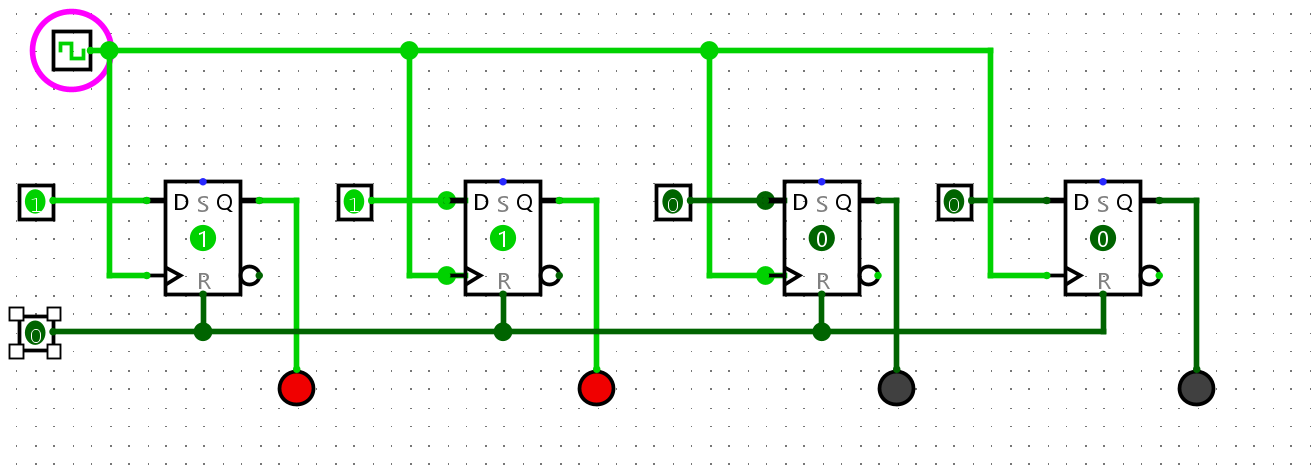


|  |  |  |  |
| --- | --- | --- | --- |
| J | K | Q | Q’ |
| 0 | 0 | 1 no change | 0 |
| 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 1 | 1-0 toggle | 0-1 |

16. J-K Flipflop can be converted into D Flipflop by driving the J and K input with the D input with a NOT gate.

17. J\_K Flipflop can be made to behave like to Toggle when both inputs J and K is 1.

18. Registers

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|  |  |  |
| --- | --- | --- |
| Ox | Input Binary | Output Binary |
| 0 | 0000 | 0000 |
| 1 | 0001 | 0001 |
| 2 | 0010 | 0010 |
| 3 | 0011 | 0011 |
| 4 | 0100 | 0100 |
| A | 1010 | 1010 |
| B | 1011 | 1011 |
| C | 1100 | 1100 |
| D | 1101 | 1101 |
| E | 1110 | 1110 |
| F | 1111 | 1111 |