Unit: COS10004

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1. Little-endian 3-bit ripple counter

Diagram

Description automatically generated

1. Little-endian count down counter

Diagram

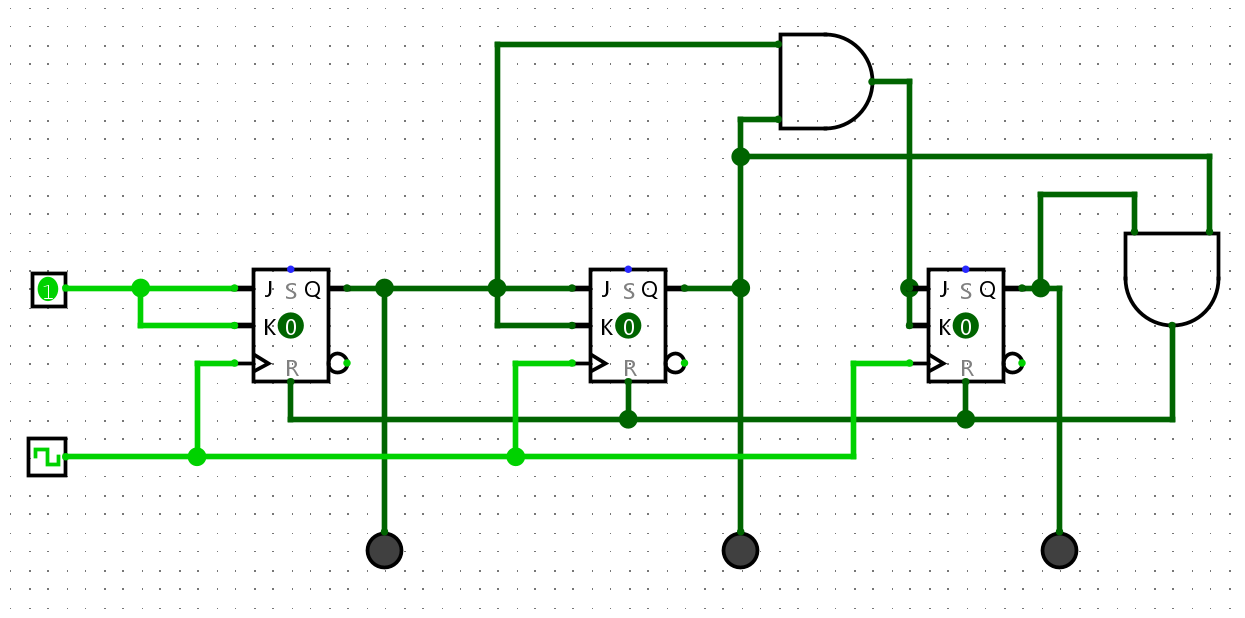
Description automatically generated

7. Common clock counter

Diagram, schematic

Description automatically generated

9. Common clock counts to 5 (MOD 6) with illegal state



10. HEX digit display no illegal state anymore

10.2 Without the D-flipflop, the circuit occurs illegal condition. At the time when the clock pulses, the Hex Display eventually counts to 6 but it happens to quickly. With the D flipflop, which means the Delay Flipflop and some logic gate (AND gate) the bits are now stored when the clock pulses. Consequently, the circuit would be more effective and more predictable for the user to use it.

