CCSU FALL 2024 Van Nguyen

CET_453

LAB 04 _ CLOCK

Goal

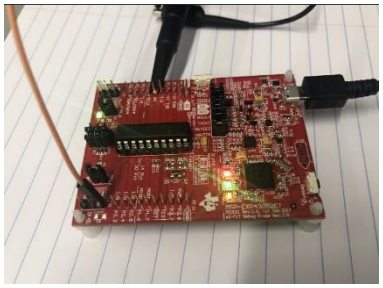
The goal of this lab is to observe the difference clock sources and signals available in a microcontroller and see how they can be used with various options.

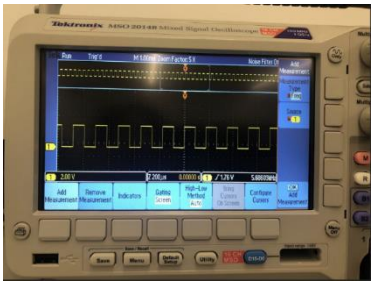
Tools

MSG430G2553 based development board

IAR Embedded Workbench

2-Channel Oscilloscope





Reference Information

MCLK / 10 is able to be measured on P1.1. (If MCLK is running at 1MHz, you will measure 100Khz)

SMCLK is able to be measured on P1.4.

ACLK is able to be measured on P1.0.

MCLK Source Config (for the MSP430G2553)

SELM_0	DCO
SELM_1	DCO
SELM_2	VLO (or LFXT1CLK)
SELM_3	VLO (or LFXT1CLK)

SMCLK Source Config (for the MSP430G2553)

SELS_0	DCO
SELS_1	VLO (or LFXT1CLK)

MCLK Divider Config

DIVM_0	1
DIVM_1	2
DIVM_2	4
DIVM_3	8

SMCLK Divider Config

DIVS_0	1
DIVS_1	2
DIVS_2	4
DIVS_3	8

ACLK Divider Config

DIVA_0	1
DIVA_1	2
DIVA_2	4
DIVA_3	8

The MSP430 addresses the conflicting demands for high performance, low power, and a precise frequency by using three internal clocks, which can be derived from up to four sources. These are the internal clocks, which are the same in all devices:

- ✓ **Master clock, MCLK**, is used by the CPU and a few peripherals.
- ✓ **Subsystem master clock, SMCLK**, is distributed to peripherals.
- ✓ **Auxiliary clock, ACLK**, is also distributed to peripherals.

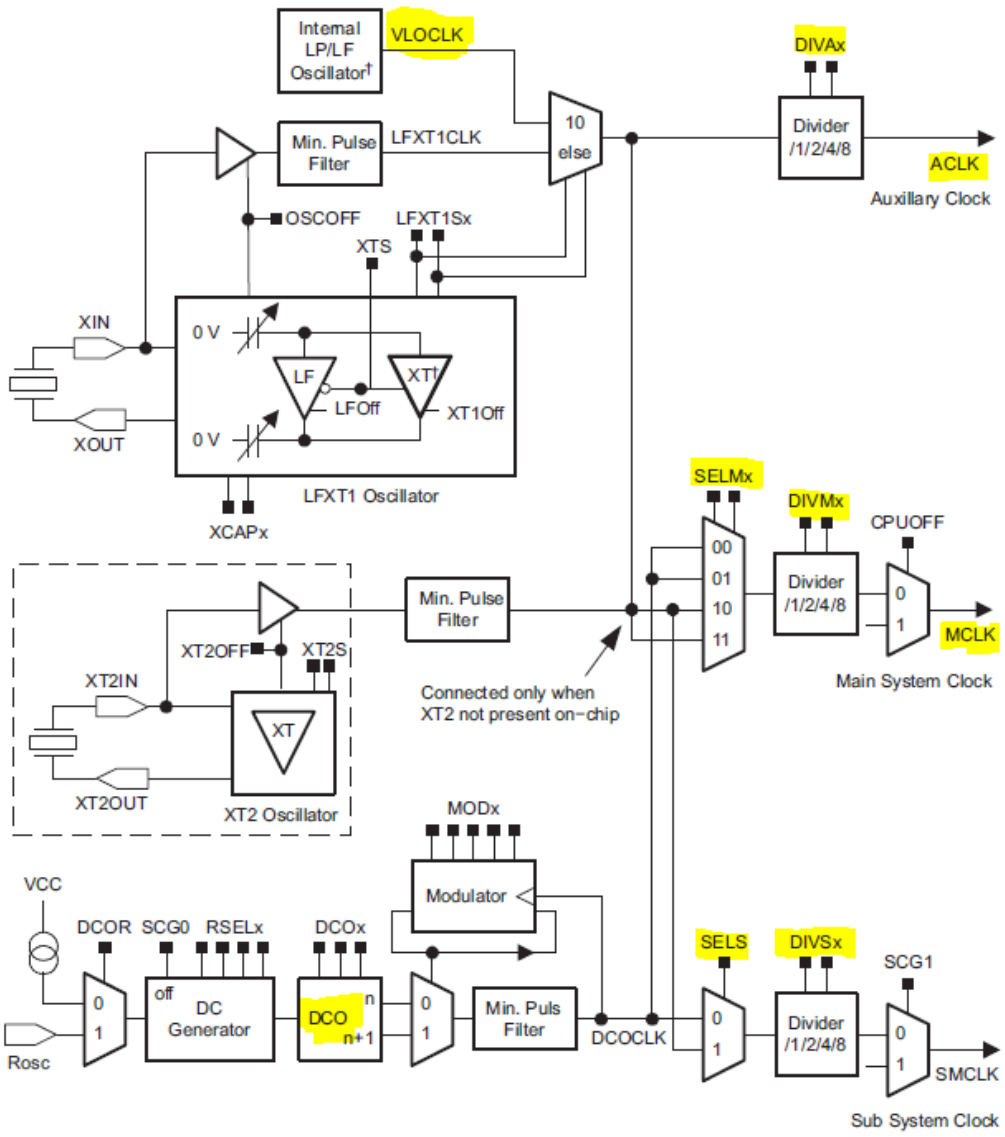
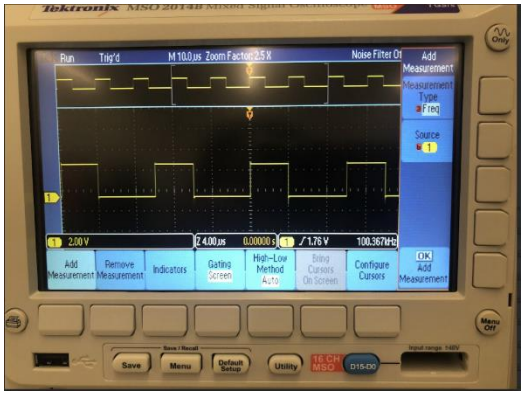


Figure 1

1. Describe how the clock signals are configured . Measure the clock outputs on the oscilloscope and describe the frequencies each clock is running at. (Reminder, MCLK is running at 10x the value measured).

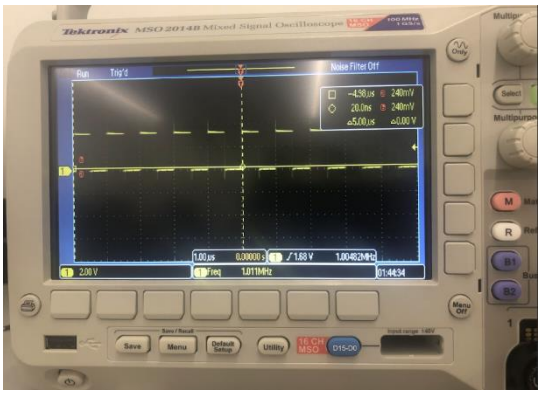
   MCLK:

   - Configuration: *Example, Clock source is DCU @ 1MHz, with no division*
   - Expected Results: *1MHz*
   - Measured Results: 100kHz (1MHz / 10)
   - Scope Capture:



   SMCLK:

   - Configuration: positive on p1.4 , negative on ground
   - Expected Results: *1MHz*
   - Measured Results: *1MHz*
   - Scope Capture:



ACLK:

- Configuration: positive on p1.0 , negative on ground
- Expected Results : 12 kHz
- Measured Results : 10.48 kHz
- Scope Capture:

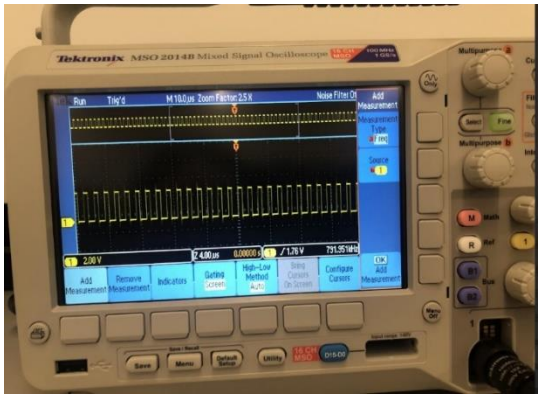
2. Modify the code and create a different frequency for each clock signal. Describe the changes made to the code (including values and registers), what their effect should be, and what their effect was. Show a screen capture of the oscilloscope.

MCLK:

- Code Changes and resulting configuration:

```
SetupDCO    mov.b   &CALBC1_8MHZ,&BCSCTL1   ; Set DCO to 1MHz
            mov.b   &CALDCO_8MHZ,&DCOCTL
```

-
- Changed from 1 MHz to 8 MHz
- Expected Results: 8 MHz
- Measured Results: 791.95 kHz (8 MHz / 10)
- Scope Capture:

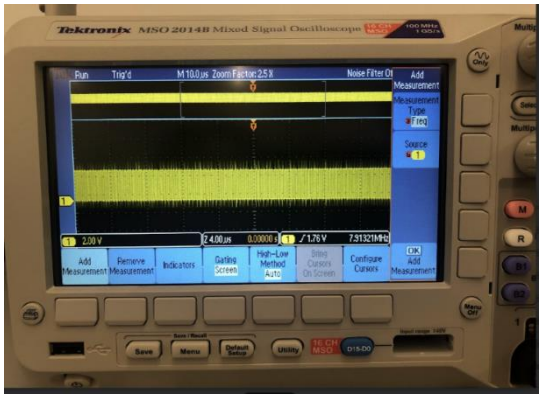


SMCLK:

- Code Changes and resulting configuration:

```
SetupDCO    mov.b   &CALBC1_8MHZ,&BCSCTL1    ; Set DCO to 1MHz
            mov.b   &CALDCO_8MHZ,&DCOCTL
```

-
- Changed from 1 MHz to 8 MHz (SMCLK does not get divided)
- Expected Results : 8MHz
- Measured Results : 7.91 MHz
- Scope Capture:

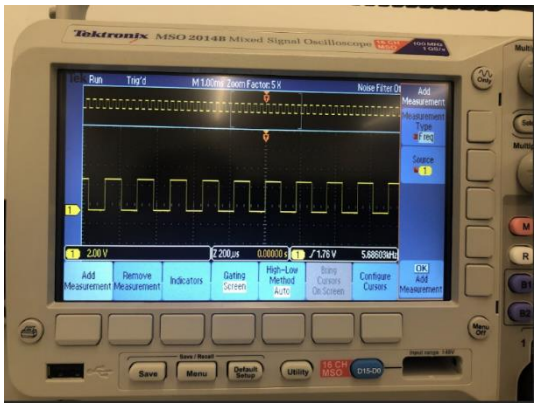


ACLK:

- Code Changes and resulting configuration:

```
SetupACLK   bis.b   #DIVA_1, &BCSCTL1          ; [DIVA] DIVIDER FOR ACLCK = 1 (100%)
```

-
- Changed divider variable to divide 12 kHz / 2 = 6 kHz
- Expected Results: 6 kHz
- Measured Results: 5.69 kHz
- Scope Capture:



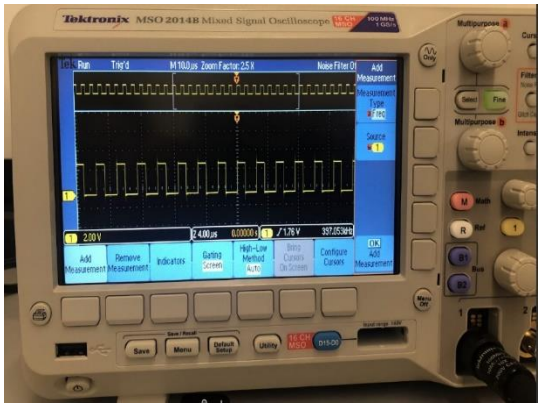
3. Modify the code again and create a different set of frequencies for each clock signal. . Describe the changes made to the code, what their effect should be, and what their effect was. Show a screen capture of the oscilloscope.

MCLK:

- Code Changes and resulting configuration:

```
SetupMCLK   bis.b   #SELM_1, &BCSCTL2          ; [SELM] CLOCK SOURCE FOR MCLK = DCO
            bis.b   #DIVM_1, &BCSCTL2          ; [DIVM] DIVIDER FOR MCLK = 1 (100%)
```

-
- Changed divider variable to divide 8 MHz /10 =800kHz/ 2 =400kHz
- Expected Results : 400 kHz
- Measured Results : 397.1 kHz
- Scope Capture:

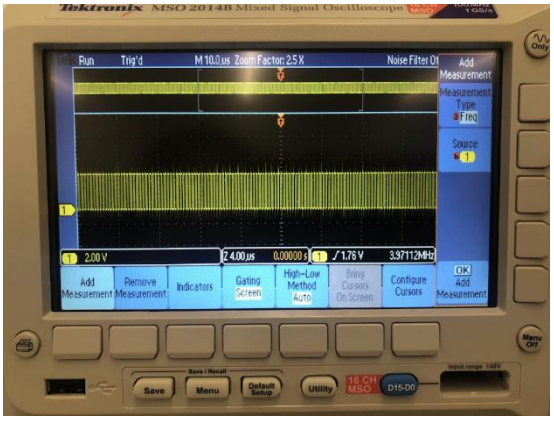


SMCLK:

- Code Changes and resulting configuration:

```
SetupSMCLK  bis.b   #SELS_0, &BCSCTL2          ; [SELS] CLOCK SOURCE FOR SMCLK = DCO
            bis.b   #DIVS_1, &BCSCTL2          ; [DIVS] DIVIDER FOR SMCLK = 1 (100%)
```

-
- Changed divider variable to divide 8 MHz /2 = 4 MHz
- Expected Results : 4 MHz
- Measured Results : 3.96 MHz
- Scope Capture:



ACLK:

- Code Changes and resulting configuration:

```
SetupACLK   bis.b   #DIVA_2, &BCSCTL1          ; [DIVA] DIVIDER FOR ACLCK = 1 (100%)
```

-
- Changed divider variable to divide 12 kHz/ 4 = 3 kHz
- Expected Results : 3 kHz
- Measured Results : 2.73 kHz
- Scope Capture: