TUTORIAL: QSYS CUSTOM ST COMPONENT

Goal

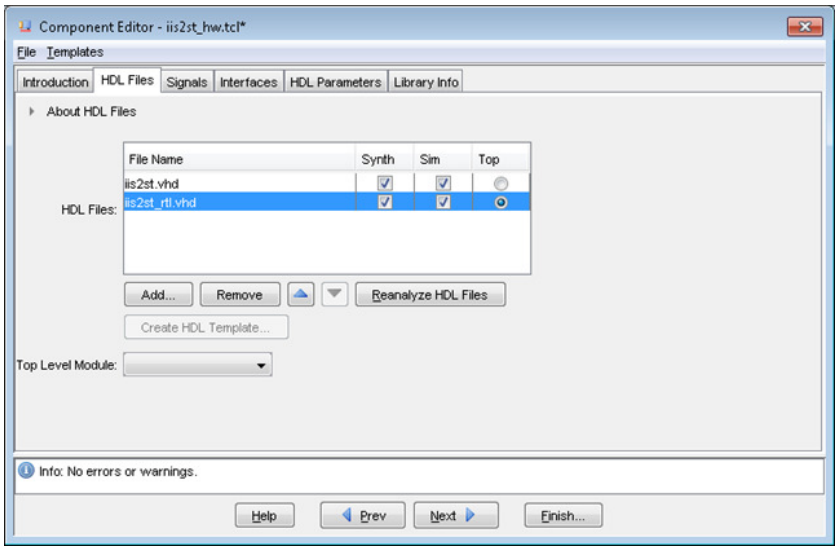
Create a custom component in Qsys with an ST Interface.

Prerequisites

- Quartus
- You must be familiar with Qsys.

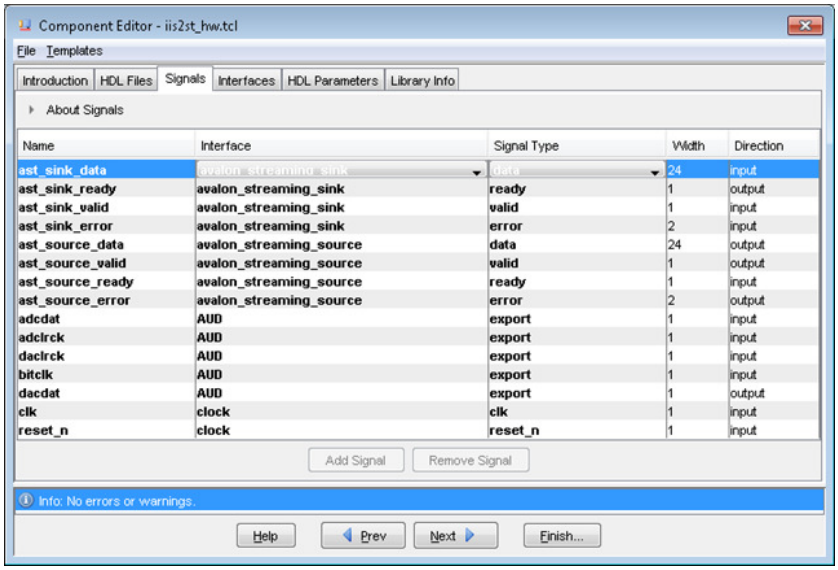
How To Do It

A) With Qsys open, press "new" in the "Component Library" panel to the left. This opens the following dialog:

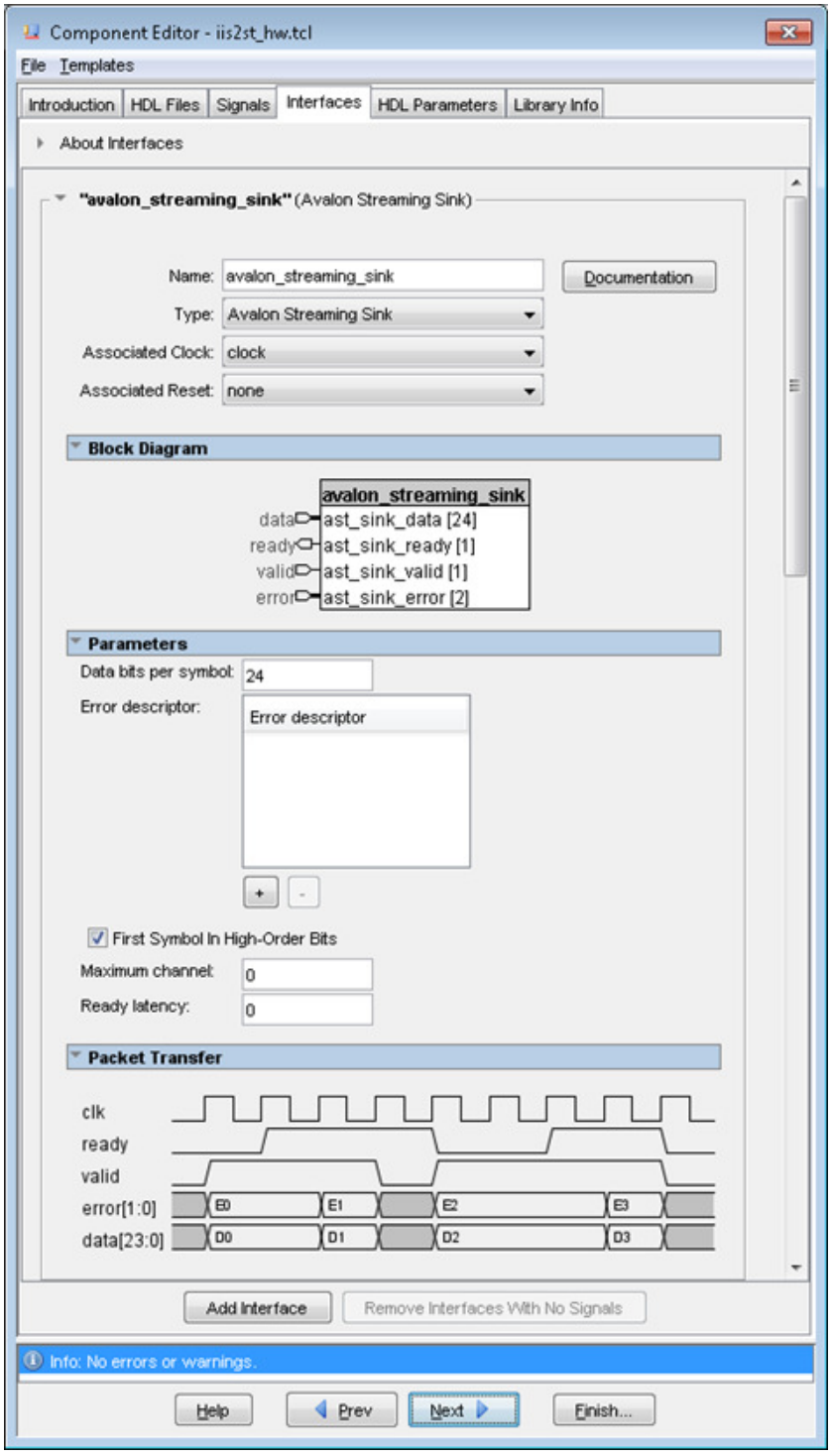


Add your hdl files and let it analysed. If analysis fails, you should go back to ModelSim and debug your code. Ensure that your interfaces are correct, that you have no unresolved generics and that the code can be syntehsized (no test becnh constructions). The figure above shows two files, the "iis2st.vhd" contains the actual code, whereas the iis2st_rtl.vhd only wraps it and selects the appropriate architecture and sets the value of the generics in iis2st.vhd.

B) Identify the interfaces. The next page lets you assign the design entity ports to well-known interfaces (Avalon-MM / Avalon-ST / clock / conduit) See mnl_avalon_spec.pdf Right-click on the interface and select ex "new Avalon Streaming Source" if need such an interface. Re-use this interface for the remaining source signals. Note that the "clk" and "reset_n" both must use the same clock interface. This way we indicate that they are related.

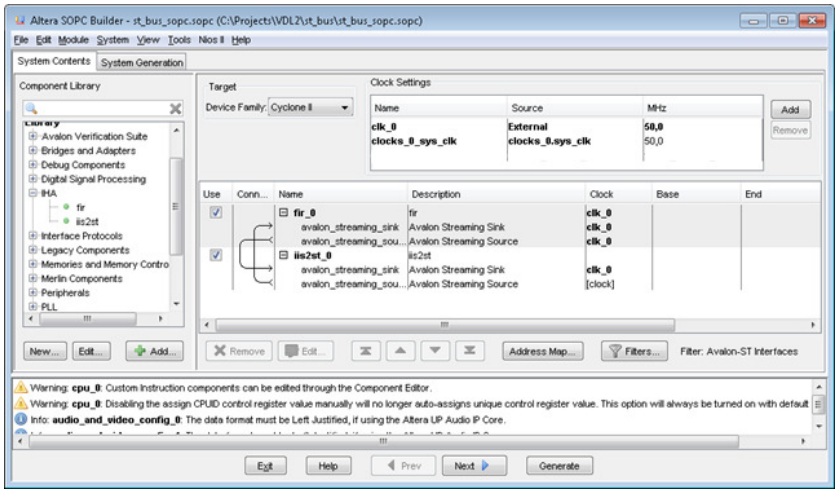


C) Going to the "Interfaces" page, you should start out by pressing "Remove Interfaces with no Signals" if it is not faded out. The streaming busses will have to have a clock signal associated. Select the clock signal. A reset signal may not be required. You also have to specify the number of bits per symbol. Qsys expects only one symbol per beat, so you'll have to specify the number of bits you expect to transfer in parallel. Not the waveform at the bottom, this should reflect what you want.



D) In the next page you may specify author, group and a lot more. Adding a group, say "ASE" will put your custom component in an ASE folder in the component library. Press Finish

E) You are now able to add your custom component to your project. You can right-click and filter the interfaces shown in the SOC overview. The new component will have source and sink busses that you can connect to other ST-bus components (with similar formatting) or use adapters from the component library adapt the ST-bus format


Altera SOPC Builder - st_bus_sopc.sopc (C:\Projects\VDL2\st_bus\st_bus_sopc.sopc)
File Edit Module System View Tools Nios II Help
System Contents System Generation
Component Library
Target
Device Family: Cyclone II
Clock Settings
Name Source MHz
clk_0 External 50,0
clocks_0_sys_clk clocks_0.sys_clk 50,0
Add
Remove
Use Conn... Name Description Clock Base End
fir_0 fir clk_0
avalon_streaming_sink Avalon Streaming Sink clk_0
avalon_streaming_sou... Avalon Streaming Source clk_0
iis2st_0 iis2st
avalon_streaming_sink Avalon Streaming Sink clk_0
avalon_streaming_sou... Avalon Streaming Source [clock]
Avalon Verification Suite
Bridges and Adapters
Debug Components
Digital Signal Processing
IHA
fir
iis2st
Interface Protocols
Legacy Components
Memories and Memory Contro
Merlin Components
Peripherals
PLL
New... Edit... Add...
Remove Edit... Address Map... Filters... Filter: Avalon-ST Interfaces
Warning: cpu_0: Custom Instruction components can be edited through the Component Editor.
Warning: cpu_0: Disabling the assign CPUID control register value manually will no longer auto-assigns unique control register value. This option will always be turned on with default
Info: audio_and_video_config_0: The data format must be Left Justified, if using the Altera UP Audio IP Core.
Exit Help Prev Next Generate