TUTORIAL: QUARTUS FIR COMPILER

Goal

Create a basic FIR filter using the Quartus II MegaWizard FIR II Compiler. The filter has the following properties:

- Low-pass filter with cut-off at pi/4
- Signed 24-bit in-/outputs
- Output is the 24 MSb
- Interface is Avalon ST (8-bit symbols, 24-bits/cycle, no back pressure)

Prerequisites

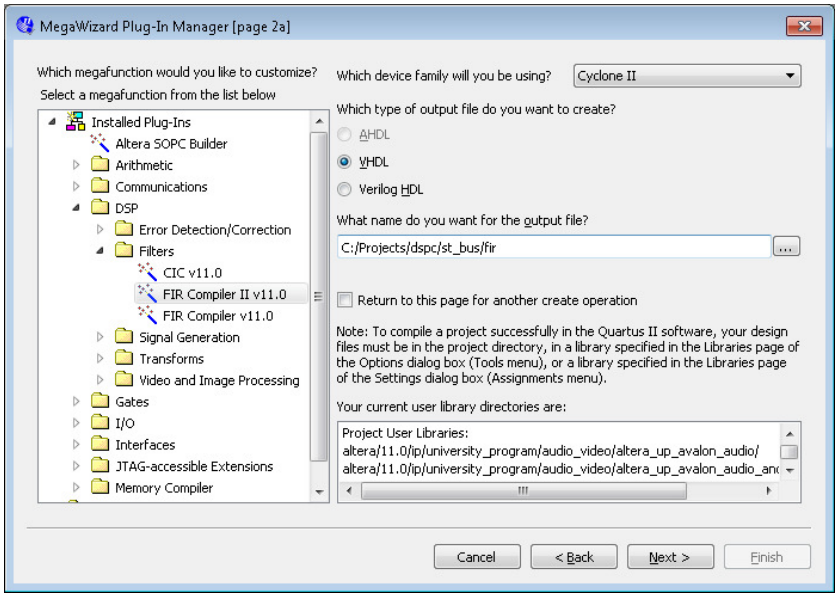
- Quartus with appropriate licenses for the FIR Compiler II

Use the FIR Compiler II MegaCore Function User Guide as reference for this guide

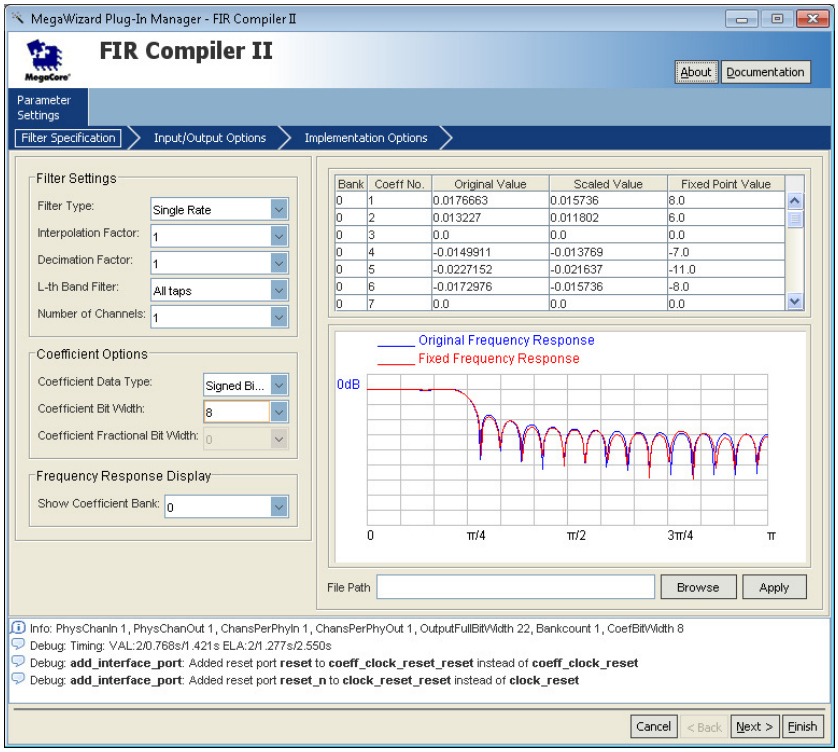
How To Do It

A) In Quartus II, open the project in which you want to use the filter. When opened, select the Altera Megawizard from the tools menu.

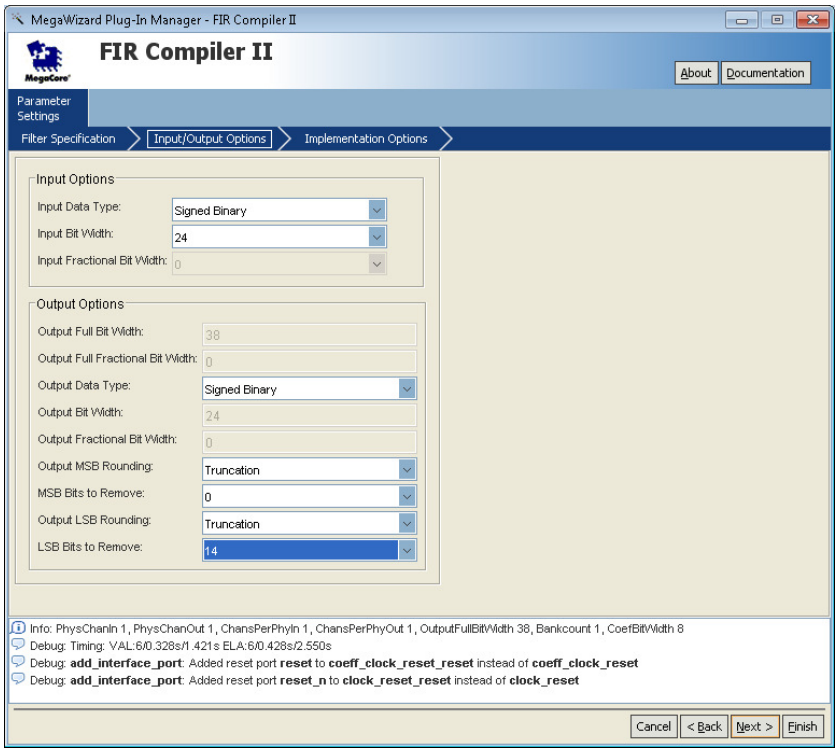
B) Select the "FIR Compiler II" from the DSP subsection. Name your function "fir_filter".



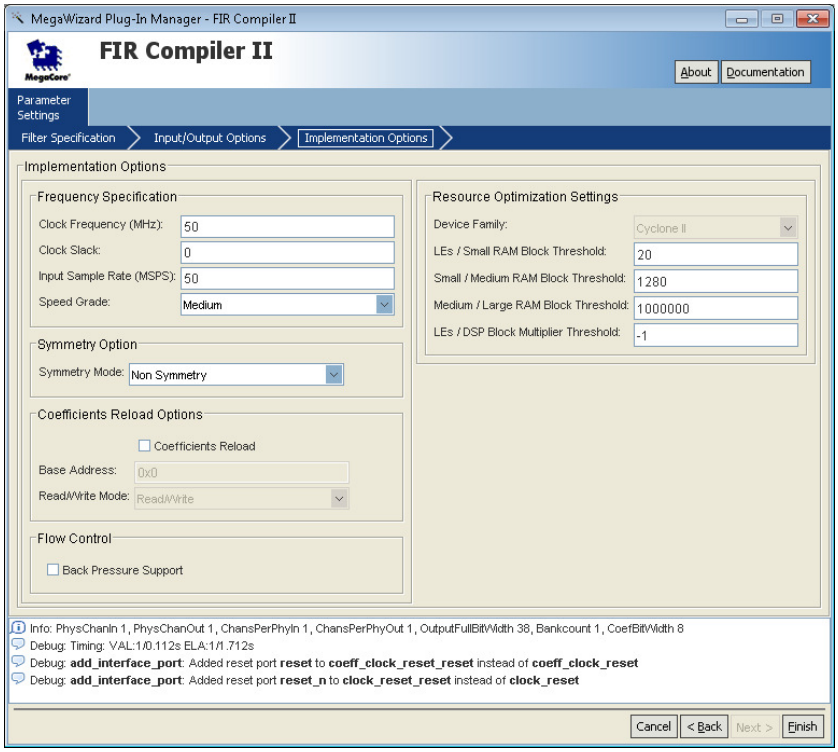
C) Use the default settings on the first page, note the frequency response, a low-pass function that cuts-off around pi/4



D) On the next page you have to select the in-/output data widths. Enter a signed 24-bit input data width. For the output, select to remove 14-bits, to get a 24-bit output. The multiplication with the 8-bit coefficients the summation of the many taps is the reason for this. Removing only LSBs ensures that no overflow will occur, but it also removes resolution. This will be significant with low-level input signals.



E) Set the clock frequency to 50 MHz and the sampling frequency likewise. Note that the filters frequency response scales with the sampling frequency (=pi/2). If the clock frequency is higher then the sampling frequency, the FIR compiler may re-use multipliers and adders when building the filter hardware.



F) Press finish and you are done.

Note that you can run the filter with a 48 KHz clock if you want, you will not be using the resources in an optimal fashion, but it will work. Keeping the clock and sampling frequency the same, pi/2 will now be the 48 KHz instead.