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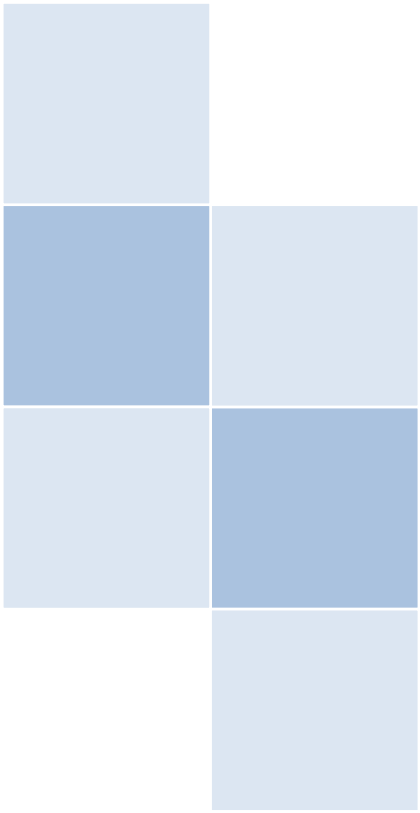
EC/LD LAB MANUAL



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Clipper And Clamper

Theory:

Diodes can be used as switches depending on the biasing type, reverse of forward. The clipping circuit, also referred to as clipper, clips off some of the portions of the input signal and uses the clipped signal as the output signal. The clamping circuit or clamper keeps the amplitude of the output signal same as that of the input signal except that the D.C. level (offset) has been changed. The clamper through which the input waveform shifts to positive direction is called positive clamper, otherwise, is called negative clamper.

Clipper Circuits

There are two types of clipper circuits, the series and parallel diode clipping circuits.

Series Diode Clipping Circuit

In these type of circuits, the diode is connected between the input and output voltage terminals. the negative cycle of the input voltage can be clipped of by this type of series clippers. Reverse of the diode pins yields to a positive cycle clipping circuit. Circuits clip the values larger or smaller than zero voltage. This voltage, technically called “threshold voltage” and can be changed to a desired value by inserting a D.C. voltage source. This is achieved in two different ways. In the first type, the voltage source of Vm (positive or negative) is connected through output terminals. Depending on the diode connection (normal or reverse), the values smaller or greater than Vm is clipped and assigned as Vm. In the second type of thresholded series clipping, the voltage source is applied between the input and output terminals, series with the diode. This time, the clipped values are assigned to zero and the net output voltage equals to the difference between the input and threshold values.

Parallel Diode Clipping Circuit

In this type of clippers, the diode is connected between output terminals. The on/off state of diode directly affects the output voltage. These type of clippers may also have a non-zero threshold voltage by addition of a voltage series with diode.

Clamper Circuits

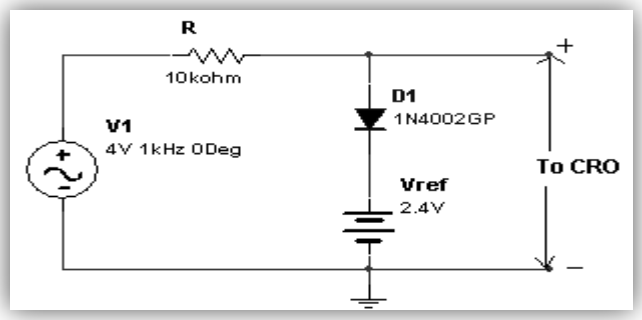
Clamper Circuits, or briefly clampers are used to change the D.C. level of a signal to a desired value. Being different from clippers, clamping circuits uses a capacitor and a diode connection. When diode is in its on state, the output voltage equals to diode drop voltage (ideally zero) plus the voltage source, if any. As you know, this circuit, in fact, is a series R-C circuit. The resistance of diode and the small capacitance yield to a small time-constant for this circuit. This means that the capacitor will rapidly be charged if any input voltage, that is enough to switch on the diode, is applied. The diode will conduct during the positive cycle of the input signal and output voltage will be ideally zero (in practice this voltage equals ~0.6 V). Note that during positive cycle the capacitor is rapidly charged in inverse polarity with the input voltage. After transition to negative cycle, the diode becomes to its off state. In this case, the output voltage equals to the sum of the input voltage and the voltage across the terminals of the capacitor which have the same polarity with each other. The resulting signal after a complete cycle.

Aim **:** Testing of Positive Diode Clipping Circuit.

Components:

Sl.No.	ITEMS	QUANTITY
1	**Signal Generator**	**1**
2	**CRO**	**1**
3	**VRPS**	**1**
4	**Probes**	**3**
5	**Patch cords**	

Circuit Diagram :



Design :

Assume,

Vo = 3V

WKT,

Vo = Vd + Vref

Where, Vd = cut in voltage of diode = 0.6V (Si diode)

3 = 0.6 + Vref

Vref = 2.4V

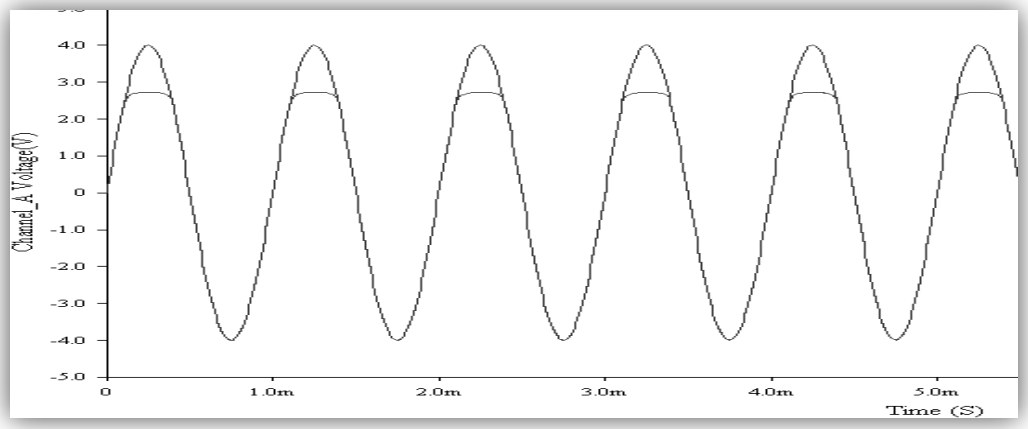
WKT, $R = (Rf + Rr)^{1/2}$

Where, Rf = Forward resistance of diode when diode is forward biased = 10Ω

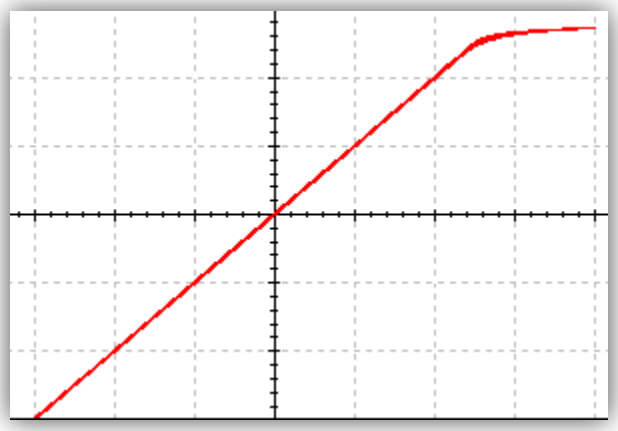
Rr = reverse resistance of diode when diode is reverse biased = 10MΩ.

Therefore, **R =10KΩ**

Input Output Waveform :



Transfer Characteristics :



Procedure :

1. Before making the connections check all components using multimeter.
2. Make the connections as shown in circuit diagram.
3. Using a signal generator (Vi) apply a sine wave of 1KHz frequency and a peak-to-peak amplitude of 4V to the circuit. (Sine wave)
4. Keep the CRO in dual mode, connect the input (Vi) signal to channel 1 and output waveform (Vo) to channel 2.
5. Observe the clipped output waveform which is as shown in waveforms. Also record the amplitude and time data from the waveforms.
6. Now keep the CRO in X-Y mode and observe the transfer characteristic waveform.
7. Adjust the ground level of the CRO on both channels properly and view the output in DC mode (not in AC mode)

Result :

The positive clipper circuit is verified.

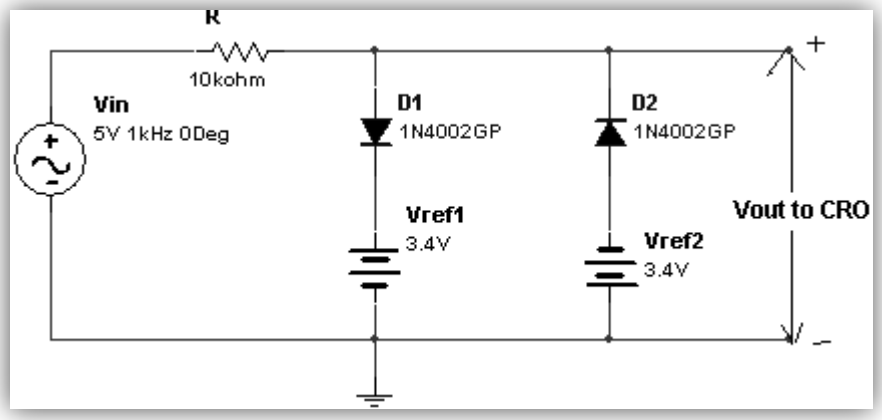
Observation:

Aim **:** Testing of Positive Diode Double ended Clipping Circuit.

Components:

Sl.No.	ITEMS	QUANTITY
1	Signal Generator	1
2	CRO	1
3	VRPS	2
4	Probes	3
5	Patch cords	

Circuit Diagram :



Design :

Assume,

Vo = 4V

WKT,

Vo(max) = Vd1 + Vref1

Where, Vd = cut in voltage of diode = 0.6V (Si diode)

4 = 0.6 + Vref1

Vref1 = 3.4V

Vo(min) = Vd2 + Vref2

-4 = -0.6 + (-Vref2)

Vref2 = -3.4V

WKT,

$R = (Rf + Rr)^{1/2}$

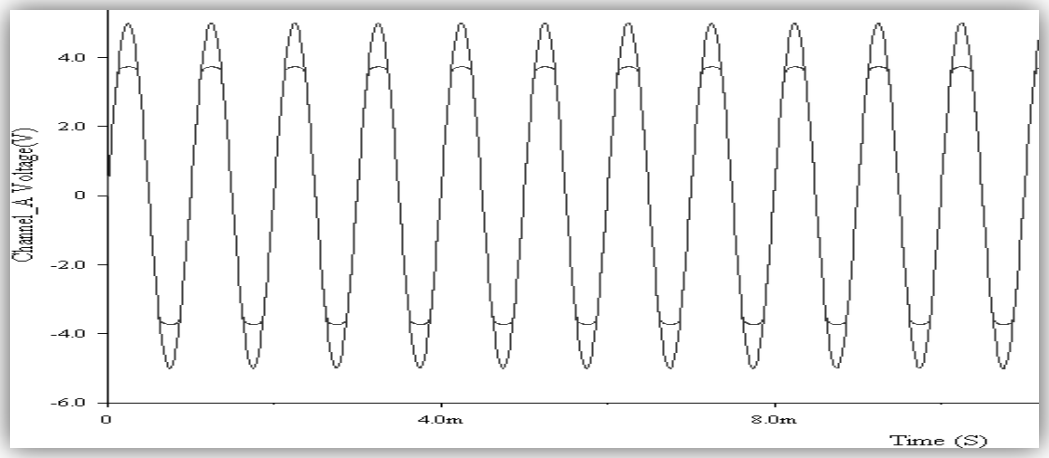
Where, Rf = Forward resistance of diode when diode is forward biased = 10Ω

Rr = reverse resistance of diode when diode is reverse biased = 10MΩ

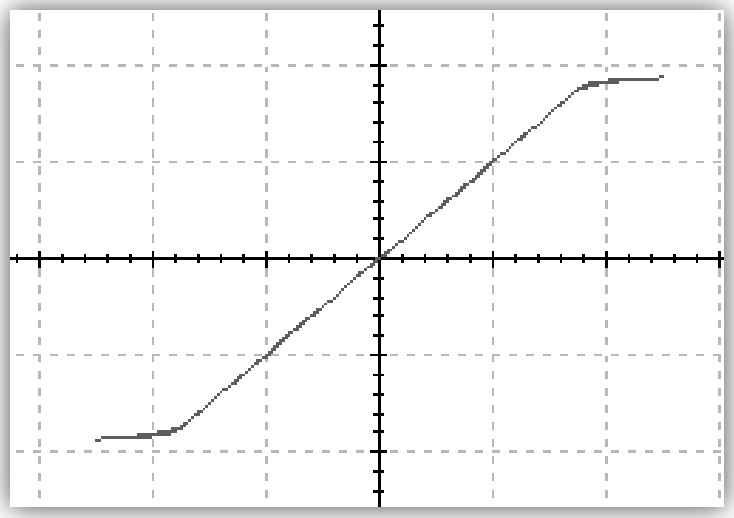
Therefore,

R =10KΩ

Input Output Waveform :



Transfer Characteristics :



Procedure :

1. Before making the connections check all components using multimeter.
2. Make the connections as shown in circuit diagram.
3. Using a signal generator (Vi) apply a sine wave of 1KHz frequency and a peak-to-peak amplitude of 5V to the circuit. (Sine wave)
4. Keep the CRO in dual mode, connect the input (Vi) signal to channel 1 and output waveform (Vo) to channel 2.
5. Observe the clipped output waveform which is as shown in waveforms. Also record the amplitude and time data from the waveforms.
6. Now keep the CRO in X-Y mode and observe the transfer characteristic waveform.
7. Adjust the ground level of the CRO on both channels properly and view the output in DC mode (not in AC mode)

Result :

The double ended clipper circuit is verified.

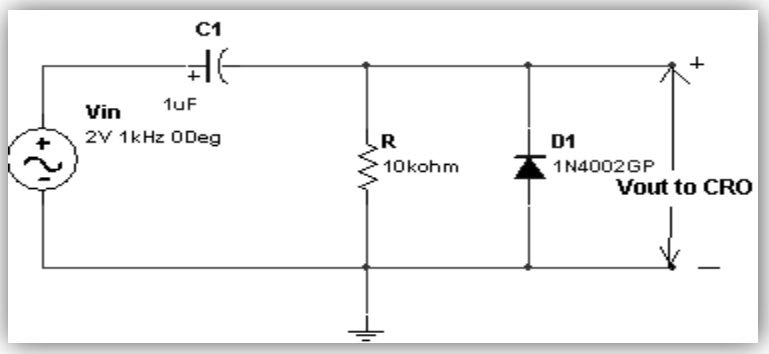
Observation:

Aim **:** Testing of Positive Diode Clamping Circuit.

Components :

Sl.No.	ITEMS	QUANTITY
1	**Signal Generator**	**1**
2.	**Capacitor : 1µF**	**1**
3	**CRO**	**1**
4	**VRPS**	**2**
5	**Probes**	**3**
6	**Patch cords**	

Circuit Diagram :



Design :

Assume, Input frequency, f =1KHz,

Therefore, T =1ms

Discharging time RC > T, RC = 10T

WKT, $R = (Rf + Rr)^{1/2}$

Where, Rf = Forward resistance of diode when diode is forward biased = 10Ω

Rr = reverse resistance of diode when diode is reverse biased = 10MΩ

R= 10 KΩ

Therefore, **C = 1 µF**

Analysis:

WKT, Vout = Vac + Vdc, ----(1)

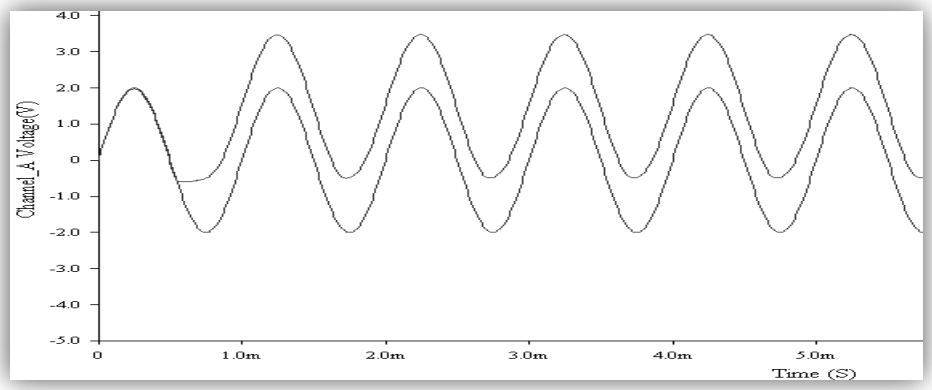
where Vac = Vin, and Vdc = Vc = Vm – Vd = 2 – 0.6 = 1.4V

Where Vd = 0.6V

To find Vout:

When Vin = 0V	When Vin = +Vin = Vm	When Vin = -Vin = -Vm
From Eq(1)	From Eq(1)	From Eq(1)
Vout = 0 +1.4 =1.4V	Vout = 2 +1.4 = 3.4V	Vout = -2 + 1.4 = -0.6V

Input Output Waveform :



Procedure:

1. Before making the connections check all components using multimeter.
2. Make the connections as shown in circuit diagram.
3. Using a signal generator (Vi) apply a sine wave of 1KHz frequency and a peak-to-peak amplitude of 2V to the circuit. (Sine wave)
4. Keep the CRO in dual mode, connect the input (Vi) signal to channel 1 and output waveform (Vo) to channel 2.
5. Observe the clipped output waveform which is as shown in waveforms. Also record the amplitude and time data from the waveforms.
6. Now keep the CRO in X-Y mode and observe the transfer characteristic waveform.
7. Adjust the ground level of the CRO on both channels properly and view the output in DC mode (not in AC mode)

Result :

Positive clamping circuit is tested.

Observation:

CE Amplifier

Theory :

In the frequency response for an IC coupled amplifier the voltage gain drops off at low and high frequencies, where as it is uniform over the mid frequency range of 50 Hz to 20 KHz.

At low frequency the reactance of the coupling capacitor is fairly high and also a very small portion of the small signal will pass from one stage to the next. The shunt capacitor cannot shunt the emitter resistance effectively because of it's large reactance at low frequencies. Due to these two reasons, there is a fall of voltage gain at low frequencies.

At high frequency the reactance of the coupling capacitor is very small and it acts as a short circuit. This results in an increase of loading of the next stage and a reduction in the voltage gain. At high frequency the reactance of base-emitter junction is low, which increases the base current. Consequently the amplification factor β is reduced. These two factors will cause the voltage gain to drop off at high frequency.

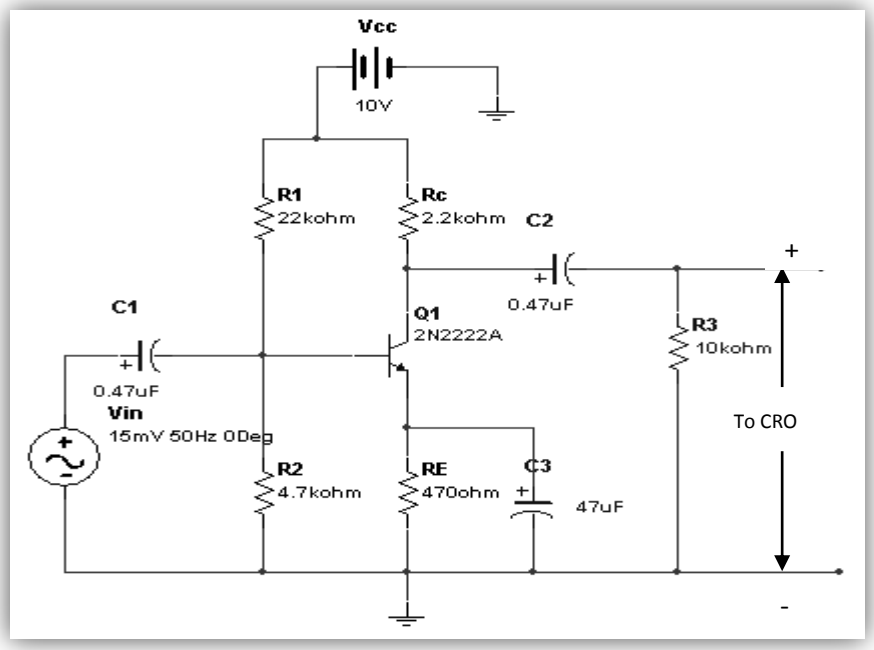
At mid frequency the voltage gain of the amplifier is constant. The effect of coupling capacitor is to maintain a uniform voltage gain. Thus with the increasing frequency in this range, the reactance of coupling capacitor decreases which tends to increase the gain. On the other hand lower reactance means higher loading of the first stage and hence lower gain. These two phenomenon practically cancel each other, resulting in a uniform gain in the mid frequency.

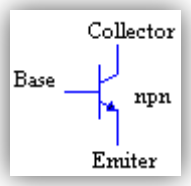
Aim: Wiring of RC coupled single stage BJT amplifier and determination of the gain, frequency response, input and output impedances.

Components:

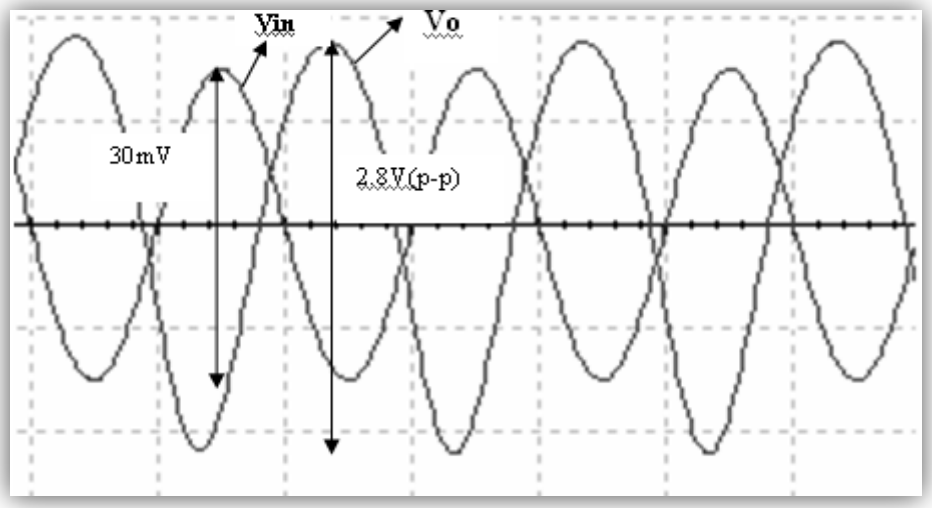
Sl.No.	ITEMS	QUANTITY
1	Transistor (npn – SL100)	1
2	Resistors: 2.2KΩ 4.7KΩ 10KΩ 22KΩ 470Ω	 1 1 1 1 1
3	Capacitors: 0.47µF 47 µF	 2 1
4 5 6 7 8 9	Decade Resistance Box (DRB) Signal Generator CRO VRPS Probes Patch cords	1 1 1 1 3

Circuit Diagram:

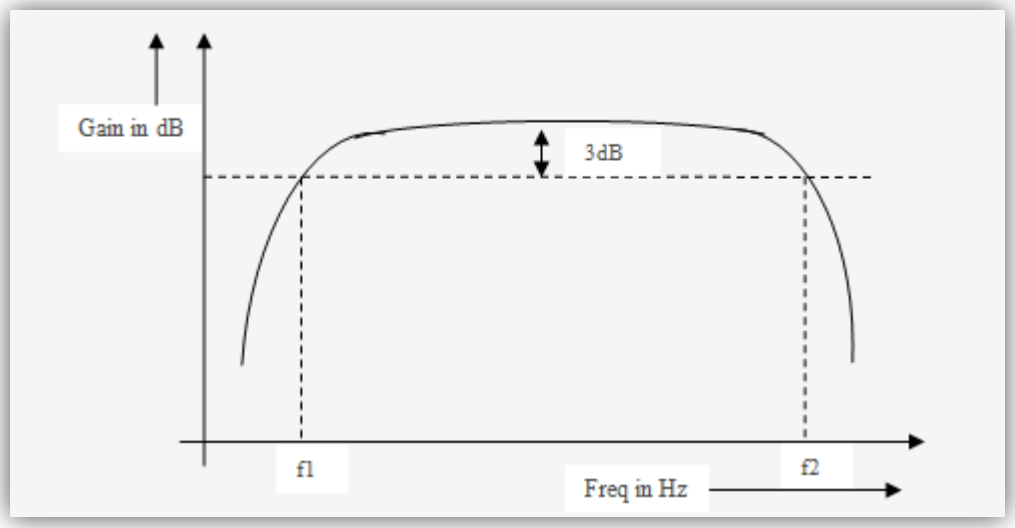




Input / Output Waveforms :



Model Graph:



Design :

Consider,

V_{CC} = 10V, I_C = 2mA.

Therefore,

$V_{CE} = V_{CC} / 2$

V_{CE} = 5V

$V_{RE} = (1/10)*V_{CC} = (1/10)*10$

V_{RE} = 1V

$R_E = V_{RE} / I_c = 1V / 2mA$

$R_E = 470\Omega$

$R_c = V_{cc} – V_{CE} – (V_{BE} / I_c) = 10 – 5 – (1V / 2MA)$

$R_c = 2.2K\Omega$

Assume,

$H_{FE} = 50$

$I_B = I_c / H_{FE} = 20mA / 50 = 0.04mA$

$V_B = V_{BE} + V_{RE} = 1V + 0.7V = 1.7V$

Assume 10 I_B flows through R1. So,

$R1 = (V_{cc} – V_B) / 10\ I_B = (10 – 1.7) / 10^* 0.04mA$

$R1 = 21K\Omega \approx 22K\Omega$

Assume 9 I_B flows through R2. So,

$R2 = V_B / 9\ I_B = 1.7 / (9 * 0.04m)$

$R2 = 4.7K\Omega$

Bypass capacitor C_E

$X_{CE} = R_E / 10$ at f_L =100Hz and $X_{CE} = 1 / (2\pi f_L C_E)$

$C_E = 10 / (2\pi * 100 * 470)$

$C_E = 33.8\mu F \approx 47\mu F$

Choose,

$C1 = C2 = 0.47\ \mu F$ and $R_L = 10K\Omega$

Tabular Column :

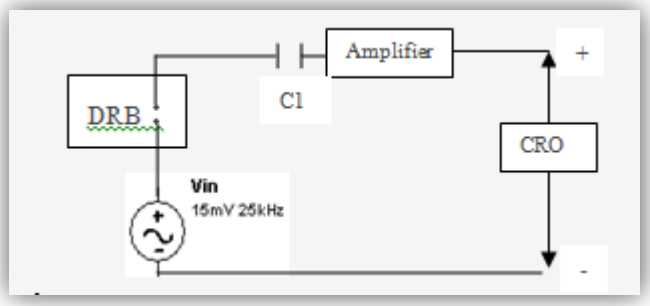
Freq 'f' in Hz	O/p Voltage 'Vo' in V	Gain A = Vo / Vin	Gain in dB A = 20log(Vo / Vin)
100			
200			
.			
.			
900			
1K			
2K			
.			
.			
9K			
10K			
20K			
.			
.			
90K			
100K			
200K			
.			
.			
900K			
1M			

Procedure :

1. Make circuit connections as shown in circuit diagram.
2. Give Vin = 30mV(p-p) from signal generator and supply voltage of 10V from power supply.
3. Frequency is varied from 100Hz to 1MHz with suitable steps by maintaining Vin = 30mV(p-p) constant and corresponding output is measured.
4. Graph is plotted in semi log graph sheet with frequency along x – axis (log scale) and gain in db along y – axis (linear scale)
5. From the maximum frequency response gain, draw a line 3db down. It cuts the frequency response at f1(lower cutoff frequency) and at f2 (higher cutoff frequency). The difference between f1 and f2 is called gain bandwidth, is measured.
6. The gain bandwidth product or figure of merit which is product of gain (factor) and bandwidth is determined.

To Measure Input Impedance:

Circuit Diagram:

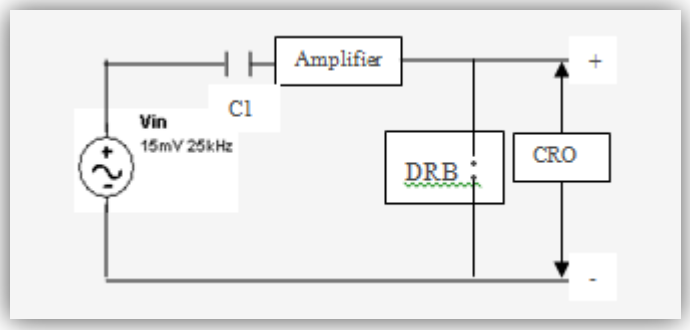


- Connect DRB in series with the input and keep the DRB in minimum value.
- Choose input frequency (25 to 30KHz), at which Vout is maximum, say Vout = Vout(max)
- Now increase DRB value so that Vout = Vout(max) / 2.
- Read the DRB Resistance value. This value is the required input impedance.

Input impedance = _____Ω

To Measure Output Impedance:

Circuit Diagram:



- Connect DRB in parallel with the output and keep the DRB in maximum value.
- Choose input frequency (25 to 30KHz), at which Vout is maximum, say Vout = Vout(max)
- Now decrease DRB value so that Vout = Vout(max) / 2.
- Read the DRB Resistance value. This value is the required output impedance.

Output impedance = _____ Ω.

Bandwidth = f2 – f1 = _____KHz

Result:

Thus the RC coupled Single Stage BJT amplifiers were wired and the gain frequency response, input and output impedances were determined.

Bandwidth = _____KHz

Input impedance = _____Ω

Output impedance = _____ Ω.

Observation:

Characteristics Of MOSFET

Theory:

The two types of MOSFETs are the depletion type and the enhancement type, and each has a n / p – channel type. The depletion type is normally on, and operates as a JFET, enhancement type is normally off, which means that the drain to source current increases as the voltage at the gate increases. No current flows when no voltage is supplied at the gate.

The Characteristics of a MOSFET:

1. High input impedance - voltage controlled device - easy to drive.
2. Unipolar device - majority carrier device - fast switching speed.
3. Wide SOA (safe operating area).
4. Forward voltage drop with positive temperature coefficient - easy to use in parallel.
5. In high breakdown voltage devices over 200V, the conduction loss of a MOSFET is larger than that of a BJT, which has the same voltage and current rating due to the on-state voltage drop.
6. Vertically oriented four-layer structure (n+ p n– n+)
7. Parasitic BJT exists between the source and the drain.
8. The p-type body region becomes base, the n+ source region becomes an emitter, and the n-type drain region becomes the collector.
9. The breakdown voltage decreases from BVCBO to BVCEO, which is 50 ~ 60 [%] of BVCBO when the parasitic BJT is turned on. At this state, if a drain voltage higher than BVCEO is supplied, the device falls into an avalanche breakdown state. If the drain current is not limited externally, it will be destroyed by the second breakdown. So the n+ source region and the p-type body region must be shorted by metallization in order to prevent the parasitic BJT from turning on. But if the VDS rate of increase is large in the high speed turn–off state, there is a voltage drop between the base and the emitter, which causes the BJT to turn–on. This is prevented by increasing the doping density of the p - body region, which is at the bottom of the n+ source region, and by lowering the MOSFETs switching speed by designing the circuit so that the gate resistance is large. Due to the source region being short, another parasitic component, the diode is formed. This is used in half-bridge and full-bridge converters.
10. **Output characteristics**

    i_D characteristics due to VDS in many VGS conditions.

    It is divided into the ohmic region, the saturation (=active) region, and the cut-off region.

Ohmic region: A constant resistance region. If the drain-to-source voltage is zero, the drain current also becomes zero regardless of gate–to-source voltage. This region is at the left side of

the VGS – VGS(th) = VDS boundary line (VGS – VGS(th) > VDS > 0). Even if the drain current is very large, in this region the power dissipation is maintained by minimizing VDS(on).

Saturation region: A constant current region. It is at the right side of the VGS – VGS(th) = VDS boundary line. Here, the drain current differs by the gate–to source voltage, and not by the drain-to-source voltage. Hence, the drain current is called saturated.

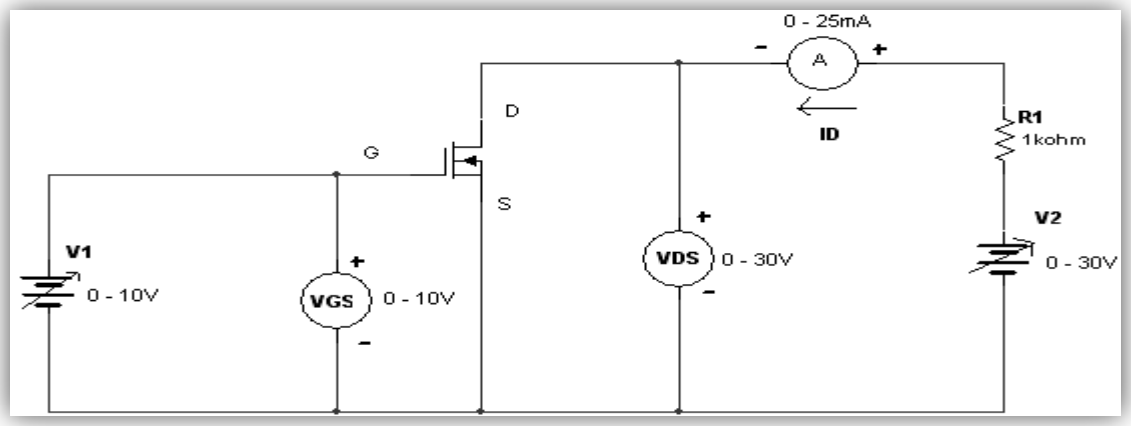
Cut-off region: It is called the cut-off region, because the gate-to-source voltage is lower than the VGS(th) (threshold voltage).

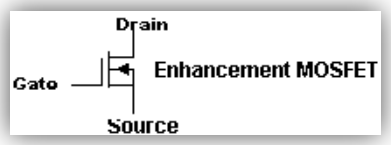
Aim: To determine the drain and transcodnductance characteristics of an enhancement mode MOSFET.

Components:

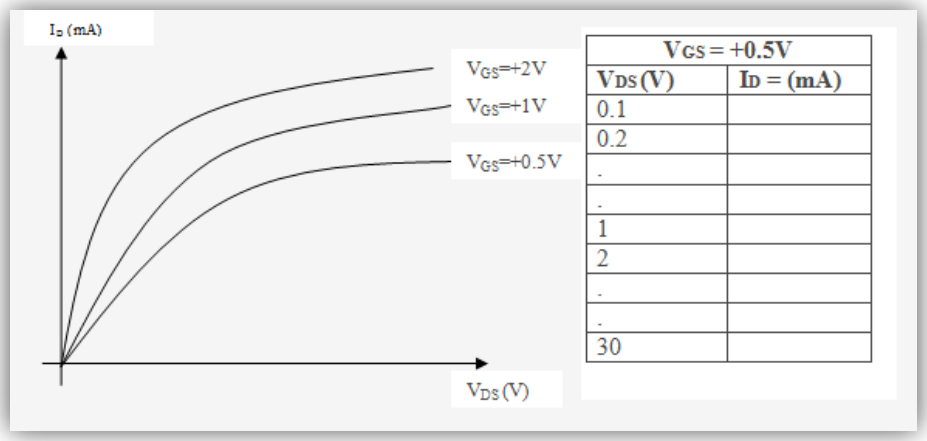
Sl.No.	ITEMS	QUANTITY
1	MOSFET(3N187)	1
	Resistors:	
2	22KΩ	1
3	1.8KΩ	1
4	100KΩ	1
5	VRPS	2
6	Ammeter	1
7	Patch cords	

Circuit Diagram:



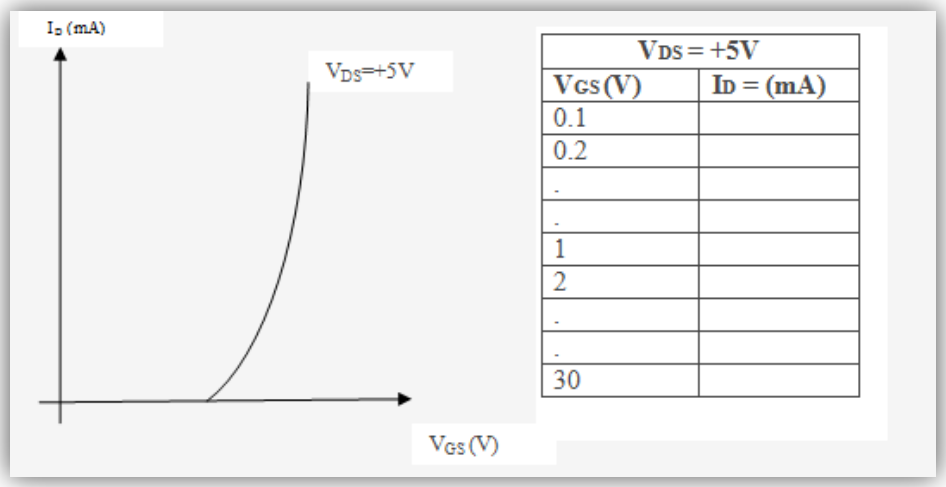


Drain Characteristics:



VGS = +0.5V	
VDS (V)	ID = (mA)
0.1	
0.2	
.	
.	
1	
2	
.	
.	
30	

Transconductance Characteristics:



$V_{DS} = +5V$	
V_{GS} (V)	I_D = (mA)
0.1	
0.2	
.	
.	
1	
2	
.	
.	
30	

Procedure:

1. Make the connections as shown in the corresponding circuit diagram. Special care to be taken in connecting the voltmeters and ammeters according to the polarity shown in circuit diagram.
2. Repeat the procedure for finding drain and Transconductance characteristics of Enhancement MOSFET.
3. Tabulate the readings in separate tabular columns as shown below.
4. Plot the drain characteristics (ID versus VDS for different values of gate voltages VGS). Take ID along the Y-axis and VDS along the X-axis in the plot.
5. From this plot of drain characteristics find the drain resistance,

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}$$

6. Similarly plot the Tranconductance characteristics with ID along the Y-axis and VGS along the X-axis in the graph for one value of VDS, say VDS = 5V.
7. From this plot find the mutual conductance or transconductance,

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

8. Lastly find the amplification factor,

$$\mu = r_d \bullet g_m$$

Procedure for finding the Tran conductance Characteristics:

1. Switch on the power supplies, with both V2 and V1 at zero voltage.
2. Initially set V1 =VGS = 0V. Now set V2 = VDS = 5V (constant).
3. Vary the power supply V1 i.e., VGS and note down the corresponding current ID (in mA) (Simultaneously note down the VGS value from the voltmeter connected at the gate terminal).
4. Repeat the above procedure for a different value of VDS, say 10V.

Note: In the above procedure VDS (i.e., the power supply V2) is kept constant and the power supply V1 (=VGS) is varied.

Drain Characteristics:

1. Initially set V1 = VGS =4V (constant), slowly vary V2 and note down the corresponding current ID. Simultaneously note down in the tabular column the voltmeter reading VGS.
2. Repeat the above procedure for different values of VGS and note down the current ID for corresponding V1 = VDS.
3. Plot the graph of ID versus VDS for different values of gate voltages.

Note: In the above procedure VDS (i.e., the power supply V2) is varied and the power supply V1 (=VGS) is kept constant.

Result:

Drain Resistance r_d **= _____**

Transconductance g_m **= _____**

Amplification factor μ **= _____**

Observation:

Schmitt Trigger Using Op-Amp

Theory:

Schmitt trigger is a comparator circuit that incorporates positive feedback.

When the input is higher than a certain chosen threshold, the output is high; when the input is below another (lower) chosen threshold, the output is low; when the input is between the two, the output retains its value. The trigger is so named because the output retains its value until the input changes sufficiently to trigger a change. This dual threshold action is called hysteresis, and implies that the Schmitt trigger has some memory. In fact, the Schmitt trigger is a bistable multivibrator.

Schmitt trigger devices are typically used in open loop configurations for noise immunity and closed loop positive feedback configurations to implement multivibrators.

Schmitt triggers are commonly implemented using a comparator connected to have positive feedback (i.e., instead of the usual negative feedback used in operational amplifier circuits). For this circuit, the switching occurs near ground, with the amount of hysteresis controlled by the resistances of R_1 and R_2:

The comparator extracts the sign of the difference between its two inputs. When the non-inverting (+) input is at a higher voltage than the inverting (-) input, the comparator output switches to $+V_S$, which is its high supply voltage. When the non-inverting (+) input is at a lower voltage than the inverting (-) input, the comparator output switches to $-V_S$, which is its low supply voltage. In this case, the inverting (-) input is grounded, and so the comparator implements the sign function – its 2-state output (i.e., either high or low) always has the same sign as the continuous input at its non-inverting (+) terminal.

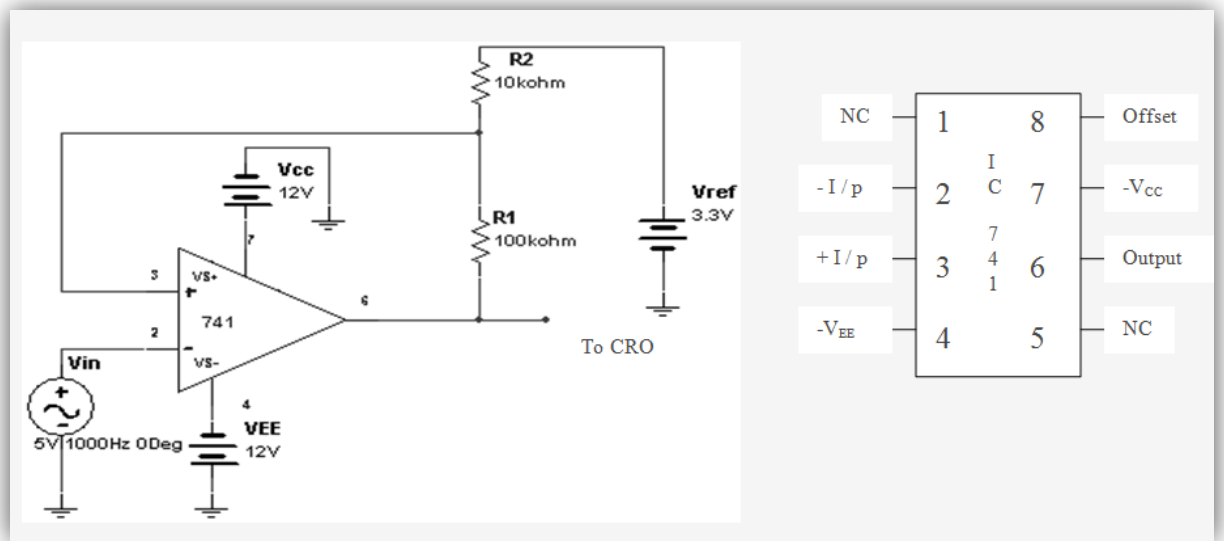
Because of the resistor network connecting the Schmitt trigger input, the non-inverting (+) terminal of the comparator, and the comparator output, the Schmitt trigger acts like a comparator that switches at a different point depending on whether the output of the comparator is high or low. For very negative inputs, the output will be low, and for very positive inputs, the output will be high, and so this is an implementation of a "non-inverting" Schmitt trigger. However, for intermediate inputs, the state of the output depends on both the input and the output. For instance, if the Schmitt trigger is currently in the high state, the output will be at the positive power supply rail ($+V_S$). V_+ is then a voltage divider between V_{in} and $+V_S$.

Aim: To design and implement a Schmitt trigger using Op-amp for given Upper Threshold Level (UTL) and Lower Threshold Level (LTL) values.

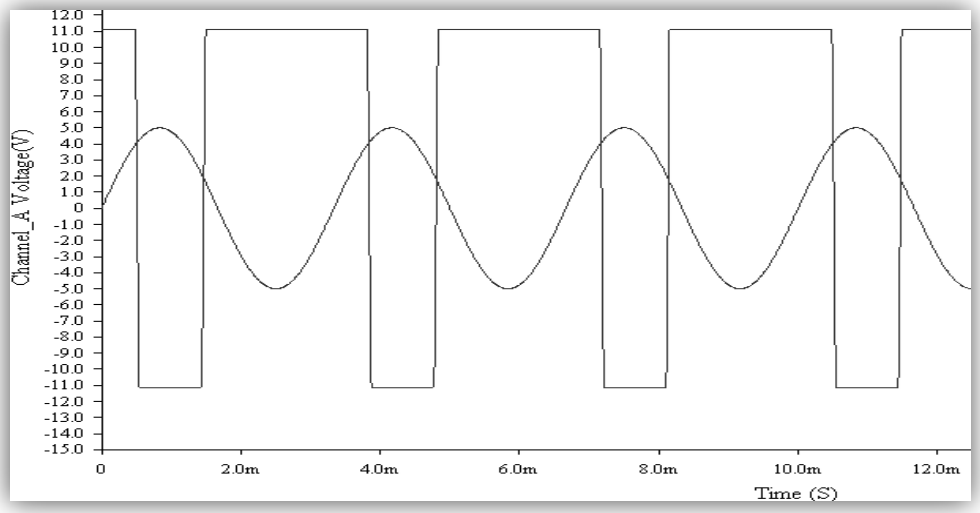
Components:

Sl.No.	ITEMS	QUANTITY
1	**Op-Amp (µA 741)**	**1**
2	**Resistors:**	
3	**10KΩ**	**1**
4	**100KΩ**	**1**
5	**Signal Generator**	**1**
6	**CRO**	**1**
7	**VRPS**	**1**
	Probes	**3**
	Patch cords	

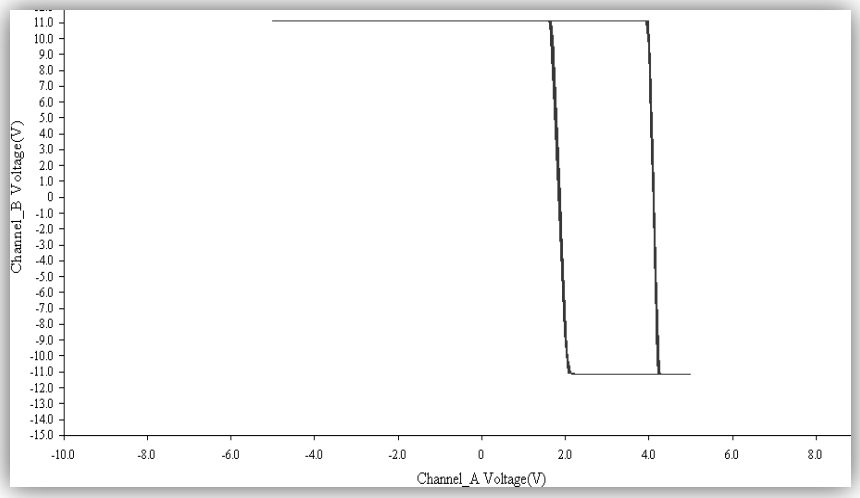
Circuit Diagram:



Input Output Waveform:



Transfer Characteristics:



Design:

Consider,

UTL = 4V, and LTL = 2V

WKT,

UTL = (R1 / (R1 + R2)) * Vref + (R2 / (R1 + R2)) * (+Vsat)

LTL = (R1 / (R1 + R2)) * Vref – (R2 / (R1 + R2)) * (+Vsat)

Where, **±Vsat = ±12V**

UTL + LTL = 2 * (R1 / (R1+ R2)) * Vref

6 = 2 * (R1 / (R1+ R2)) * Vref ----------(1)

UTL – LTL = 2 * (R2 / (R1+ R2)) * (+Vsat)

2 = 2 * (R2 / (R1+ R2)) * (+Vsat) ----------(2)

From (2),

2 /12 = 2 * (R2 / (R1+ R2))

(R2 / (R1+ R2)) = 1/ 12 = 0.083

R1+ R2 = 12 * R2

R1 = 11 R2

From (1),

6 = 2 * (11 R2 / 12 R2) * Vref

Verf = 3.272V ≈ 3.3V

Choose,

R2 = 10KΩ,

Therefore,

R1 = 11 * 10KΩ ≈ 100KΩ

Procedure:

1. Before doing the connections, check all the components using multimeter.
2. Make the connection as shown in circuit diagram.
3. Using a signal generator apply the sinusoidal input waveform of peak-to-peak amplitude of 6-10V, frequency 1 kHz.
4. Keep the CRO in dual mode; apply input (Vin) signal to the channel 1 and observe the output (Vo) on channel 2 which is as shown in the waveform below. Note the amplitude levels from the waveforms.
5. Now keep CRO in X-Y mode and observe the hysteresis curve.

Result:

The output waveforms are studied for Schmitt trigger and the practical values of UTL and LTL are matching with the theoretical value.

UTL = _____V

LTL = _____ V

Observation:

Op-Amp Relaxation Oscillator

Theory:

This circuit is an oscillator that generates a square wave. The op-amp starts with its two inputs in an unknown state; let's say it starts with + slightly higher than –. The op-amp greatly amplifies this difference, bringing its output to the op-amp's positive power supply voltage, its maximum output. The two 10k resistors act as a voltage divider which put the + input at half the output voltage. The – input is at ground, lower than the + input, so the op-amp output stays at Vsat.

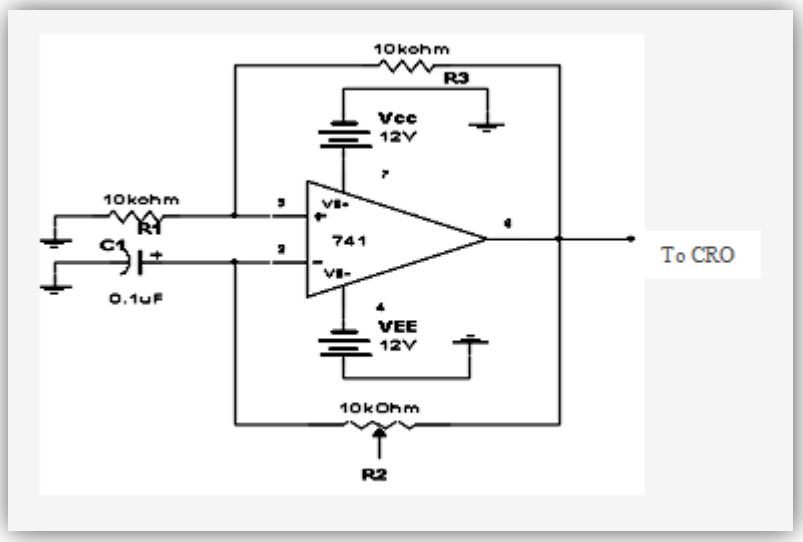
Now current flows in the other direction, discharging the capacitor and reversing its polarity.

Aim: To design and implement a rectangular waveform generator for given frequency.

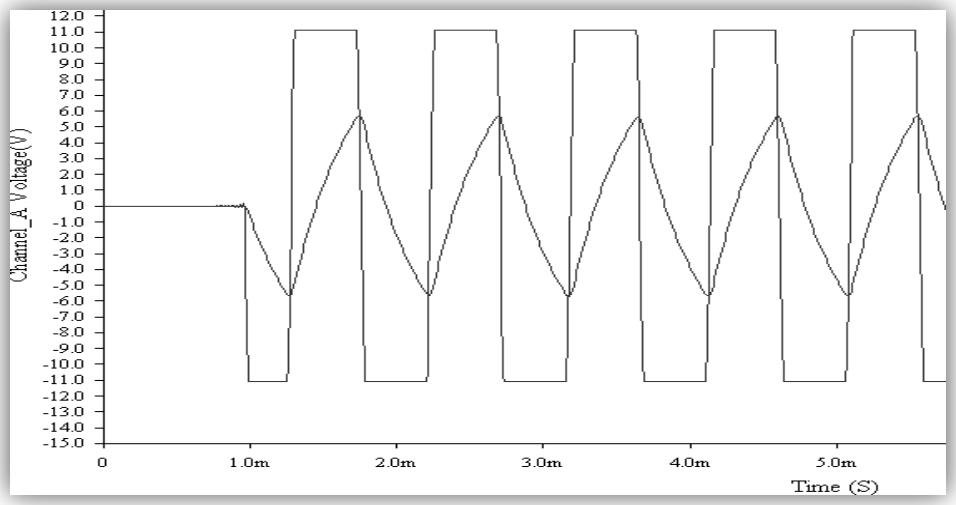
Components:

Sl.No.	ITEMS	QUANTITY
1	**Op-Amp (µA 741)**	**1**
2	**Resistors: 10KΩ**	**2**
3	**Potentiometer :10KΩ**	**1**
4	**Capacitor:0.1 µF**	**1**
5	**CRO**	**1**
6	**VRPS**	**1**
7	**Probes**	**2**
8	**Patch cords**	

Circuit Diagram:



Input Output Waveform:



Design:

Consider,

Frequency **f = 1KHz**

For Relaxation oscillator,

$F = 1/ 2RC$

Assume,

C = 0.1 µF

Therefore,

$R = ½ * 1 * 10^{3} * 0.1 * 10^{-6}$

R = 10KΩ (Range)(Potentiometer)

Procedure:

1. Before making the connections check all the components using multimeter.
2. Make the connections as shown in figure and switch on the power supply.
3. Observe the voltage waveform across the capacitor on CRO.
4. Also observe the output waveform on CRO. Measure its amplitude and frequency.

Result:

Relaxation oscillator using op-amp is designed for given frequency and output waveform is observed (square wave).

Observation:

Astable Multivibrator Using 555 Timer

Theory:

The 555 is also a common CMOS multivibrator used in timing applications.

The astable multivibrator does not require any external trigger to change the state of the output.

An astable multivibrator is a timing circuit whose 'low' and 'high' states are both unstable. As such, the output of an astable multivibrator toggles between 'low' and 'high' continuously, in effect generating a train of pulses. This circuit is therefore also known as a 'pulse generator' circuit.

In this circuit, capacitor C1 charges through R1 and R2, eventually building up enough voltage to trigger an internal comparator to toggle the output flip-flop. Once toggled, the flip-flop discharges C1 through R2 into pin 7, which is the discharge pin. When C1's voltage becomes low enough, another internal comparator is triggered to toggle the output flip-flop. This once again allows C1 to charge up through R1 and R2 and the cycle starts all over again.

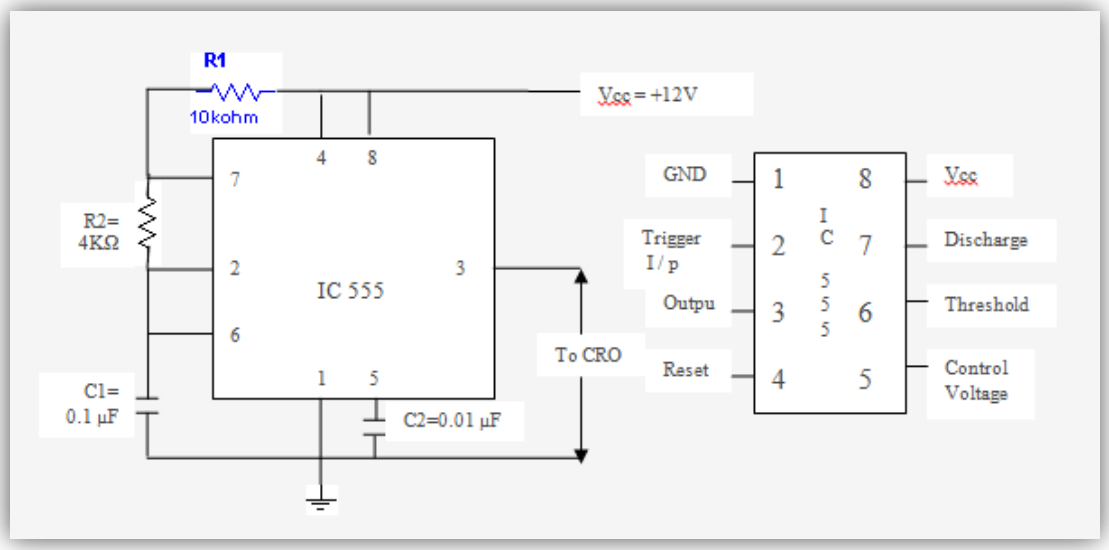
C1's charge-up time t1 is given by: t1 = 0.693(R1+R2)C1. C1's discharge time t2 is given by: t2 = 0.693(R2)C1. Thus, the total period of one cycle is t1+t2 = 0.693 C1(R1+2R2). The frequency f of the output wave is the reciprocal of this period, and is therefore given by: f = 1.44/(C1(R1+2R2)), wherein f is in Hz if R1 and R2 are in megaohms and C1 is in microfarads.

Aim: To design and implement an astable multivibrator circuit using IC 555 timer for a given frequency and duty cycle (frequency 1KHz and 0.75 duty cycle unsymmetrical).

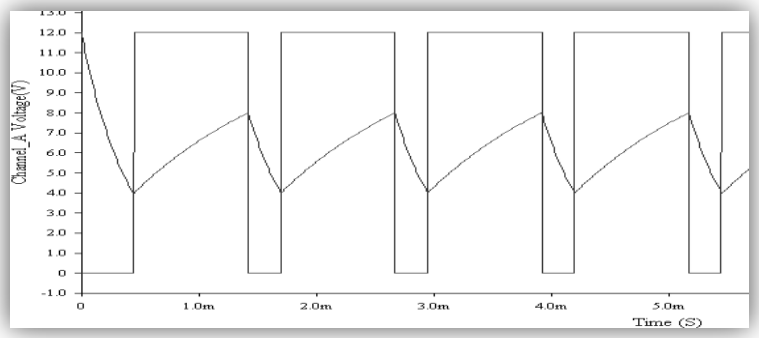
Components:

Sl.No.	ITEMS	QUANTITY
1	IC 555 Timer	1
2	Resistors: 10KΩ 4KΩ	 1 1
3	Capacitor: 0.1 µF 0.01 µF	 1 1
4 5 6 7	CRO VRPS Probes Patch cords	1 1 2

Circuit Diagram:



Input Output Waveform:



Design:

WKT,

Vcc = +12V

V_{UT} = Upper Threshold voltage = 2/3 Vcc

V_{LT} = Lower Threshold voltage = 1/3 Vcc

$T_H = 0.693 (R_1 + R_2) C_2$

$T_L = 0.693 R_2 C$

$T = T_H + T_L = 0.693 (R_1 + 2R_2) C_2$

Output frequency = $f = 1/T = 1 / 0.693 (R_1 + 2R_2) C_2$

$= 1.44 / (R_1 + 2R_2) C_2$

Output duty cycle $d = T_H / T = (R_1 + R_2) / (R_1 + 2R_2)$

Frequency **f = 1KHz,**

d = 0.75,

$T = 1/f = 1 / 1*10^3 = 1ms = T_H + T_L$

Duty cycle, $d = T_H / T$ = % duty cycle / 100

$T_H = 0.75 * T = 0.75ms$

$T_L = T - T_H = 1 – 0.75 = 0.25ms$

$T_L = 0.693 R_2 C$

Choose,

C_2 = 0.1 µF

$R_2 = T_L / 0.693C = 0.25 * 10^{-3} / 0.693 * 0.1 * 10^{-6} = 3.6K\Omega$

$T_H = 0.693 (R_1 + R_2) C_2 = 0.75ms$

$R_1 + R_2 = 0.75 / 0.693 * 0.1 * * 10^{-6} = 10.82 K\Omega$

$R_1 = 10.82 K\Omega - 3.6 K\Omega = 7.2 K\Omega$

Choose, **$R_1 \approx 10 K\Omega$, and $R_2 \approx 4 K\Omega$.**

Procedure:

1. Make circuit connections as shown in circuit diagram.
2. Switch ON the DC power supply Vcc = +12V.
3. Observe the output waveform at pin number 3 using CRO.
4. Measure the output pulse amplitude.
5. Observe the capacitor voltage waveform at pin number 6 and measure the maximum and minimum voltage levels. Verify that V_{UT} = 2/3 Vcc and V_{LT} = 1/3 Vcc.
6. Compare the capacitor voltage Vc with output waveform Vo and note that capacitor charges and Vc raises exponential when output is high. The capacitor C discharges through R_2 and discharges transistors. Vc follows when output is low.
7. Calculate the duty cycle 'd' and output frequency 'f'. Verify the same.
8. Verify whether the theoretical value are matching with the practical values and observe the output.

Result:

The output waveform for astable multivibrator is studied and practical and theoretical values are verified.

T_H = _____ms

T = _____ms

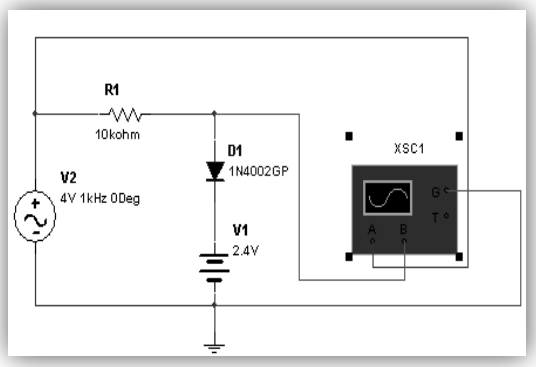
Duty cycle = _____%

Observation:

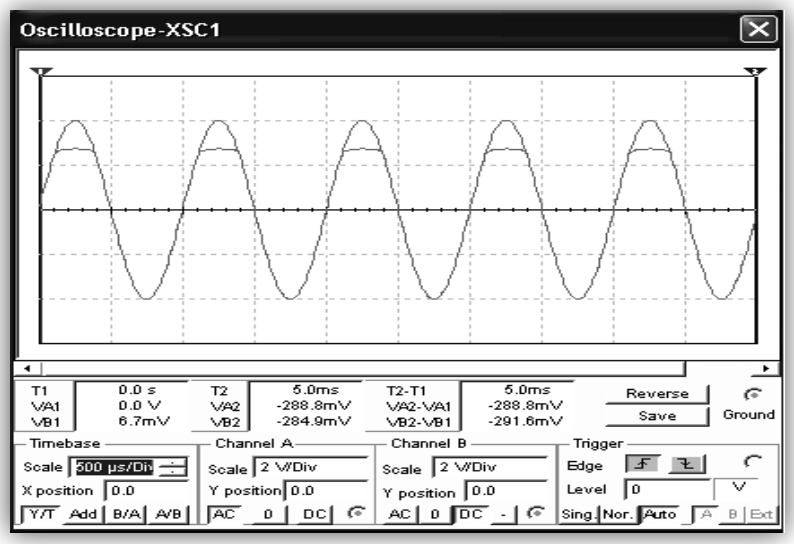
Clipper And Clamper

Aim: Testing of Positive Diode Clipping Circuit.

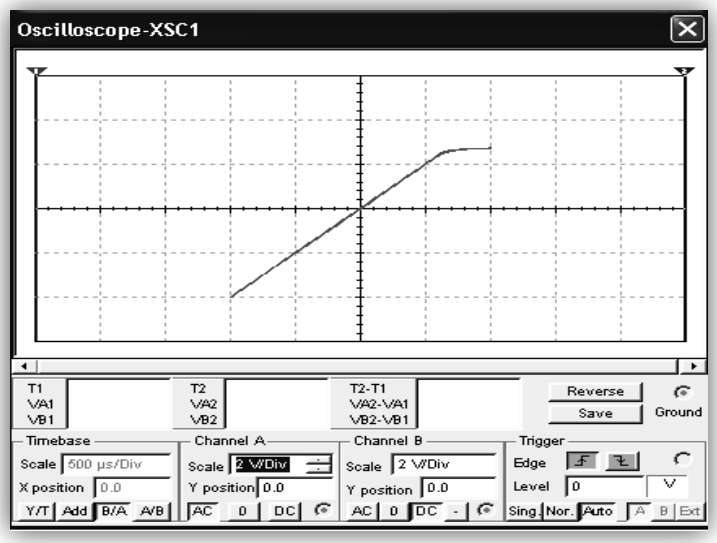
Circuit Diagram:



Input Output Waveform:

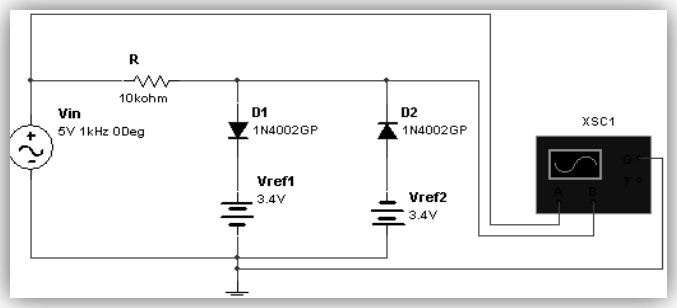


Transfer Characteristics:

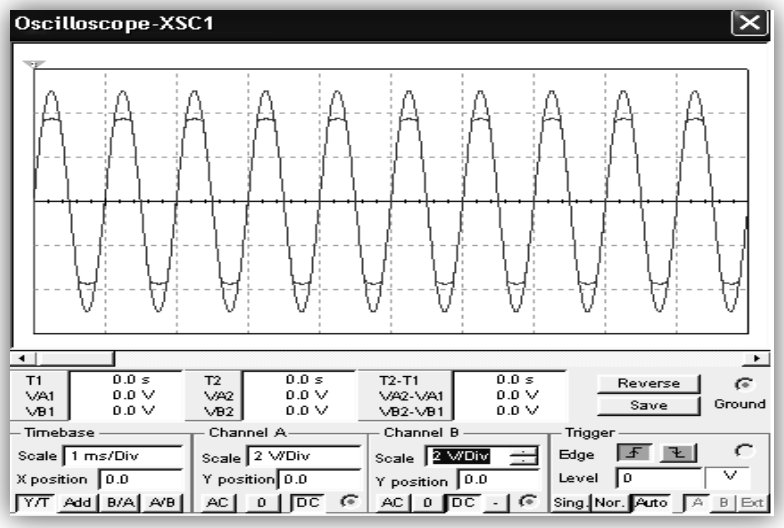


Aim: Testing of Positive Diode Double ended Clipping Circuit.

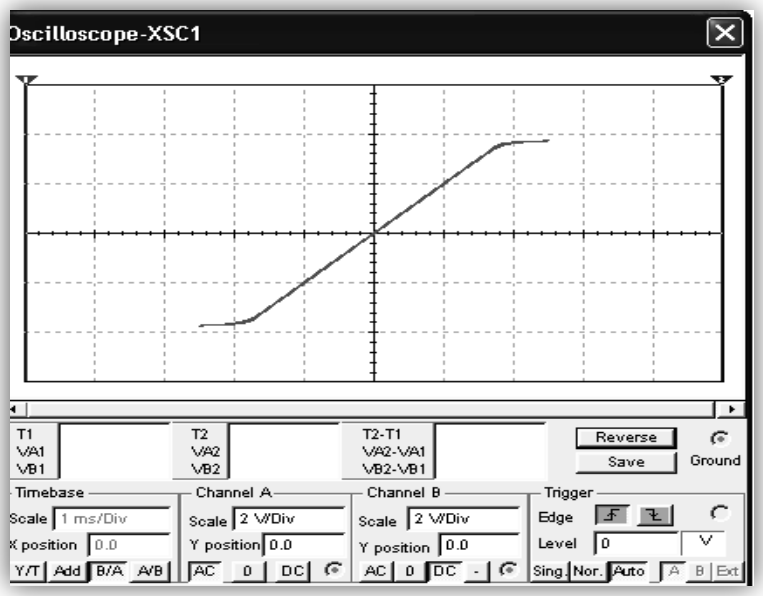
Circuit Diagram:



Input Output Waveform:

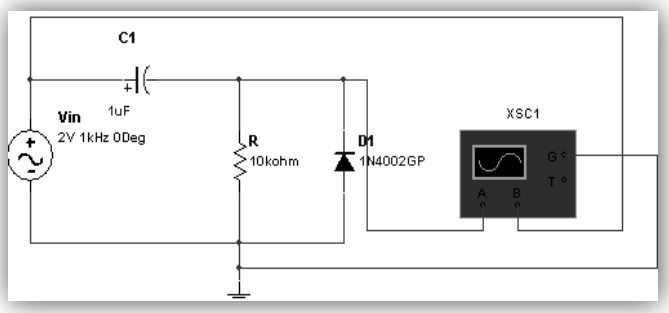


Transfer Characteristics:

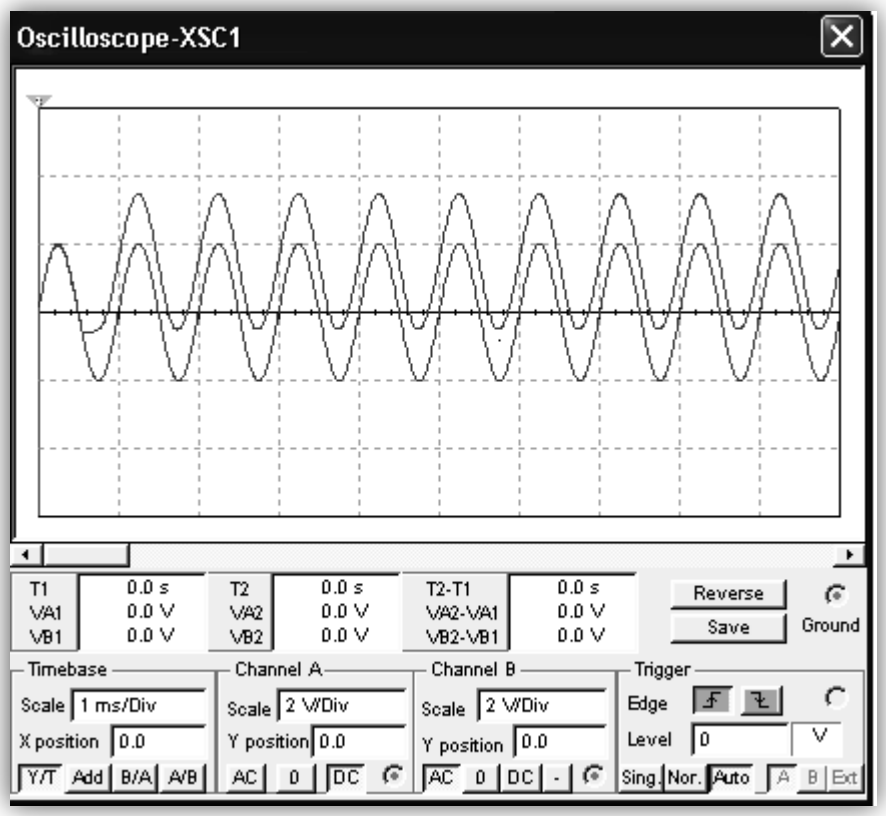


Aim: Testing of Positive Diode Clamping Circuit.

Circuit Diagram:



Input Output Waveform:



Result:

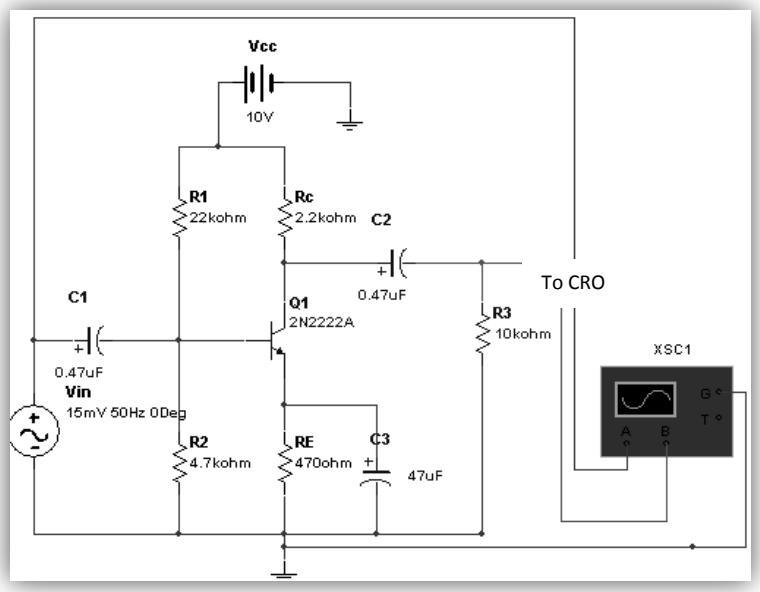
Positive and double ended diode clipping circuits and positive clamping circuits are tested.

Observation:

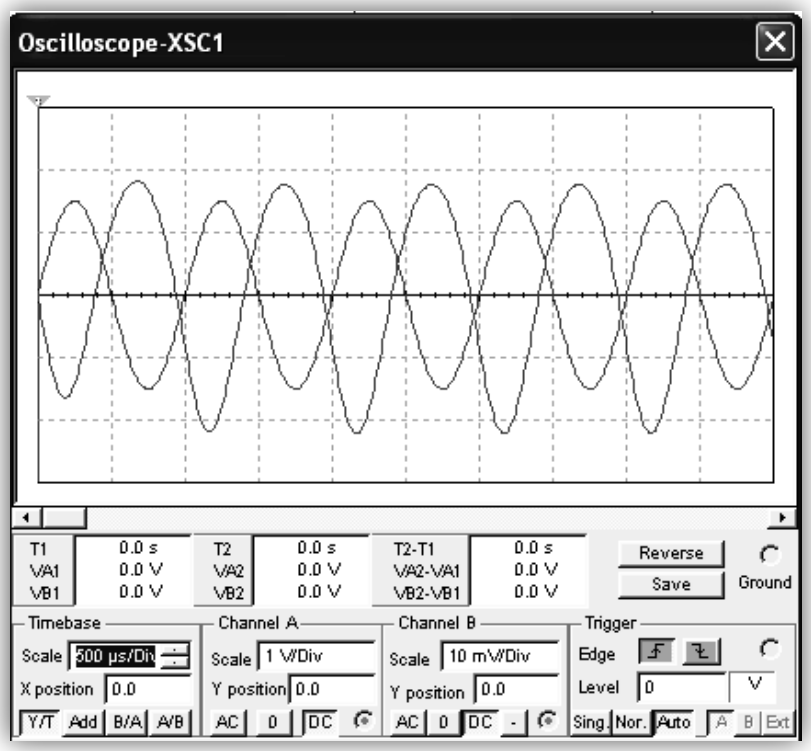
CE Amplifier

Aim: Wiring of RC coupled single stage BJT amplifier and determination of the gain, frequency response, input and output impedances.

Circuit Diagram:

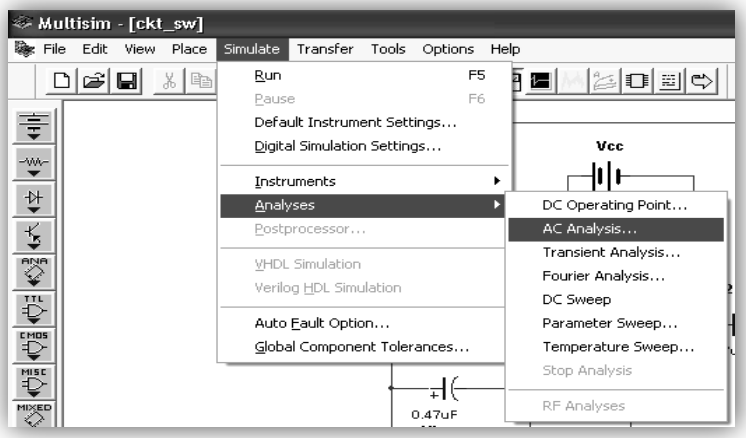


Input Output Waveform:

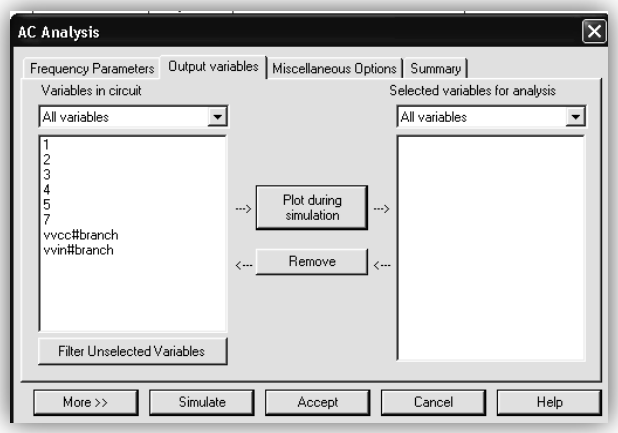


To Find Frequency Response:

Step1:

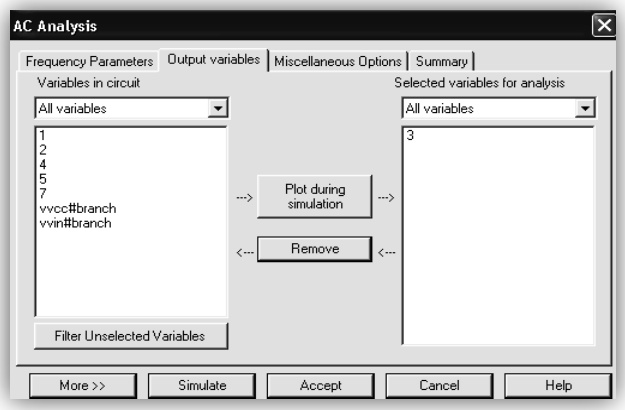


Step 2:

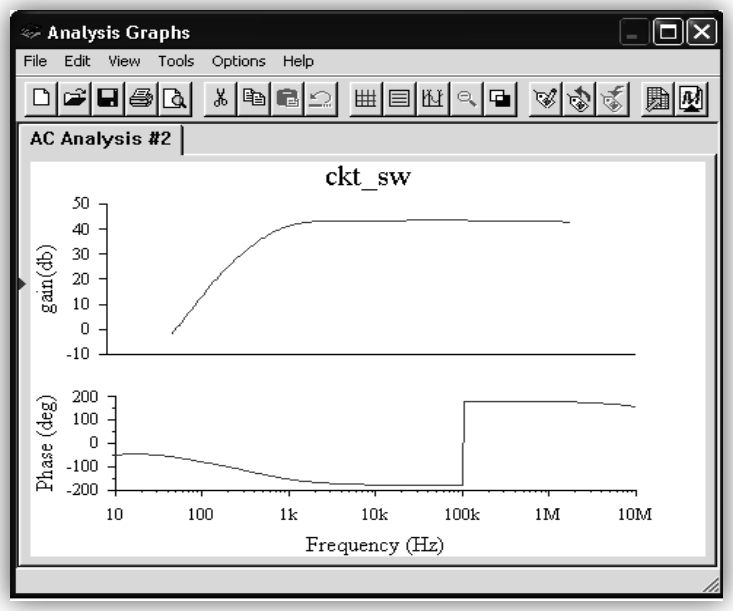


Step 3: Select variable '3'.

Step 4: Click on plot during simulation.

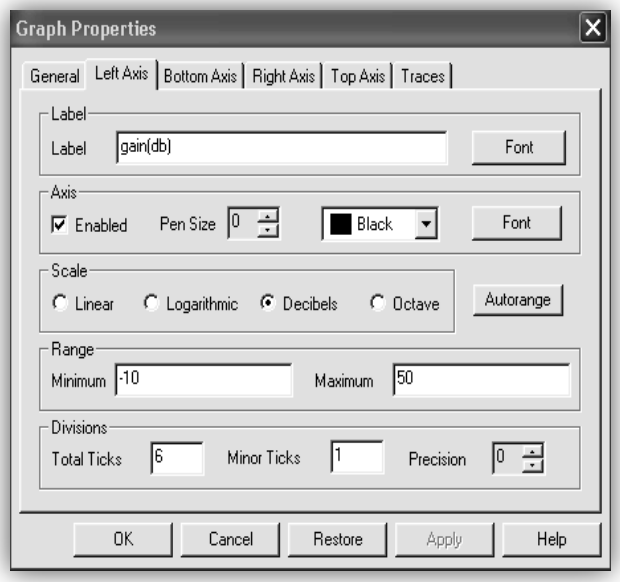


Step 5: Click on Simulate.

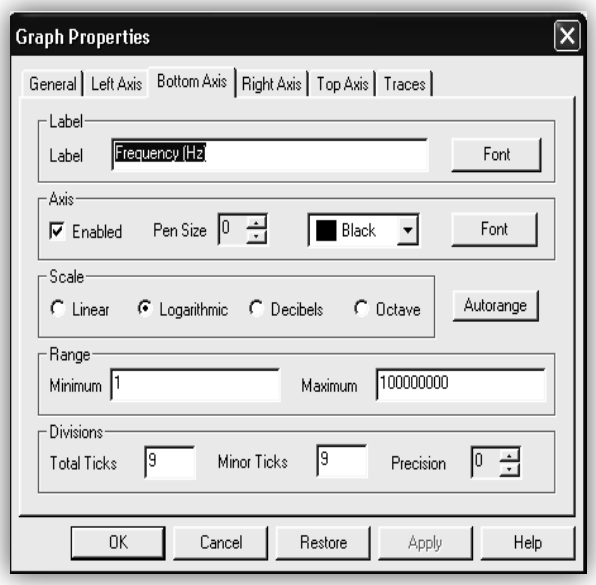


Note:

For x-axis and y-axis adjustments



Right click on the plot



Result:

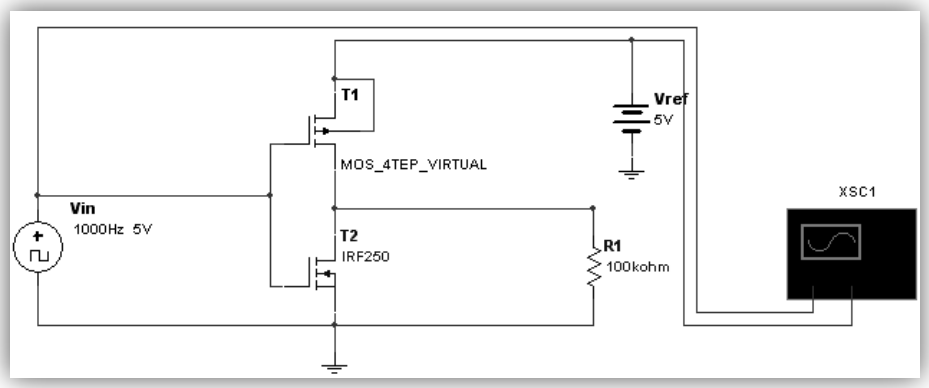
Thus the RC coupled Single Stage BJT amplifiers were wired and the gain frequency response, input and output impedances were determined.

Observation:

COMS Inverter Using MOSFET

Aim : To implement a CMOS inverter using a simulation package and verify its truth table.

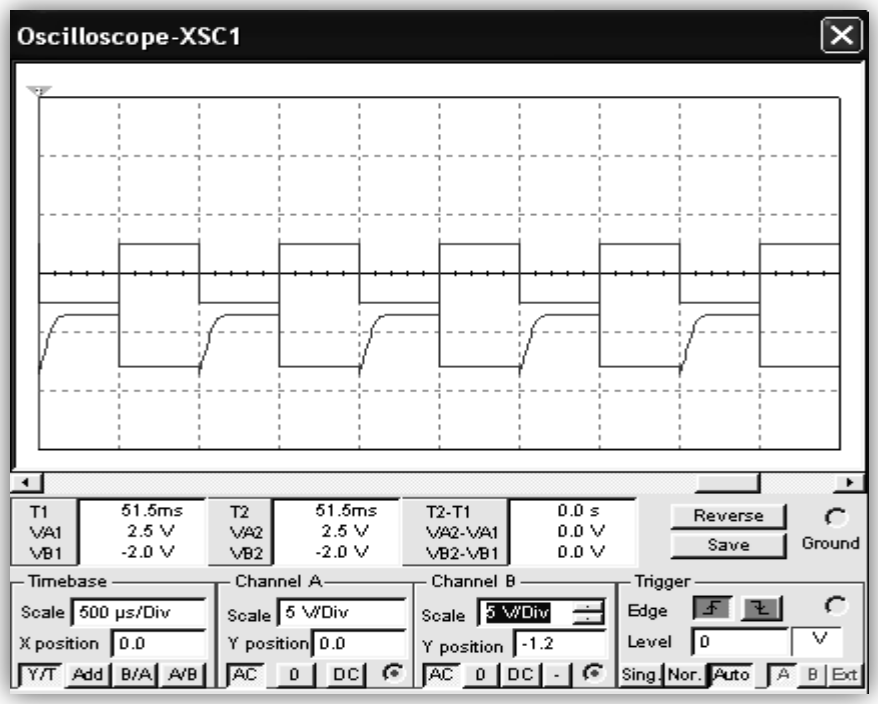
Circuit Diagram :



Truth Table :

Input Vin	Output (CRO)
High	**Low**
Low	**High**

Input Output Waveform :



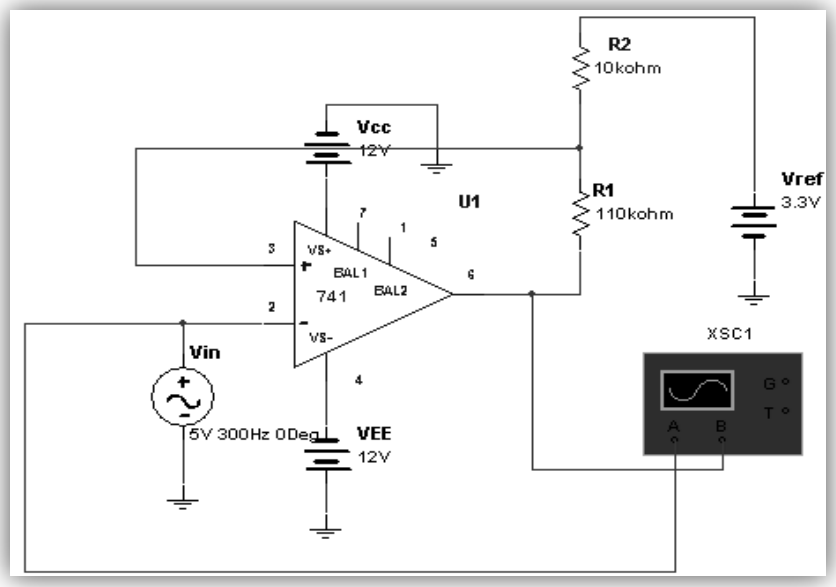
Result : Output is verified according to the truth table.

Observation:

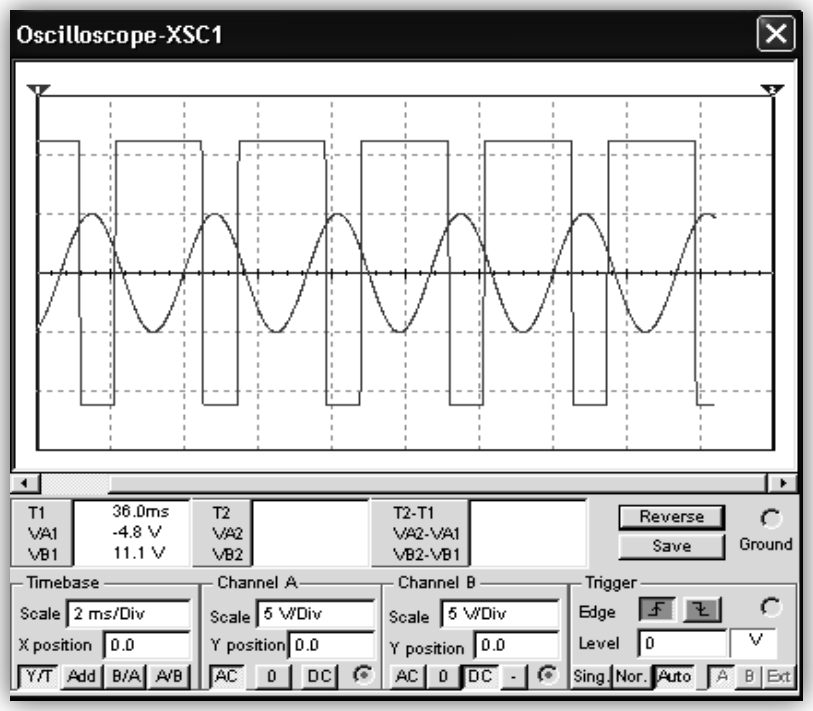
Schmitt Trigger Using Op-Amp

Aim: To design and implement a Schmitt trigger using Op-amp for given Upper Threshold Level (UTL) and Lower Threshold Level (LTL) values.

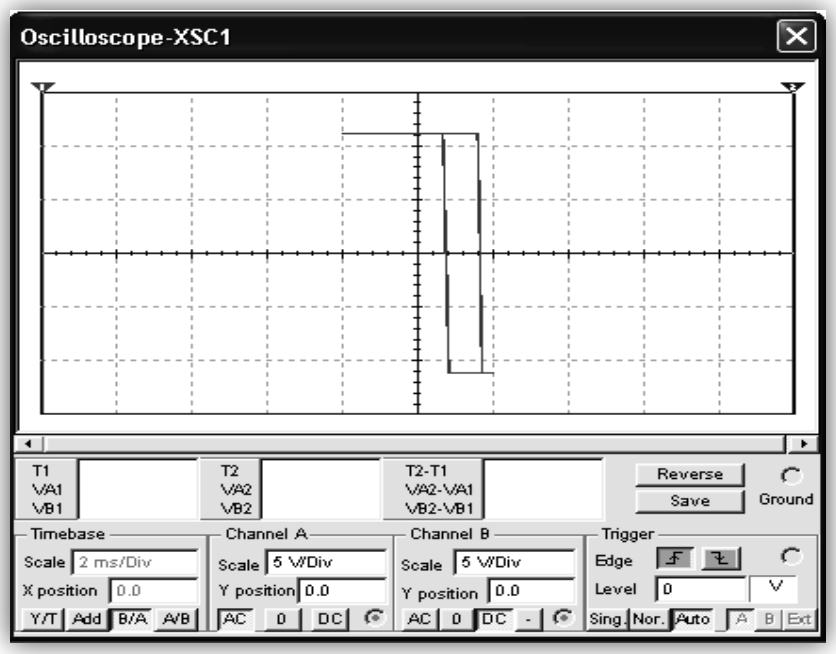
Circuit Diagram:



Input Output Waveform:



Transfer Characteristics:



Result:

The output waveforms are studied for Schmitt trigger and the practical values of UTL and LTL are matching with the theoretical value.

UTL = _____V

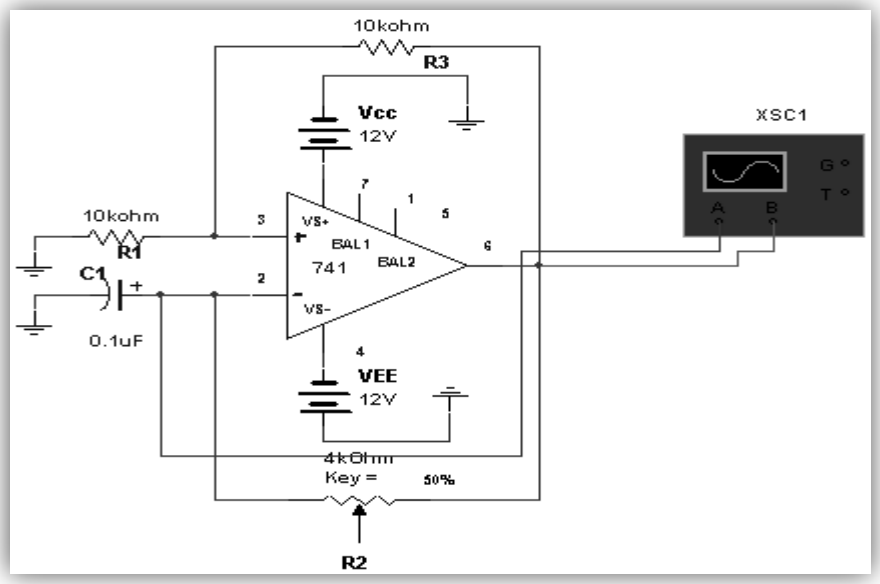
LTL = _____ V

Observation:

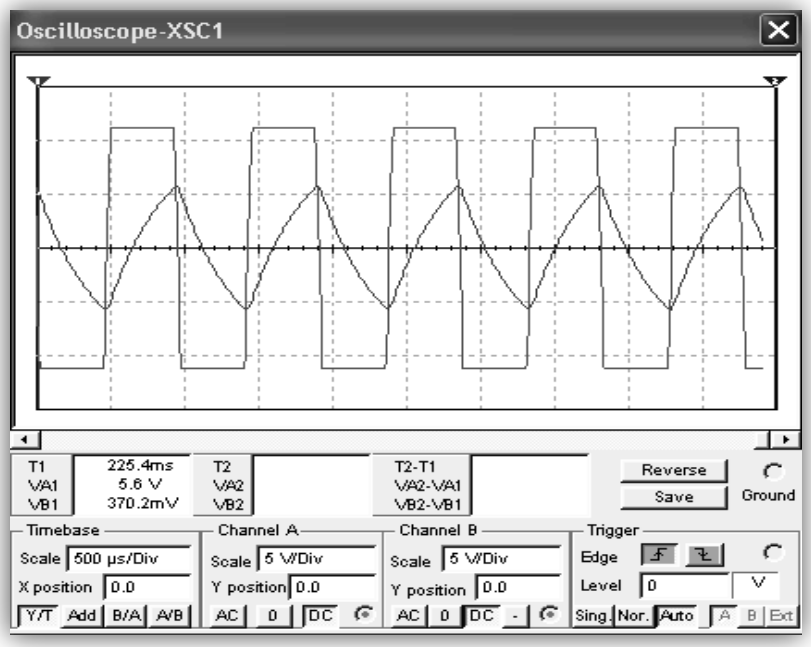
Op-Amp Relaxation Oscillator

Aim: To design and implement a rectangular waveform generator for given frequency.

Circuit Diagram:



Input Output Waveform:



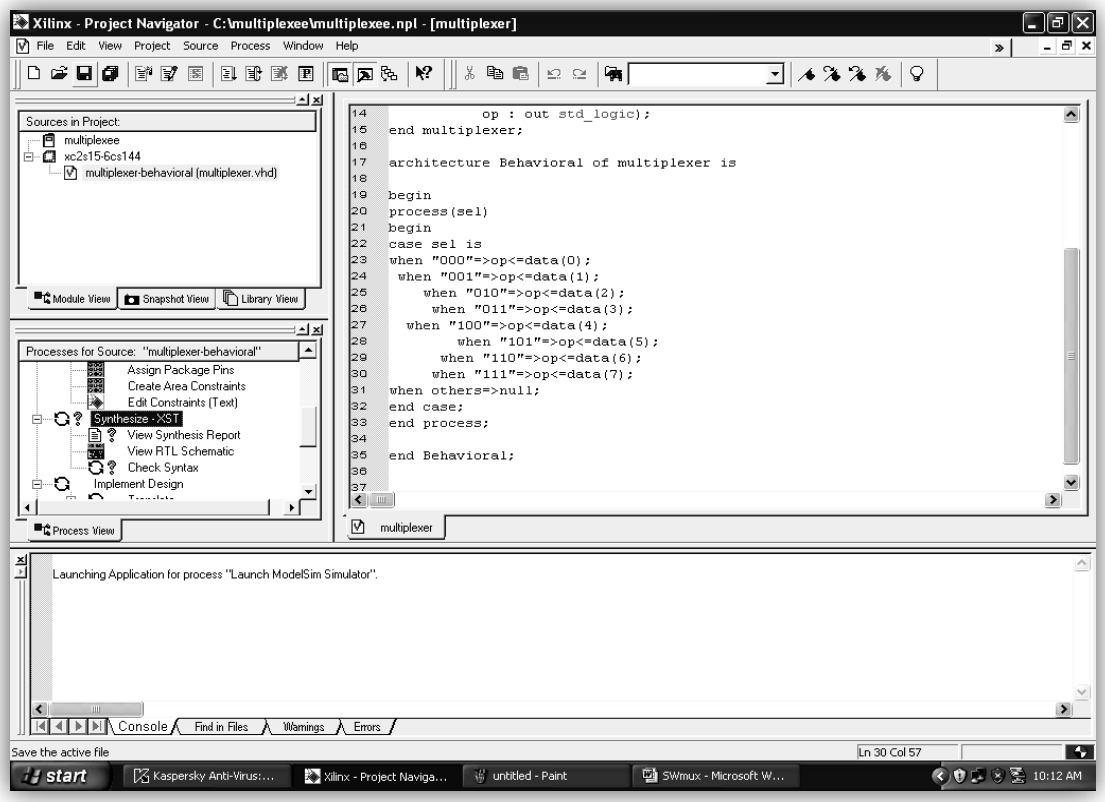
Result:

Relaxation oscillator using op-amp is designed for given frequency and output waveform is observed (square wave).

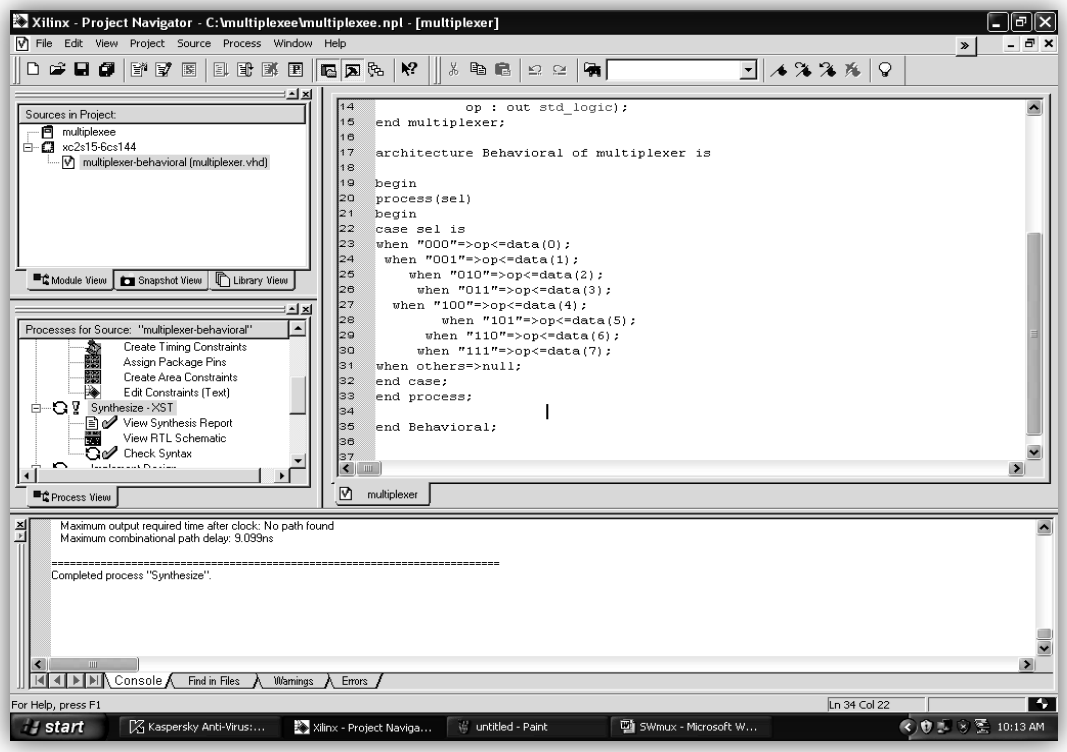
Observation:

Steps to execute an HDL program:

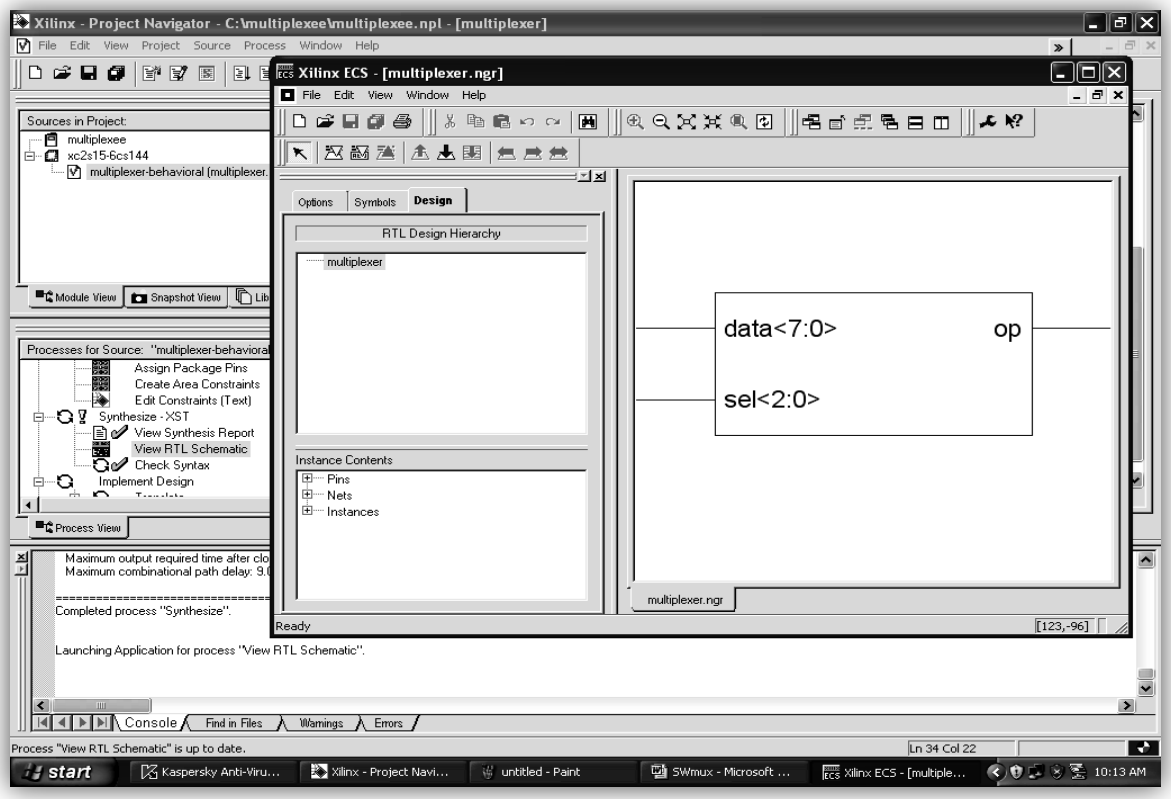
Step1: To synthesize



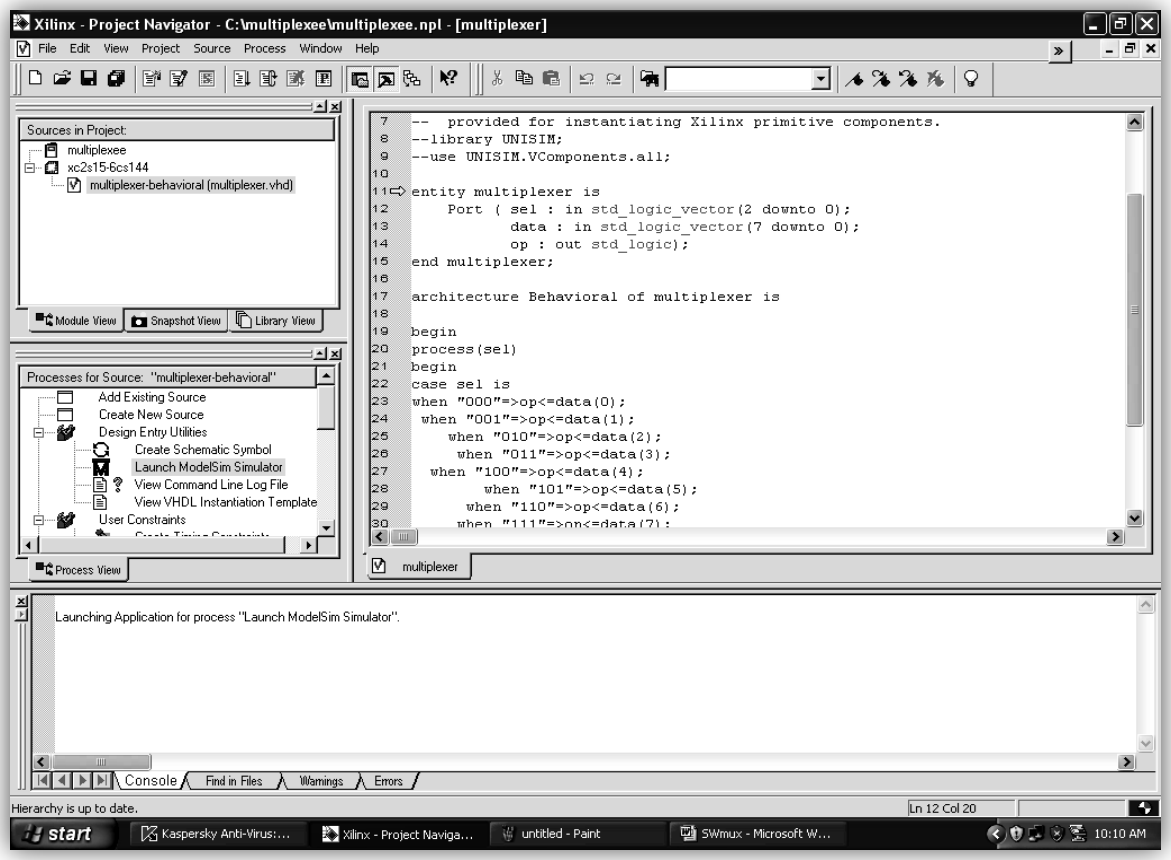
Step2: When synthesis completes successfully



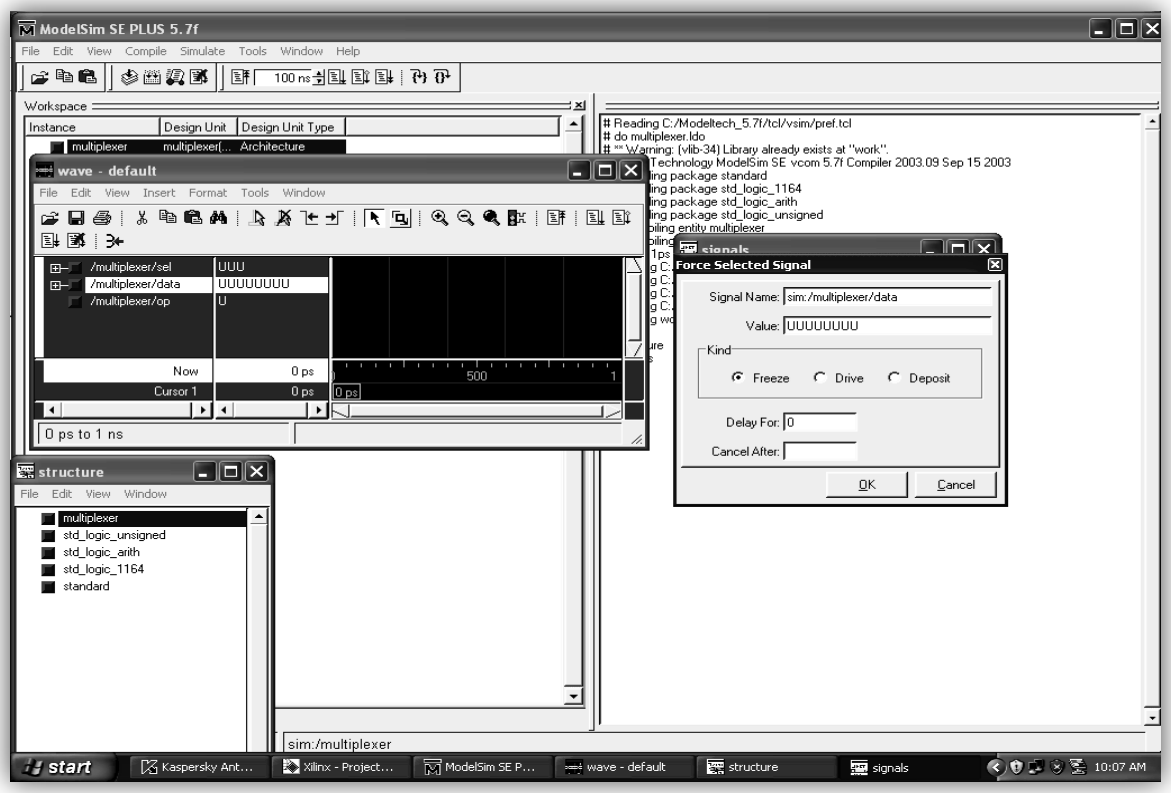
Step3: To view RTL schematic



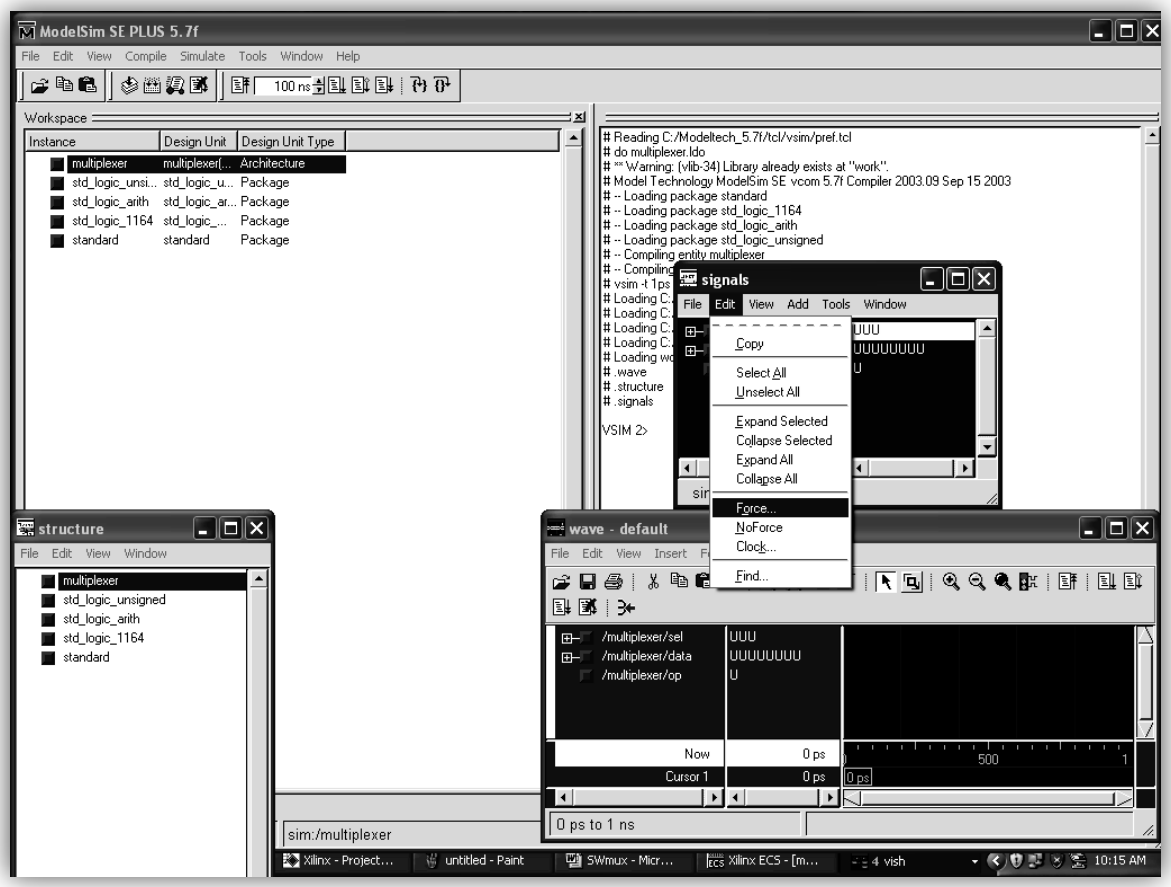
Step4: To view processing waveform



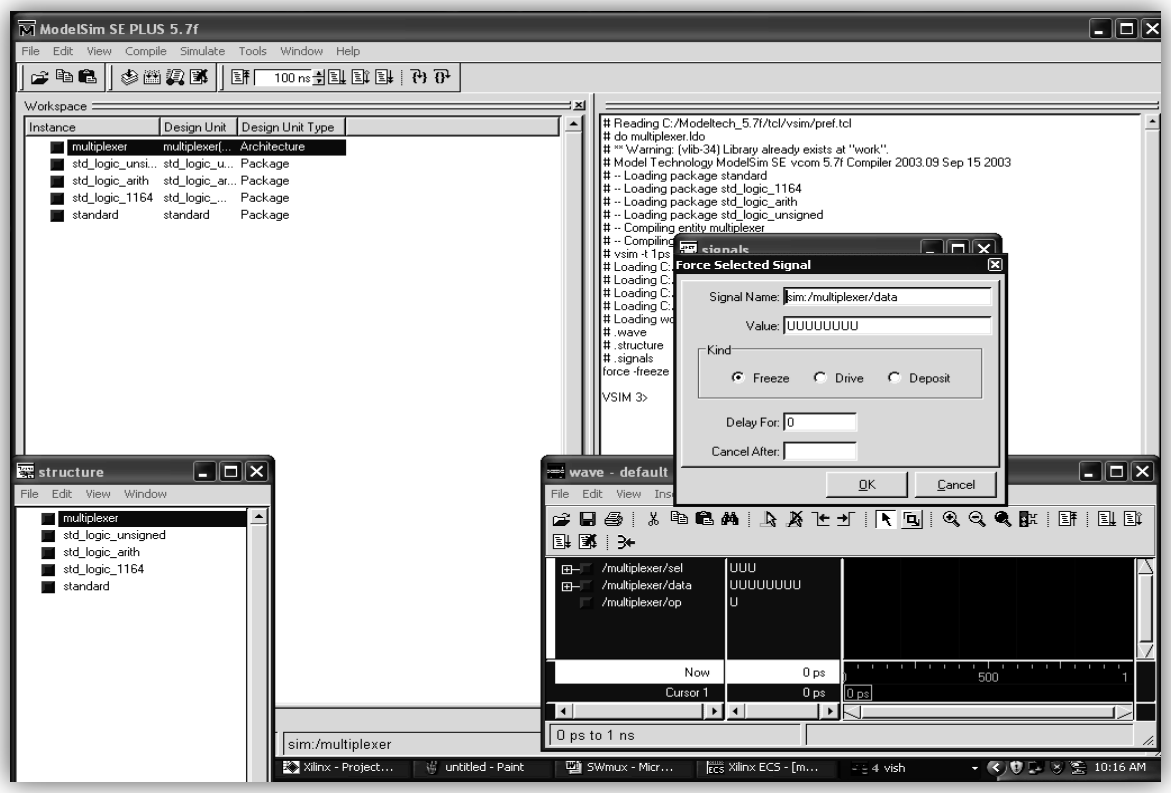
Step5:



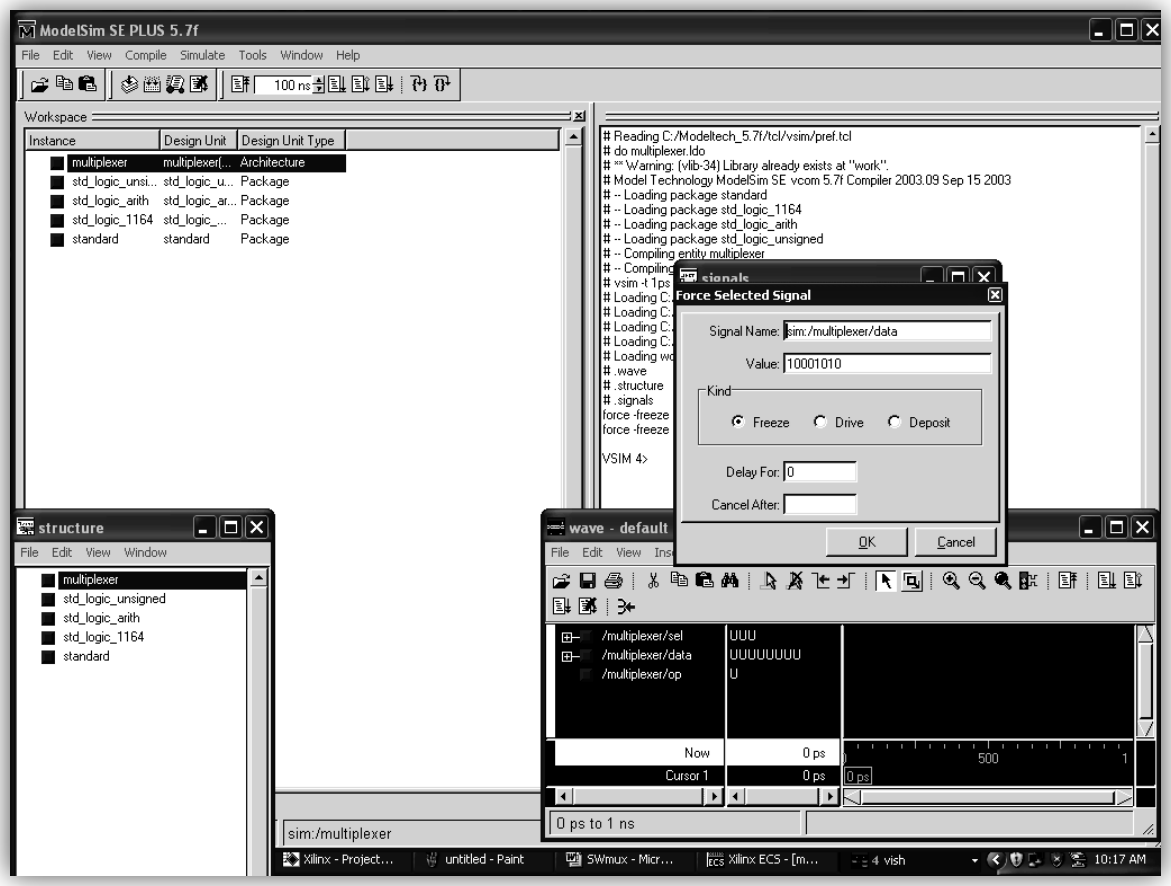
Step6: To force values into the input ports



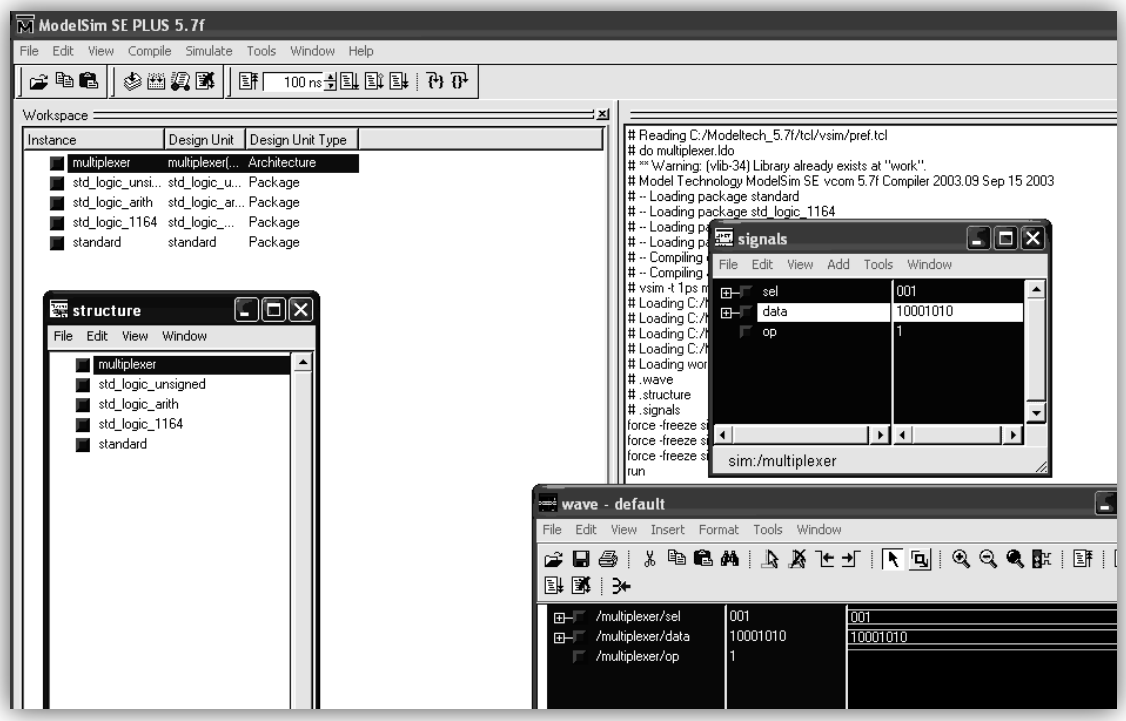
Step7:


ModelSim SE PLUS 5.7f
Force Selected Signal
Signal Name: sim:/multiplexer/data
Value: UUUUUUUU
Kind
Freeze
Drive
Deposit
Delay For: 0
Cancel After:
OK
Cancel
structure
wave - default
/multiplexer/sel
/multiplexer/data
/multiplexer/op
sim:/multiplexer
0 ps to 1 ns

Step8:


ModelSim SE PLUS 5.7f
Force Selected Signal
Signal Name: sim:/multiplexer/data
Value: 10001010
Kind
Freeze
Drive
Deposit
Delay For: 0
Cancel After:
OK
Cancel
structure
wave - default
/multiplexer/sel
/multiplexer/data
/multiplexer/op
sim:/multiplexer
0 ps to 1 ns

Step9:


ModelSim SE PLUS 5.7f
File Edit View Compile Simulate Tools Window Help
Workspace
Instance Design Unit Design Unit Type
multiplexer multiplexer(... Architecture
std_logic_unsi... std_logic_u... Package
std_logic_arith std_logic_ar... Package
std_logic_1164 std_logic_... Package
standard standard Package
structure
File Edit View Window
multiplexer
std_logic_unsigned
std_logic_arith
std_logic_1164
standard
Reading C:/Modeltech_5.7f/tcl/vsim/pref.tcl
do multiplexer.do
** Warning: (vlib-34) Library already exists at "work".
Model Technology ModelSim SE vcom 5.7f Compiler 2003.09 Sep 15 2003
-- Loading package standard
-- Loading package std_logic_1164
signals
File Edit View Add Tools Window
sel 001
data 10001010
op 1
sim:/multiplexer
.wave
.structure
.signals
run
wave - default
File Edit View Insert Format Tools Window
/multiplexer/sel 001
/multiplexer/data 10001010
/multiplexer/op 1

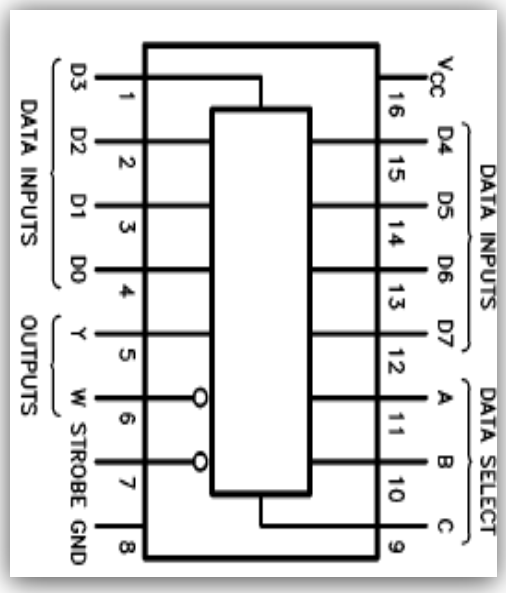
8: 1 Multiplexer

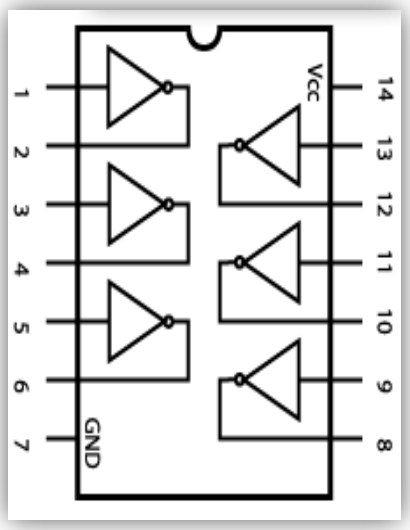
Aim: Given a 4-variable logic expression to smpify using Variable Entered Map and to realize the simplified logic expression using 8:1 Multiplexer.

Components:

Sl.No.	ITEMS	QUANTITY
1	**IC 74151 (8:1 Mux)**	**1**
2	**IC 7404 (NOT Gate)**	**1**
3	**Patch cords**	**20**

Pin Diagram:





Design:

Given a four variable expression,

F = ABCD + ABCD + ABCD + ABCD + ABCD + ABCD

Steps To Simplify Using Variable Entered Map:

1. Write truth table for inputs ABCD with its 16 possible inputs as shown in truth table.
2. Put '1' in 'F' coloumn for the min term (ABCD) present in the above expression.
3. Group similar inputs of ABC with respect different inputs for D.
4. Then based on grouping, if
   - F is 0 & 0, then F is 0
   - F is 1 & 1, then F is 1

- F is 0 & 1, or 1 & 0, then for F=1, check corresponding D, if D = 1, then, F is D, or if D = 0, then, F is D.

5. Then match the D inputs(D0, D1, D2, D3, D4, D5, D6, D7) to F values.
6. The complete truth table is shown below (Table - 1)

Truth Table:

A	B	C	D	F	F	Data input
0	0	0	0	0	0	D0
0	0	0	1	0		
0	0	1	0	1	1	D1
0	0	1	1	1		
0	1	0	0	0	D	D2
0	1	0	1	1		
0	1	1	0	0	D	D3
0	1	1	1	1		
1	0	0	0	1	D	D4
1	0	0	1	0		
1	0	1	0	0	0	D5
1	0	1	1	0		
1	1	0	0	0	0	D6
1	1	0	1	0		
1	1	1	0	1	D	D7
1	1	1	1	0		

Circuit Connections:

1. Draw the circuit diagram using Truth table and pin diagram.
2. Interconnect all data inputs whose F is 0 and connect it to logic input and keep switch in low.
3. Interconnect all data inputs whose F is 1 and connect it to logic input and keep switch in high.
4. Interconnect all data inputs whose F is D and connect it to logic input and keep switch in low.
5. Interconnect all data inputs whose F is D and connect it to logic input through NOT Gate, such that we get D.
6. Make Vcc and GND connections of both IC 74151 and IC 7404.
7. Pin 6 of IC74151 is No Connection.
8. Pin 5 of IC74151 is connected to output logic, to check output (F), for different inputs(ABCD).
9. Pin 7 of IC74151 is connected to GND, such that the IC is strobed.

Circuit Diagram:

Result:

The truth table is verified.

Observation:

1b. Write the VHDL code for an 8:1 Multiplexer. Simulate and verify its working.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity m is
    Port ( i: in std_logic_vector(7 downto 0);
    sel: in std_logic_vector (2 downto 0);
    z: out std_logic);
end m;

architecture Behavioral of m is
begin
    process(sel)
    begin
        case sel is
        when "000"=>z<=i(0);
when "001"=>z<=i(1);
when "010"=>z<=i(2);
when "011"=>z<=i(3);
when "100"=>z<=i(4);
when "101"=>z<=i(5);
when "110"=>z<=i(6);
when "111"=>z<=i(7);
when others=>null;
end case;
end process;
end Behavioral;
```

Observation:

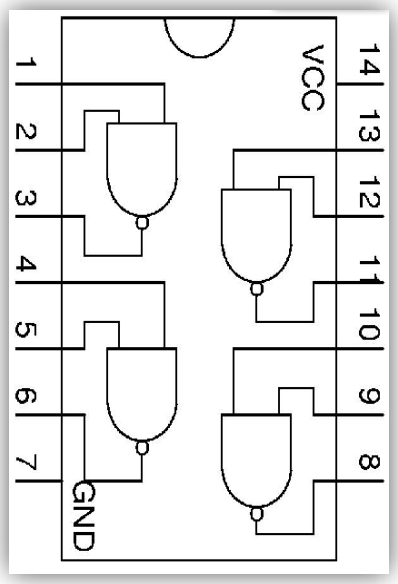
J-K Master / Slave Flip Flop

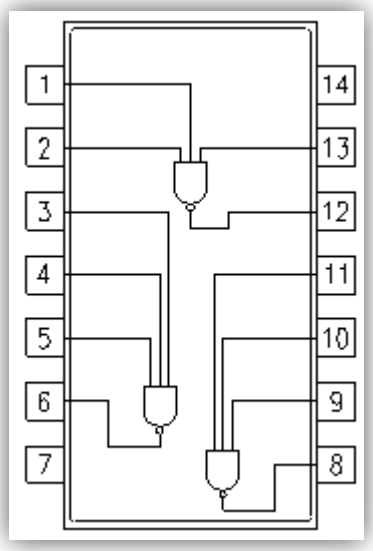
Aim : To realize a J – K Master / Slave Flip Flop Using NAND gates and to verify its truth table.

Components:

Sl.No.	ITEMS	QUANTITY
1	IC 7400(2 input NAND Gate)	2
2	IC 7410 (three input NAND Gate)	1
3	Patch cords	20

Pin Diagram :





J K master-slave flip flop consists of clocked JK flip flop as a master and clocked SR flip flop as a slave. The clock signal is connected directly to the master flip flop but connected through an inverter to the slave flip flop. Therefore the information present at J and K inputs are transmitted to the output of master flip flop on the positive clock pulse and it is held there until the negative clock pulse occurs, after which it is allowed to pass through to the output of slave flip flop.

When J=1, K=0 & positive clock →master is set. The high on y output of master drives S i/p of slave. So at negative clock is set.

When J=0, K=1 and positive clock → master is resets. The high $\bar{y}$ output of master goes to R input of slave. So at negative clock slave is reset.

When J=1, K=1 → master toggles on positive clock & slave then copies the output of master on negative clock.

Truth Table :

CLK	J	K	Q	Q
┌	0	0	Previous Output	
┌	0	1	0	1
┌	1	0	1	0
┌	1	1	Toggle	

Procedure :

1. Verify all components
2. Make connections as in design diagram
3. Connect Vcc and GND of all ICs properly.
4. Give inputs (JK), and then give clock.
5. Observe output after each clock
6. Similarly verify truth table.

Result :

The Truth Table is verified.

Observation:

3b. D Flipflop

```
1   library IEEE;
2   use IEEE.STD_LOGIC_1164.ALL;
3   use IEEE.STD_LOGIC_ARITH.ALL;
4   use IEEE.STD_LOGIC_UNSIGNED.ALL;
5
6   entity ff is
7       Port ( d: in std_logic;
8              clk: in std_logic;
9                   q: inout std_logic;
10                  qbar: out std_logic);
11  end ff;
12
13  architecture Behavioral of  ff is
14  begin
15  process(clk)
16  begin
17          if rising_edge(clk) then
18          q<=d;
19  end if;
20  end process;
21          qbar<=not q;
```

Observation:

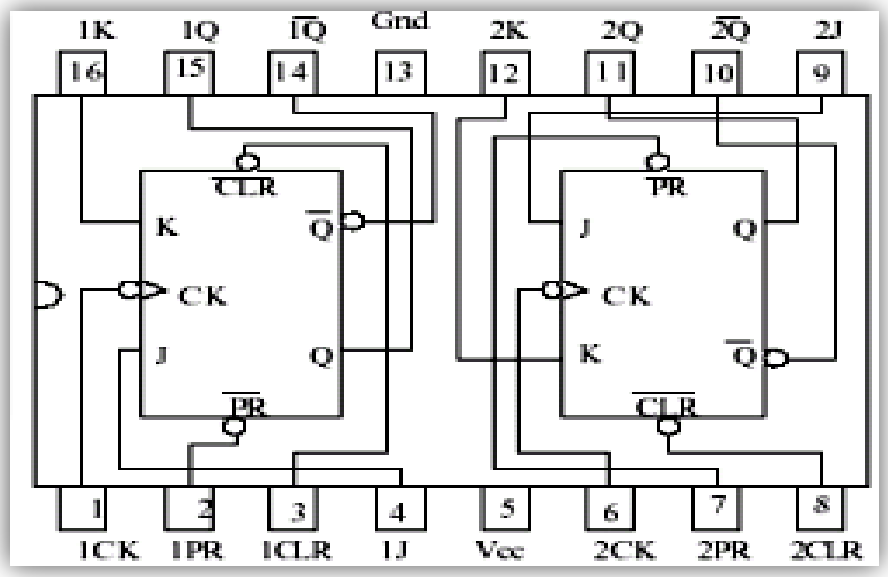
MOD-n Synchronous Up Counter

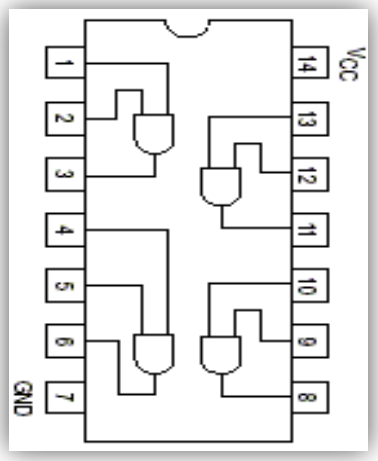
Aim :To design and implement a mod-n synchronous up- counter using JK flip flop.

Components:

Sl.No.	ITEMS	QUANTITY
1	IC 7476 (Flip Flop)	1 or 2
2	IC 7408(AND Gate)	1 or 2
3	Patch cords	20

Pin Diagram:





Truth Table Of J-K Flip Flop:

CLK	J	K	Q	Q
┌	0	0	Previous Output	
┌	0	1	0	1
┌	1	0	1	0
┌	1	1	Toggle	

Design:

1. Check the mod-n value from AIM, then based on 'n' choose the number of IC7476 (flip flops).

   Use formula $m<=2^n$, where, m → number of flip flops.

   Since, in IC7476, 2 flip flops are there, so for every 2 flip flop, choose 1 IC7476.
2. Then, draw the Excitation Table for the given mod-n.
3. With respect to the Excitation Table, derive Output equations for all the flip flops using K-map technique.
4. Then draw the circuit diagram using the flip flops and output equations obtained.

Example:

Excitation Table:

K-Maps:

Circuit Diagram:

Procedure:

1. Make the circuit connections as shown in the circuit diagram.
2. Connect input lines to input logic on trainer kit and output lines to output logic.
3. Then, give clock. For every clock pulse the output logic should count from 0 to mod-n.

Result:

The Excitation Table is verified.

Observation:

4b. Johnson Counter

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity sww is
    Port ( clk: in std_logic;
                    q: inout std_logic_vector(3 downto 0):="0000");
 end sww;

architecture Behavioral of  sww is
begin
process(clk)
begin
        if (clk' event and clk='0') then
        q(3)<=not q(0);
        q(2)<= q(3);
        q(1)<=q(2);
        q(0)<=q(1);
end if;
end process;
end Behavioral;
```

Observation:

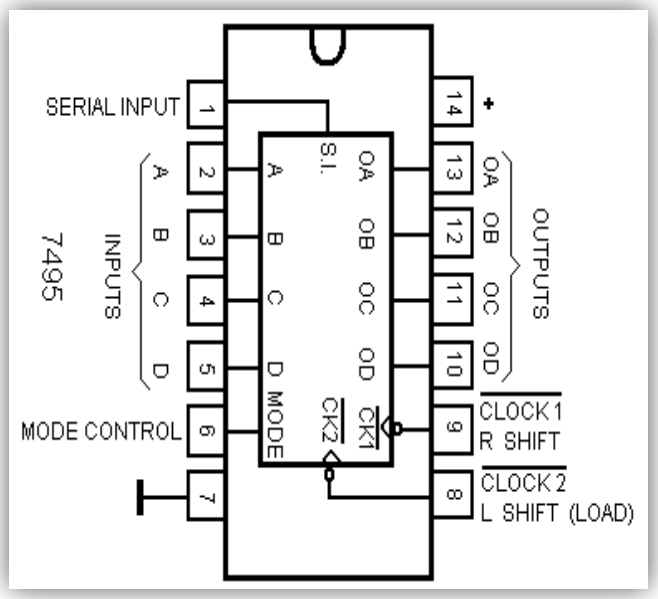
4-Bit Ring Counter

Aim : To design and implement 4 bit ring counter using 4 bit parallel access shift register.

Components:

Sl.No.	ITEMS	QUANTITY
1	**IC 7495 (4-bit parallel shift register IC)**	**1**
2	**Patch cords**	**20**

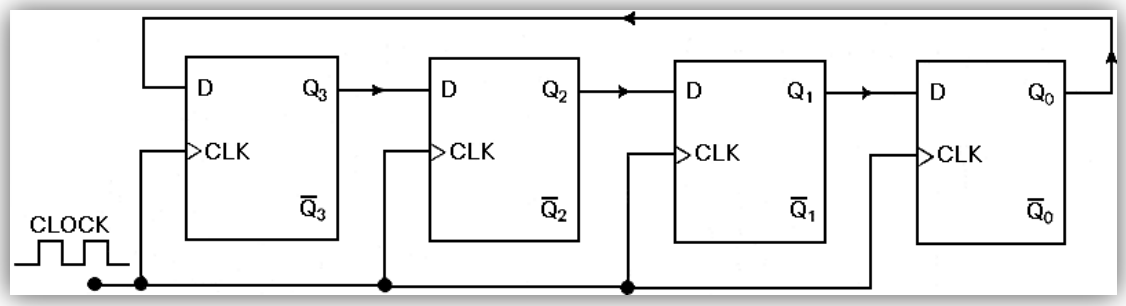
Pin Diagram:



Design:

1. The ring counter is made up of shift registers.
2. Since, according to the AIM, it is 4-bit ring counter, 4 Data flip flops are required, and Hence, 4-bit Shift register is used i.e., 1- IC7495.
3. Since in ring counter operation, the outputs of each flip flop is shifted n-number of times, the output of 1 flip flop is given as input to the next flip flop. Hence, the output of last flip flop is given as input to the serial input pin.
   i.e., Q_D (pin 10) is connected to Serial input (pin 1).
4. To give new inputs to flip flops, give new values to input pins ABCD(pin 2,3,4, and 5), and give a low input to Mode (pin 6). Now the new inputs are stored in 4 flip flops of 4-bit Shift register.
5. Now for every clock pulse the values of the present flip flops will be shifted to the next flip flop.

Circuit Diagram Of Ring Counter:



Circuit Diagram:

Procedure:

1. Make the circuit connections as shown in circuit diagram.
2. Connect input lines and Mode pin to the input logic and output lies to output logic.
3. Give new input values to ABCD (say 1 0 0 0).
4. Then give '0' to Mode pin, then give '1' to Mode pin.
5. Give clock pulse and observe logic outputs for each clock pulse and verify the Truth Table as shown below for the example.

Truth Table:

CLK	Q_A	Q_B	Q_C	Q_D
┌	1	0	0	0
┌	0	1	0	0
┌	0	0	1	0
┌	0	0	0	1
┌	1	0	0	0

Result:

The Truth Table is verified.

5b. Mod-8 Synchronous Up Counter

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3  use IEEE.STD_LOGIC_ARITH.ALL;
4  use IEEE.STD_LOGIC_UNSIGNED.ALL;
5
6  entity m8 is
7      Port ( clk: in std_logic;
8             clk: in std_logic;
9                  q: inout std_logic_vector(2 downto 0):="000");
10  end m8;
11
12 architecture Behavioral of  m8 is
13 begin
14 process(clk,clk)
15 begin
16         if ( clk='0') then
17         q<="000";
18         elseif (clk'event and clk='0') then
19         q<=q+'1';
20 end if;
21 end process;
22 end Behavioral;
```

Observation:

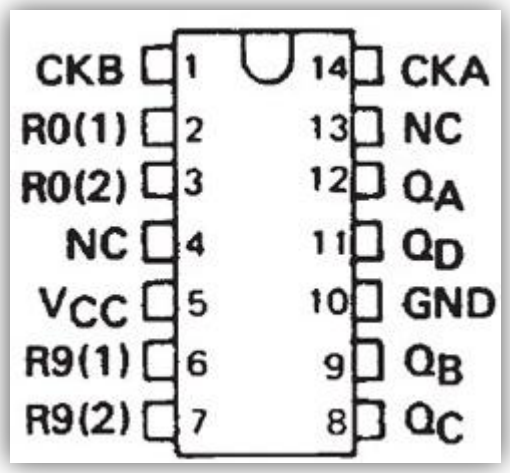
Asynchronous Counter Using Decade Counter

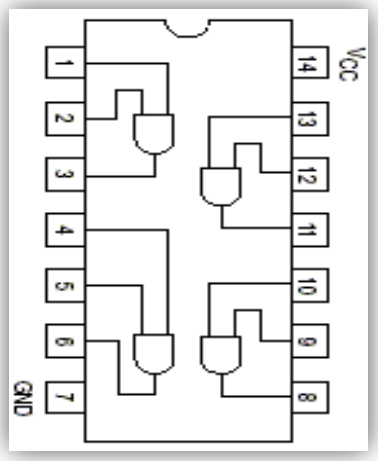
Aim : To design and implement an Asynchronous Counter using a decade counter to count up from 0 to n (n>0) and display count on 7 segment LED.

Components:

Sl.No.	ITEMS	QUANTITY
1	IC 7490 (Decade Counter IC)	1
2	IC7408 (AND Gate IC)	1
3	Patch cords	20

Pin Diagram:





Design:

Consider an example of mod-6 counter.

1. For mod 6, counter is to be reset, when count reaches 0110 (decimal equivalent 6). Hence, outputs Q_B, Q_C of the counter are given to its reset pins 2,3 where Q_A, Q_B, Q_C, Q_D (MSB) are outputs.
2. The output of 7-segment code counter is given to 7-segment LED display.
3. Apply manually operated clock pulses at the clock terminal (pin 14). Apply asynchronous clock pulses from output (Q_A) to the clock input (pin1).

Circuit Diagram:

Procedure:

1. Make connections as shown in circuit diagram
2. Connect Q_A(pin 12) to pin 1, Q_B(pin 9) to Reset pin(pin 2), Q_C(pin 8) to reset pin(pin 3), pin 5 to Vcc, pin 6 & 7 to GND, pin 10 to GND, pin 14 to CLK.
3. Connect all output pins to output logic.
4. Apply manually operated clock pulses at the clock terminal (pin 14), and verify the Truth Table shown below for each clock pulse.

Q_D	Q_C	Q_B	Q_A	a	b	C	d	e	f	g	h	7- Segment display
0	0	0	0	1	1	1	1	1	1	0	0	0
0	0	0	1	0	1	1	0	0	0	0	0	1
0	0	1	0	1	1	0	1	1	0	1	0	2
0	0	1	1	1	1	1	1	0	0	1	0	3
0	1	0	0	0	1	1	0	0	1	1	0	4
0	1	0	1	1	0	1	1	0	1	1	0	5
0	1	1	0	1	0	1	1	1	1	1	0	6
0	1	1	1	1	1	1	0	0	0	0	0	7
1	0	0	0	1	1	1	1	1	1	1	0	8
1	0	0	1	1	1	1	0	0	1	1	0	9

Result:

The truth table is verified for the given mod-n.

Observation:

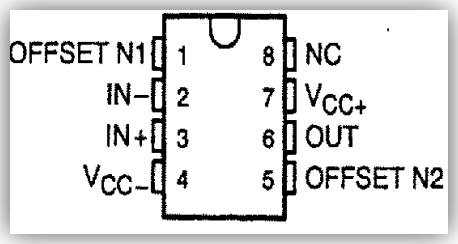
R-2R Ladder DAC

Aim : Design a 4-bit R -2R ladder D/A converter using Op-Amp and determining its accuracy and resolution.

Components:

Sl.No.	ITEMS	QUANTITY
1	IC 741 (Op-Amp IC)	1
2	2.2KΩ Resistors	6
3	1KΩ Resistors	3
4	Bread Board	1
5	Single Strand connecting wires	15
6	Patch cords	10
7	Digital Multimeter	1

Pin Diagram:



Theory:

A digital to analog converter (DAC) converts digital data into analog data. That is binary input data is converted to analog voltage or current. R -2R ladder is the method by which binary data is translated to suitable analog data.

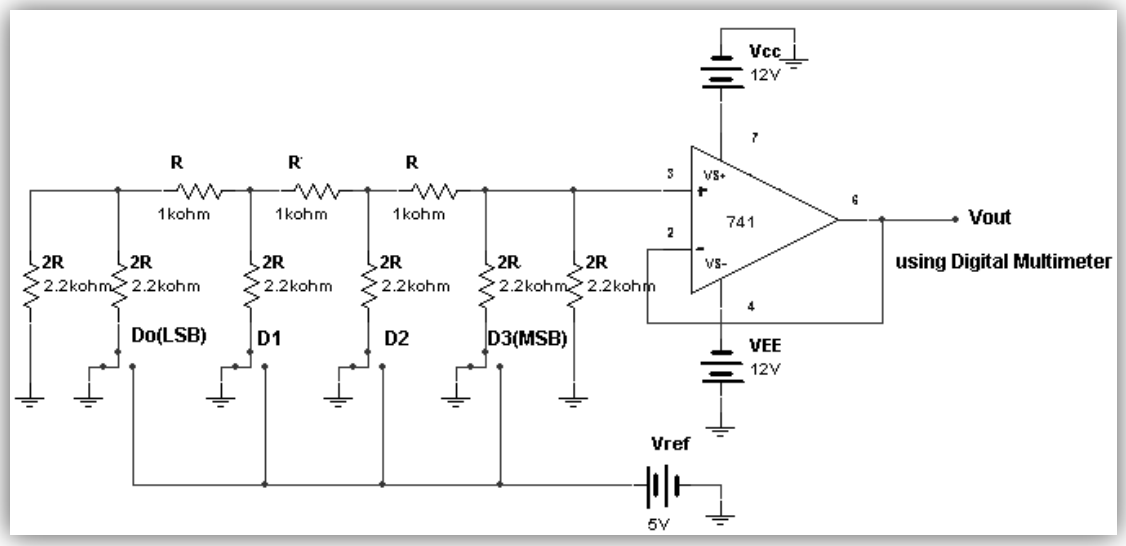
Resolution or step size: The smallest analog voltage circuit can provide when only the LSB is 1. If 'V' represents the binary state '1'. The step size = $V / 2^n$ where 'n' is the number of bits of input data. For an 8-bit DAC with V = 5, the step size will be equal to 20 mV.

Voltage corresponding to MSB = V / 2 , irrespective of the size of DAC. Full scale voltage, V_{FS} = V – step size.

Offset Error: When all inputs to Op- Amp are zero, a small voltage may appear as output. The error introduced to this fact is called the offset error expressed in terms of voltage.

Accuracy : The difference between expected and measured output voltage of the DAC is called the accuracy. As per design, accuracy should be within + ½ or – ½ of LSB.

Circuit Diagram:



Design:

Output voltage $V_0 = V\,[2^3 D_3 + 2^2 D_2 + 2^1 D_1 + 2^0 D_0]$

But

$$V = \frac{V_R}{2^4} \times \frac{2R}{3R}$$

Resolution $= \frac{V_R}{24} = \frac{5}{24} = 0.2.83V$

When $D_3 = D_2 = D_1 = D_0 = 1$, $V_{0(max)} = 5 \times \frac{15}{24} = 3.125V$

When $D_3 = D_2 = D_1 = D_0 = 1$, $V_{0(min)} = 5 \times \frac{1}{24} = 0.2083\ V$

Tabular Column:

Values of 4-bit DAC

Decimal Equivalent	Output	Analog Output Voltage V_0 (V)
	D_3 D_2 D_1 D_0	**Theoretical**
0	0 0 0 0	**0**
1	0 0 0 1	**1V = 0.20833**
2	0 0 1 0	**2V = 0.4166**
3	0 0 1 1	**3V = 0.625**
4	0 1 0 0	**4V = 0.833**
5	0 1 0 1	**5V = 0.10416**
6	0 1 1 0	**6V = 1.25**
7	0 1 1 1	**7V = 1.45**
8	1 0 0 0	**8V = 1.66**
9	1 0 0 1	**9V = 1.875**
10	1 0 1 0	**10 V= 2.08**
11	1 0 1 1	**11 V =2.29**
12	1 1 0 0	**12V = 2.5**
13	1 1 0 1	**13 V = 2.708**
14	1 1 1 0	**14 V =2.916**
15	1 1 1 1	**15 V = 3.125**

Procedure:

1. Rig up the circuit as per the diagram.
2. Energize the Op- Amp pin number 4 with -12 V and pin number 7 with +12 V.
3. D3 ,D2 ,D1 ,D0 are the digital inputs. When ‘ 0’ no voltage flows, when ‘1’ flow of voltage present.
4. Set the input to required state and measure the output voltage with a digital multimeter.
5. Draw straight line graph of output voltage (y-axis) and the digital input (x-axis) of expected and measured values.
6. Verify theoretical values with practical values and observe outputs.

Result:

The tabular column is verified.

Observation: