# A survey on memristor-based ternary logic gates

Mehtab Singh
*Industrial and maritime systems*
*University of South-Eastern Norway*
Kongsberg, Norway
140411@student.usn.no

***Abstract*—Moore's law is gradually failing due to complications manufacturing smaller and smaller transistors [1]. On the contrary, this gives rise to other emerging technologies utilizing memristors and ternary-based systems, reported to have certain advantages over their binary equivalents. This paper aims to discuss present memristor-based ternary logic gate models that rise new, ternary-based computing architectures.**

***Index Terms*—Memristor, ternary, CNTFET, MOSFET, logic gate**

## I. Introduction

Modern digital systems utilize 2-base (binary radix) number system to carry out all low-level computation behind the scenes, making our day-to-day life seamless with technology. Intel Corporation co-founder Gordon Moore [2] projected Moore's law in 1965; the number of transistors in a integrated circuit (IC) would double every year, inherently predicting the increasing complexity, smaller unit of space and less cost of ICs. However, the projection is gradually failing due to complications in manufacturing smaller and smaller transistors [1] [3] [4]. What will carry the next paradigm shift in technological development? The end of Moore's law will raise need for a evolutionary step in technology. Memristors and MLV (multi-valued logic) shows promising potential as foundation for next-generation technology. As part of this foundation, 3-base (ternary radix) number system has proven a strong candidate as platform for post-binary technology since ternary radix has the lowest average radix economy [5]. In other words, for all positive radix $b$, number representation in $b = 3$ will on average be able to use least amount of digits to represent any number. For computer systems, this means fewer wire-connections to transmit data compared with binary radix. For further information on advantages of using ternary radix for computing systems, see [6].

The most fundamental pieces of digital electronics are arguably basic logic gates; functions that constitute larger circuits and therein more complex electronic architectures. Modern constituent of logic gates include metal-oxide-semiconductor field-effect transistors (MOSFETs) and diodes. However, MOSFETs and its conventional way of modeling, CMOS (Complementary metal–oxide–semiconducto), is currently being semi-superseded by hybrid- or pure modeling of carbon nanotube field-effect transistors (CNTFETs). For further information on MOSFET, CMOS and CNTFET, see [7] [8] [9] respectively.

As the binary number system comprises two possible states a digit can represent at a single instant - $\{1, 0\}$, the ternary number system introduces a third state. It is possible to model the ternary number system through the *balanced* convention, meaning the set of possible states is $\{-1, 0, 1\}$, or the *unbalanced convention* - $\{0, 1, 2\}$. Moreover, each of these modeling conventions have advantages and disadvantages with respect to each other. A unbalanced ternary number with N digits can represent $3^N$ positive integers (incl. 0). A balanced ternary number with N digits has the same informational bandwidth, however, the bandwidth is divided for positive (incl. 0) + negative integers; $3^N = \frac{3^N+1}{2} + \frac{3^N-1}{2}$. This enables the balanced convention to represent negative and positive integers without a sign digit, while the unbalanced convention deploys the whole bandwidth to represent positive integers.

Furthermore, the ternary number system has previously been utilized in the development of Setun by Moscow State University in 1958; inexpensive computer suitable for academic- and semi-industrial work [10]. However, mass-production of Setun was halted in favor of a binary-based computer. For further information on favoring of binary number systems for computer systems in mid 1950s, see [11]. The electronic hardware architecture of Setun consisted of "(...) miniature ferrite cores and semiconductor diodes to implement threshold logic and its ternary version (...)" [10]. However, the memristor presents another way of implementing multi-valued threshold logic, and its ternary-version (applicable for ternary-based systems).

Leon Ong Chua identified the *memristor* in 1971 [12] - the "missing, fourth fundamental circuit element". He defined its unit as memristance and reasoned that the newfound element bridges the relational gap between magnetic flux and electric charge as seen in Fig. 1 [13]. In 2014, Leon O. Chua published another paper [14] providing "(...) in depth review of the memristor from a rigorous circuit-theoretic perspective, independent of the material the device is made of.", defining the memristor;

”(...) any two-terminal black box is called a memristor if, and only if, it exhibits a pinched hysteresis loop for all bipolar periodic input current signals (resp., input voltage signals) which result in a periodic voltage (resp., current) response of the same frequency, in the voltage–current (v–i) plane.” [14]

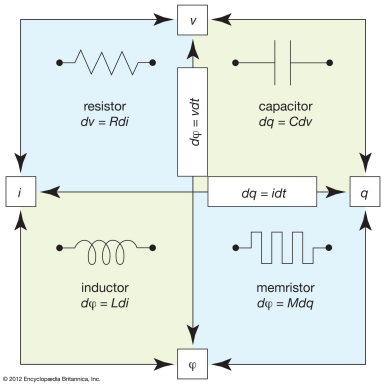


Fig. 1: Fundamental circuit elements

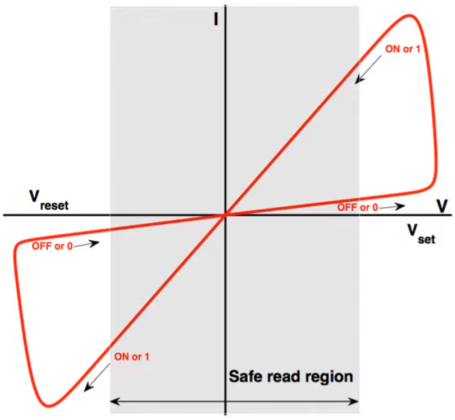


Fig. 2: Pinched hysteresis loop for bipolar input voltage signal

The purpose of this survey is to discuss and summarize recent research and development of memristor-based ternary logic gates. Logic gates constitutes larger electronic circuitry and devices, which makes investigation into stated logic gates interesting in perspective of future technology. This paper is suitable for undergraduates and others who want to enter into the developing field of memristors and their usage in logic gates.

In the first section, a brief introduction of ternary number system and memristor has been provided. Secondly, survey findings are presented in section II. Section III consists of a discussion of survey findings. Section IV comprises of future work, and last section V presents the conclusion.

## II. Survey findings

The basic logic gates in binary computation includes AND, OR and NOT, which can further be used to construct NAND, NOR, XAND and XOR gates. At state-of-the-art level, we can construct equivalent ternary logic gates by utilizing memristors. It is worth noting that for radix 3, the number of possible 2-ary functions are given:

$$F_r(R, A) = R^{R^A} = 3^{3^2} = 19683 \quad (1)$$

While for radix 2, possible 2-ary functions are given:

$$F_r(2, 2) = R^{R^A} = 2^{2^2} = 16 \quad (2)$$

While it is possible to implement all 27 univariate ternary functions using a memristor [15], a vast number of 3-base, 2-ary functions are still unmapped, but of great interest in terms of logic gates. It is possible to define a majority of these functions using the basic logic gates already known. A proposal for some of the basic, memristive logic gates is given in [16]. The ternary OR (TOR) logic is defined as a maximum function of all its inputs:

$$X_1 TOR X_2 ... TOR X_n = MAX(X_1, X_2, ..., X_n) \quad (3)$$

On the contrary, the ternary AND (TAND) logic is defined as a minimum function of all its inputs:

$$X_1 TAND X_2 ... TAND X_n = MIN(X_1, X_2, ..., X_n) \quad (4)$$

The logic of both these basic ternary gates utilizes a VTEAM [17] memristor in series organisation, depicted in Fig. 4 and Fig. 5 [16]. TOR gate architecture in Fig. 4 functions as follows; when input voltages are applied to both memristors, the memristor with the largest input voltage switches to $R_{on}$ (low memristance), while the memristor with smallest input voltage switches to $R_{off}$ (high memristance). See Fig. 2 for reference. The output voltage adopts the voltage of the memristor with lowest memristance, in other words the highest input voltage is represented at the output. In addition, [18] presents a logic gate capable of computing the average value of voltage inputs, See Fig. 3:

$$TAvg(v_1, v_2, ..., v_n) = \frac{(v_1 + v_2 + ... + v_n)}{n}$$

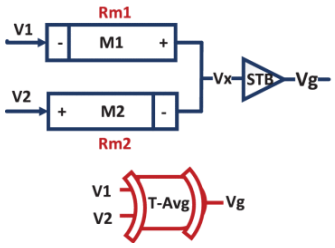


Fig. 3: Average-value computing logic gate

TABLE I: Truth table for ternary inverters

| Ternary inverters | | | | | | | |
|---|---|---|---|---|---|---|---|
| Balanced ternary | | | | Unbalanced ternary | | | |
| Input | NTI | PTI | STI | Input | NTI | PTI | STI |
| -1 | 1 | 1 | 1 | 0 | 2 | 2 | 2 |
| 0 | -1 | 1 | 0 | 1 | 0 | 2 | 1 |
| 1 | -1 | -1 | -1 | 2 | 0 | 0 | 0 |

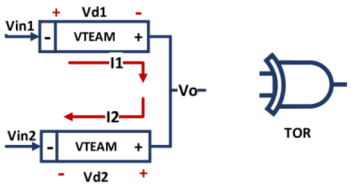


Fig. 4: TOR gate

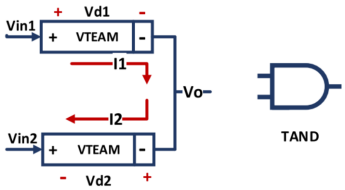


Fig. 5: TAND gate

TAND gate architecture in Fig. 5 functions as follows; when input voltages are applied to both memristors, the memristor with the lowest input voltage switches to $R_{on}$ (low memristance), while the memristor with largest input voltage switches to $R_{off}$ (high memristance). See Fig. 2 for reference. The output voltage adopts the voltage of the memristor with highest memristance, in other words the lowest input voltage is represented at the output. Furthermore, ternary inverters can be designed by utilizing memristors and CNTFETs [16]. Table I shows the truth table for negative-, positive- and standard ternary inverters.

The proposed ternary logic gates for ternary NOR and NAND (TNOR, TNAND) in [16] and [19] are comprised by CNTFETs and memristors. The hybrid combination of next-generation field-effect transistors and memristors is claimed to nullify the loading-effect on the memristive circuit which would consist of many cascaded memristors (in order to build higher level gates). In order to nullify the loading-effect, a buffer consisting of two CNTFET-based NTI/PTI gates in series is proposed in [16]. Another memristor would load the buffer in order to raise the output impedance of the buffer. See Fig. 6 [16].

[16] also reports that CNTFET's I-V performance is 13x better than MOSFET, and has 100x better power delay product. This forms some of the basis of CNTFETs superiority over MOSFETS. Adders, decoders and other high-level architectures that can be constructed by pure- or hybrid memristor-CMOS/CNTFET logic gates are overall better than traditional CMOS-based architectures.

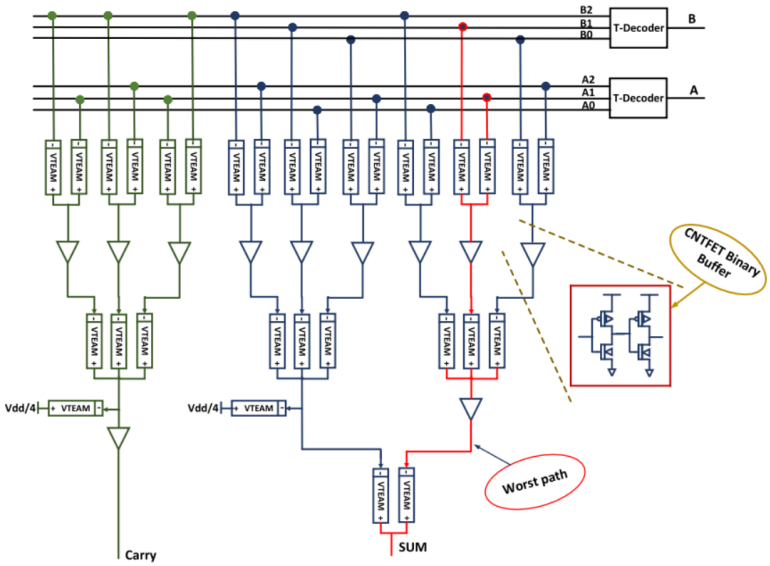


Fig. 6: Memristor- and CNTFET-based half-adder

Moreover, [20] claims that a metal-DNA-metal memristor can contruct reversible logic gates with potential of over 1 million gigabytes of data compression per square inch. It also reports of a study in which a "(...) biomolecular device based on DNA with memristor behavior (...)" and "(...) memristor was also designed using DNA. It is used to design cells with biological memory". [20] presents "NOT, Cycle, Self-Shift" gates that are reversible. See Fig. 7 [20] for their symbolic representation. The logic gates were designed with CNTFETs and the proposed DNA memristor. See Fig. 8 [20].

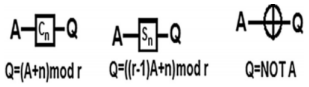


Fig. 7: Cycle, Self-Shift and NOT reversible gate

TABLE II: Truth table of reversible gates

| Input | Output | | | | | | |
|---|---|---|---|---|---|---|---|
| A | C_0 | C_1 | C_2 | S_0 | S_1 | S_2 | NOT |
| 0 | 0 | 1 | 2 | 0 | 1 | 2 | 2 |
| 1 | 1 | 2 | 0 | 2 | 0 | 1 | 1 |
| 2 | 2 | 0 | 1 | 1 | 2 | 0 | 0 |

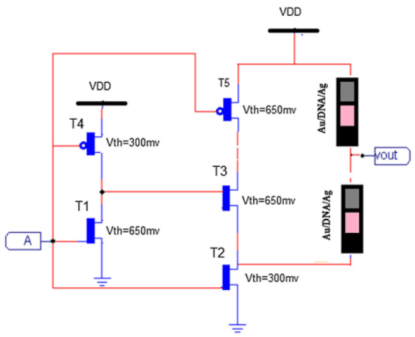


Fig. 8: Proposed circuit for gate $C_2$

## III. Discussion

From table 2 and 3 in [16], we can see that the pure CNTFET implementations for 2- and 3-input TNOR gate has better performance in terms of power consumption and delay than their hybrid counterpart consisting of memristor-CNTFET. However, table 5 shows that for the ternary decoder comparison, the hybrid implementation has comparable performance in terms of stated characteristics. We can also see in table 9 that the proposed ciruit with memristor-CNTFET implementation (proposed circuit 2) utilizes fewer components (memristors, transistors) to implement the two-bit adder, thus resulting in smaller dice space. In table 10, the proposed circuit in-question utilizing threshold approach has better performance characteristics than any of the other two circuit designs. Per [16], the circuit has "(...)15x better performance than the CNTFET-based design." This is in unity with the findings in [20]; table 2 shows that the proposed gate ($C_2$) circuit (in Fig. 8) scored better in terms of power consumption and signal latency. Moreover, the paper also raised the possibility of design of a low-power, efficient and reversible full adder utilizing new logic gate.

However, table 4 in [19] also shows that the proposed design consisting of memristor-MOSFET combination resulted in fewer transistor count compared to other exitsting designs utilizing CNTFET and CMOS. This shows that memristor-based solutions for existing circuit designs has to be mixed with known techniques to give advantage. This in turn confirms that memristor-based ternary logic gates still need time to root in new, state of the art technology that mankind can utilize in coming years. These low-level building blocks are still in their upstart and will require further implementations in novel and newfound architectures to provide solid grounds for replacing existing technology. Still, the survey of memristor-based ternary logic gates presented in section II lays a solid foundation for such technology to show its capability. The presented logic gates have the potential to revolutionize existing technology-domain. Out of the 19683 bivariate functions for radix 3, only a handful are known. Ternary numbers are inherently better in terms of informational bandwidth, since more numbers can be presented in the same amount of digits. For ternary logic gates, this means that a greater number of input permutations to bivariate functions will give a wider range of function outputs. In other words, ternary logic gates are inherently more capable than their binary equivalents. However, since mankind went forth with a binary-favored computational architecture in 1950s, a great deal of development has been done on stated computational architecture while other types of architectures with roots in other radices have somewhat been left behind.

## IV. Future work

In order to transition to pure memristor-based logic gates that nullify the loading-effect [16] without using a CNTFET-based buffer, further research and development into memristor-based buffers is required. Such a memristor-based buffer may provide better overall performance compared to traditional CMOS- or hybrid-based buffers.

The majority of two-input, one-output ternary logic gates have not been mapped. The continued experimentation, exploration, utilization and development of memristor-based ternary logic can give rise to a new branches of technology. Also, the continued mapping of ternary bivariate functions and development of new circuitry consisting of memristors has the potential to unravel new capability and performance that might not have been explored before.

DNA-based memristors and/or cells with biological memory [20] can be utilized as new platform for creating cell-based logic gates. These logic gates has the potential to expand the biotechnology arena to a great extent. Cell- and DNA-based memristors require further investigation to determine if they are viable for next-generation technology.

Since memristors are not inherently restricted to three levels, they can and probably will be utilized for development in architectures rooted in other radices than 2 and 3. This might very well be the steps for being able to implement quantum technology for normal usage in the future. We already have promising reports of memristors being utilized in a number of technological fields, such as resistive random access memory (RRAM), high-density Boolean logic and reconfigurable electronics according to [21]. [16] also claims that memristors are suitable for pattern recognition, image processing, and neuromorphic computing.

## V. Conclusion

Memristors and memristor-based ternary logic gates implemented in hybrid-component designs are showing promising results as candidate for the next paradigm shift in technological development. Results shown in [16], [19], and [20] show that memristor- and hybrid-based ternary logic gate implementations of existing systems perform better in terms of power consumption, latency, component count and occupied dice space. Memristors also show promising value and capability in a range of other scientific and technological fields, such as neuromorphic computing and memory devices.

However, pure memristor-based solutions are not explored, experimented, utilized and developed enough to fully replace existing CMOS- and hybrid-based implementations of existing systems. Much development and progress is needed before memristor-based technology can be realized for usage in novel systems. The use of memristors and hybrid-based logic gate implementations are likely to contribute to development of technology geared in higher radices such as quaternary

and quinary. There is a chance that development of systems rooted in bigger and bigger radices contribute to the overall development of quantum-based technology.

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