# Minji Shon

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## RESEARCH INTERESTS

Circuit Reliability, Analog and Mixed-signal IC design, Digital circuit design,
Wafer Level Reliability, Device modeling, Characterization, Evaluation and Analysis

6+ years of strong hands-on experience with DFR (Design For Reliability) as reliability engineer' in Quality & Reliability team, Foundry Business, Samsung Electronics

## EDUCATION

Mar. 2012 – Aug. 2016 **SOGANG UNIVERSITY** **Seoul, Republic of Korea**
*B.S., Electronic Engineering*
- **Graduated with Honors** **GPA(Major) 3.92/4.0, GPA(Total) 3.85/4.0** (1 out of 18, 130 credits)

Jan. 2015 – May. 2015 **UNIVERSITY of CONNECTICUT** **Storrs, CT, USA**
*Exchange Student, Electrical and Computer Engineering*
- **GPA (Major) 4.0/4.0**

## WORK EXPERIENCE

Aug. 2016 – Present **SAMSUNG ELECTRONICS** **Republic of Korea**
***Engineer, Technology Quality & Reliability Group***

**Implemented circuit aging environment**
- Built up aging PDK components based on accelerated Si test results up to 3nm GAA technology

**Improved the coverage and accuracy of transistor's aging models**
- Implemented aging models including HCI(Hot Carrier Injection), BTI(Bias Temperature Instability) degradation and TDDB(Time Dependent Dielectric Breakdown) ppm calculation on FinFET Technology
- Improved consistency of Model to Hardware Correlation (MHC) with ring oscillators' frequency degradation
- Provided layout-based self-heat models and simulation environments collaborating with device reliability group
- Implemented statistical aging simulation tools to support process variation based on wafer level Si test results

**Provided IP and product-level reliability verification methods**
- Guided aging-aware circuit design methods contributing to Samsung's Exynos devices from 14nm to 4nm technology
- Reviewed HCI body-effect and implemented aging models in simulation environments to support 1.8V and 3.3V GPIO by stacking Single Gate devices for 3nm GAA technology
- Collaborated with a Design Technology group to provide guidance of reliability timing margin for Application Processor devices with critical path aging simulation. Put efforts to provide realistic timing margin analyzing BTI effects
- Provided aging-aware verification methods in real operating conditions: Multi-step aging and Power-Down mode simulation methods causing HCI degradation and aging-induced Vt mismatch in ICs
- Implemented verification methods to support overdrive voltage memory IPs such as eFUSE, OTP and MRAM.

Oct. 2021 – Dec. 2021 **SAMSUNG ELECTRONICS** **Republic of Korea**
***Engineer, Dispatch, Design Enablement Team***
- Dispatched to RF device modeling group to enhance RF device reliability in both DC and AC simulation
- Extracted binning and global models for 8nm RF technology

Jul. 2016 – Aug. 2016 **SAMSUNG ELECTRONICS** **Republic of Korea**
***Intern, Technology Quality & Reliability Group***
- Proposed enhancing dynamic device voltage check methodology by analyzing bias check simulation environment

Jan. 2016 – Jun. 2016 **SOGANG UNIVERSITY** **Republic of Korea**

***Undergraduate student research, Signal Processing Systems Laboratory***

- Implemented real-time high-speed and high-resolution ultrasound image processing in equipment by using CUDA GPU language (Advisor: Taekyung Song)

## HONORS & AWARDS

- Graduated with honors; Dean's List, Sogang University
- Full National Scholarship for Academic Excellence, Korea Student Aid Foundation (KSAF), 2014~2016
- Honors Scholarship for Academic Excellence, Sogang University, 2012~2015

## PUBLICATION

- Shim, H., Jo, J., Kim, Y., Jeong, B., ***Shon, M.***, Jiang, H., & Pae, S., Aging-aware design verification methods under real product operating conditions. *In 2019 IEEE International Reliability Physics Symposium (IRPS)*, pp. 1-4, 2019

## ENGINEERING SKILLS & TOOLS

- Development of customized reliability simulation tools from Cadence and Synopsys
- Data analysis. Automation script for aging model implementation

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|---|---|
| **Circuit Netlisting** | Finesim; Hspice; Spectre |
| **Reliability Simulation Tools** | RelXpert; MOSRA; OMI; Spectre-native |
| **Tool Packages** | Cadence Virtuoso; MATLAB |
| **High level-languages** | Python; C |
| **Scripting Languages** | Perl; TCL |

## TEACHING EXPERIENCE

**SAMSUNG ELECTRONICS** **Republic of Korea**

***Education Mentor*** Jan. 2020 – Mar. 2020

- Dispatched as a mentor for SVP(Samsung Value Program) mentoring new employees
- Presented lectures of global business manners and etiquettes, also managed time schedules for education programs
- Performed the role of facilitator providing guidance in team projects to bring out members' creativity and abilities

**SAMSUNG ELECTRONICS** **Republic of Korea**

***Education Mentor*** Jan. 2022 – Mar. 2022

- Dispatched as a sub-course manager for GNEC(Global New Employee Course)
- Presented lectures of communication skills and creative thinking

## EXTRACURRICULAR ACTIVITIES

**SAMSUNG SQUASH CLUB** **Republic of Korea**

***Chief of a Club; Playing Coach*** Jan. 2017 – Present

- Held squash competitions for Samsung squash clubs and year-end parties managing club members and finance
- Provide lessons to new members
- Achieved 1st prize in amateur squash competitions held in the Republic of Korea

## LANGUAGE PROFICIENCY

- Proficient in English, Native in Korean
- IBT TOEFL : 102 (Reading: 26, Listening: 29, Speaking: 21, Writing: 26)
- New GRE : 154(Verbal Reasoning)/ 168(Quantitative Reasoning)/ 4.0(Analytical Writing)