[Statement of Purpose]

"Such a waste of time to sleep more than 4 hours a day." I can confidently say that I lived more fiercely than anyone else in the last semester of my college year. During the first half of 2016, my day started at the ultrasound system laboratory at 8 a.m. and finished the following day at 3 a.m.. Working as an engineer in Samsung, as Samsung fabrications operate 24 hours a day, sometimes I stayed up all night to acquire the proper data and solutions. This is how I survive in the “Excellence”- required competitive society.

In the semiconductor industry, “Excellence” is often defined by its Power, Performance, and Area (usually we call this “PPA"). Working as a Design For Reliability (DFR) Engineer for close to seven years, I am enabling solutions to cover from performance to reliability by providing a more stable design environment to help designers; reducing the time required for design, verification and sign-off process, while also boosting product reliability.

Unfortunately, at least from my point of view, the more we pursue PPA, which is "Excellence," I recognize that the importance of reliability and robustness is increasingly overlooked.

As an engineer in Samsung, I felt limited to invest my time and resources to research and resolve issues. Leveraging my work experience in transistor-level aging-aware design, I hope to extend my knowledge by seeking a solution to intrinsic and extrinsic failures and eventually enhance reliability and robustness of the product. I have an unquenchable thirst for this, so I'm challenging myself for a Ph.D.

Not only did I acquire knowledge about semiconductors in general, but I also experienced the latest technologies for real products while working at Samsung. I developed degradation modeling that had not been treated before: such as the off-state HCI model, the off-state TDDB model, and the HCI body bias model. To be more specific, I had issues that non-operating states caused unintended device degradation and aging-induced mismatching of the circuit. To solve them, I devised aging-aware design verification methods under real product operation conditions, such as power down mode, which can be easily missed but can cause significant failures. As a result, problems that may arise in the circuit can be predicted in advance. My team published a paper named “Aging-aware design verification methods under real product operating conditions” in the International Reliability Physics Symposium (IRPS). My contributions are to implement models and tools to allow aging-aware simulation. Through this experience, I have developed a habit of looking at things from a different point of view and examining even the parts that were taken for granted.

The strong field experience is one of my strengths. As I aforementioned, “Excellence” is defined by the transistor's PPA. Likewise, I believe it is not the best choice to make products having extremely boosted reliability. To increase performance without taking risk of failure, I developed a methodology using the short time TDDB reliability data by collaborating with the device reliability team. For instance, because efuse cells are highly biased to program data, they are not competitive with traditional analysis methods. I was able to increase their lifetime in a new way and meet the needs of customers by realizing an excessive margin. Such experience made me improve skills to identify needs and derive realistic plans no matter what kind of research I do.

As nano-scale technology becomes more complicated, the challenges for modeling, methods, and tools are increasing. I would like to do research on more accurate and faster design methodologies not only in terms of reliability but also in the design performance. Recently, I am focusing on ways to improve accuracy of aging models and simulation methodologies to predict failure mode in the design phase. To overcome a lot of approximations for acceleration test and aging simulation, I had a project to

improve Model to Hardware Correlation (MHC) by developing mobility aging simulation methods. I am planning to study the impact of this methodology compared to traditional methods.

I believe my work experience has broadened my perspective in the field. I have learned the importance of finding a balance between performance and reliability. Not only limited to reliability, I am also interested in VLSI design and device technologies collaborating with data analysis and machine learning. Therefore, I want to do research that can fill the gap by grafting experience on reliability from circuit design to device characteristics. Eventually, I want to enable a solution where simulation-based analysis provides data to discuss both aspects (performance and reliability) without having to wait for tedious tests.

I have various research ideas that I want to study in your school, because a wide variety of factors from transistors to circuits make circuit reliability an extremely complex topic. Beyond using the existing modeling method, if the aging effect can be observed through in-situ testing, not only intrinsic but also extrinsic modeling can be considered. Not only analog blocks, I think aging-aware STA, based on machine learning modeling, can be a way to verify digital blocks. Moreover, as a product's applications are getting complexed depending on different users, I want to do research on how to increase the speed of verifying all the scenarios.

Semiconductors are essential in society from smartphones to robots for disabled people, autonomous cars and artificial intelligence medical care. It was shocking that all of our lives are contained in nanometer-scale semiconductor devices, so I was eagerly looking forward to participating in this kind of life. I thought I was an introvert and afraid of change, but by participating in study groups at University of Connecticut, I found that I could enjoy new environments and like to get along with different people. Therefore, I am confident that I can do better with many renowned professors in your school by collaborating with industry. After finishing graduate programs and receiving Ph.D, I would like to go back to industry and contribute myself to overcome challenges.

Thank you for your time and consideration of this letter.