People First; Pursuing Excellence; Leading Change; Upholding Integrity; Ensuring Co-prosperity. These are the five values of Samsung, a pioneering company in semiconductors, which are engraved in every employees' mind, including myself.

In the semiconductor industry the "Excellence" is often defined by its power, performance, and area (PPA). Working as a Design For Reliability (DFR) Engineer in Quality & Reliability team, I enabled solutions to cover from performance to reliability by providing a more stable design environment to help designers; reducing the time required for design, verification and sign-off process, while also boosting product reliability. When Samsung began chip production using 3 nm Process Technology, I recognized that the importance of reliability and robustness are getting overlooked as we are pursuing PPA. However, as an engineer in Samsung, I felt limited to invest my time and resources to research and resolve issues. Leveraging my work experience in transistor-level aging-aware design, I am admiring to extend my knowledge by seeking a solution to intrinsic and extrinsic failures and eventually enhance reliability and robustness of the product.

I not only acquired knowledge about semiconductors in general, but also experienced the latest technologies for actual products while working for Samsung. I developed degradation modeling that had not been treated before, such as the off-state HCI model, the off-state TDDB model, and the HCI body bias model. To be more specific, I had issues that non-operating states caused unintended device degradation and aging-induced mismatching of the circuit. I devised aging-aware design verification methods under real product operation conditions such as power down mode which can be easily missed but can cause significant failures. These lead to the results that the number of possible issues in the circuit could be predicted in advance. As a result of these works, my team published a paper named "Aging-aware design verification methods under real product operating conditions" in International Reliability Physics Symposium (IRPS). My contributions are to implement models and tools to allow aging-aware simulation. Through this experience, I have developed a habit of looking at things from a different point of view and examining even the parts that were taken for granted.

The strong field experience is one of my strengths. As I aforementioned, "Excellence" is often defined by the transistor's PPA. Likewise, I believe it is not the best choice to make products having extremely boosted reliability. To increase performance without taking risk of failure, I developed a methodology using the short time TDDB reliability data by collaborating with the device reliability team. For instance, because efuse cells are highly biased to program data, they are not competitive with traditional analysis methods. I was able to increase their lifetime in a new way and meet the needs of customers by realizing an excessive margin. Such experience made me improve skills to identify needs and derive realistic plans no matter what kind of research I do.

As nano-scale technology becomes more complicated, the challenges for modeling, methods, and tools are increasing. I would like to do research on more accurate and faster design methodologies not only in terms of reliability but also in the design performance. Recently, I am focusing on ways to improve aging models accuracy and simulation methodologies to predict failure mode in advance. To overcome a lot of approximations for acceleration test and aging simulation, I had a project to improve Model to Hardware Correlation (MHC) by developing mobility aging simulation methods. I am planning to study the impact of this methodology compared to traditional methods and preparing for a paper.

I have learned the importance of finding a balance between performance and reliability. A wide variety of factors, from transistors to circuits, make circuit reliability an extremely complex topic. I believe my work experience has broadened my perspective in the field. Not only limited to reliability, I am also interested in VLSI design and device technologies collaborating with data analysis and machine learning. Therefore, I want to do research that can fill the gap by grafting experience on reliability to circuit design and device characteristics. Eventually, I want to enable a solution where simulation-based analysis provides data to discuss both aspects without having to wait for tedious tests. Beyond using the existing modeling method, if the aging effect can be observed through in-situ testing, not only intrinsic but also extrinsic modeling can be considered. Not only analog blocks, I think aging-aware STA based on machine learning modeling can be a way to verify digital blocks. Moreover, as a product's applications are getting complexed depending on different users, I want to do research on how to increase the speed of verifying all the scenarios.

I am eagerly awaiting to study with Professor Chris Kim because his research involving on-chip monitoring circuits inspired me to research more on the field through different approaches. Moreover, I am also looking forward to the opportunity to work with Professor Keshab K. Parhi who is expanding his research to reliability-aware VLSI signal processing because I think they can lead to correspondence with my experience. Lastly, I was also impressed by Professor Sachin who has done research on design automation. (UMN example)

I believe that OOO University is the perfect place that I can contribute to school and also to the semiconductor industry by harmonizing your research programs and proper guidance from professors with my strong working experience. Semiconductors are essential in society from smartphones to robots for disabled people, autonomous cars and artificial intelligence medical care. It was shocking that all of our lives are contained in nanometer-scale semiconductor devices, so I was eagerly looking forward to participating in this kind of life. I thought I was an introvert and afraid of change, but by participating in study groups at UCONN, I found that I could enjoy new environments and like to get along with different people. Therefore, I am confident that I can do better with many renowned professors in your school by collaborating with industry. After finishing graduate programs and receiving Ph.D, I would like to go back to industry and contribute myself to overcome challenges.

Thank you for your time and consideration of this letter.