Minjing Lee

+086-21-15921901226 | minjing.lee@sjtu.edu.cn | Personal Website

Research Interest

My research interest is in Analog and RF integrated circuits design. Currently, I am interested in tunable RF front-end circuits exploiting N-path techniques. I hope to contribute to efficient and green integrated circuits and communication systems to improve the quality of life and help protect the beautiful Earth I love.

Education

Shanghai Jiao Tong University Shanghai, China

B.Eng in Microelectronics Science and Engineering, minor in Philosophy *Sep 2019 - June 2023(Expected)*

- **GPA: 90.25/100, 3.87/4.3** (Ranked 4 out of 67 students)

Research Experience

RF Front-End Circuits Exploiting N-Path Transformers July 2022 – Present

Center for Analog/RF Integrated Circuits(CARFIC), Shanghai Jiao Tong University *Shanghai, China*

- **Advisor:** Prof Xiaoming Liu and Prof Jing Jin
- **Paper under submission:** "Name omitted to maintain anonymity", **Minjing Lee**, Xiaoming Liu, Zhaolin Yang, Jing Jin. *[International Symposium on Circuits and Systems (ISCAS) 2023]*
  A compact passive LNA with an N-path 1:3 transformer is proposed to replace the bulky step-up spiral transformer, thus consuming less chip area than prior arts.
- **A reconfigurable prototype using an N-path 1:9 transformer is taped out in 55-nm CMOS.**

Low Power Successive Approximation Register Analog-to-Digital Converter Mar 2021 – Aug 2021

Center for Analog/RF Integrated Circuits(CARFIC), Shanghai Jiao Tong University *Shanghai, China*

- **Advisor:** Prof Jing Jin
- Researched calibration techniques for SAR ADC and dynamic amplifier design for pipelined SAR ADC.

Projects

A Spice Circuit Simulator | *MR325 Introduction to Design Automation* Sep 2022 – Nov 2022

- Realized a circuit simulator in C++, capable of performing DC, AC and Tran simulations on linear elements and basic non-linear devices.

A VCO-Based ADC | *MR413 Course Design for Analog Integrated Circuits* Sep 2022 – Nov 2022

A Wideband Blocker-Tolerant Receiver | *Center for Analog/RF Integrated Circuits* Mar 2022 – Aug 2022

- Implemented a 0.5-2GHz 4-path Mixer-First receiver with a 2nd order baseband TIA in 65-nm CMOS.
- Completed systematic tape-out flow including schematic design, simulation, layout, and post-layout verification.
- Won **1st Prize** in National Final at the 6th China College IC Competition(IEEE Cup).

Awards & Honors

Baosteel Excellence Scholarship, Baosteel Education Foundation 2022

National First Prize, The 6th China College IC Competition(IEEE Cup) 2022

Undergraduate Excellence Scholarship, Shanghai Jiao Tong University 2021

Taiwanese Student Scholarship, Shanghai Jiao Tong University 2019, 2020, 2021

Community & Leadership

Outdoor Association, SJTU Dec 2021 – Sep 2021

President

Philosophy Club, SJTU 2021

Co-Founder

Technical Skills

Languages: Mandarin(Native), English
Programming: C++, C, Verilog, Spice
EDA Tools: Cadence Virtuoso, Cadence ADE