Submission 11

10.1.1

```
SUBS (immediate)
1111 0001 00ii iiii iiii iinn nnnd dddd
```

10.1.2

```
SUBS will set the Nzcv- bits, SUB wont
Instruction encoding of SUB (immediate) (Diff von SUBS)
29th bit:
    SUBS sets it to '1'
    SUB sets it to '0'
```

10.1.3

```
Tabelle 10.1.2
```

```
                  Machine Code (bin)                          | Machine Code (hex)
orr x0, xzr, #3   1011 0010 0100 0000 0000 0111 1110 0000     | b24007e0
(given)
and x1, x1, xzr   1000 1010 0001 1111 0000 0000 0010 0001     | 8a1f0021
(given)
and x2, x2, xzr   1000 1010 0001 1111 0000 0000 0100 0010     | 8a1f0042
subs x0, x0, #1   1111 0001 0000 0000 0000 0100 0000 0000     | f1000400
add x1, x1, #3    1001 0001 0000 0000 0000 1100 0010 0001     | 91000c21
(given)
add x2, x2, #7    1001 0001 0000 0000 0001 1100 0100 0010     | 91001c42
b.ne my_loop      0101 0100 1111 1111 1111 1111 1010 0001     | 54ffffa1
add x0, x1, x2    1000 1011 0000 0010 0000 0000 0010 0000     | 8b020020
ret               1101 0110 0101 1111 0000 0011 1100 0000     | d65f03c0
(given)
```

10.1.4

```
machine_code_asm_1:
.inst 0xb24007e0        //orr   x0, xzr, #0x3
.inst 0x8a1f0021        //and   x1, x1, xzr
.inst 0x8a1f0042        //and x2, x2, xzr
//my_loop
```

```
.inst 0xf1000400        //subs  x0, x0, #0x1
.inst 0x91000c21        //add   x1, x1, #0x3
.inst 0x91001c42        // add  x2, x2, #0x7
.inst 0x54ffffa1        //b.ne  c <my_loop>  // b.any
.inst 0x8b020020        //add   x0, x1, x2
.inst 0xd65f03c0        //ret
```

10.2.1

```
x0: -, x1: -, x2: -,  x3: -
x0: 7, x1: -, x2: -,  x3: -
x0: 7, x1: 0, x2: -,  x3: -
x0: 7, x1: 0, x2: 10, x3: -
x0: 7, x1: 0, x2: 10, x3: 4
x0: 6, x1: 0, x2: 10, x3: 4
```

10.2.2

```
In order, control signals for: RegSrc RegW ImmType AluSrc AluCtrl MemW Mem2Reg
```

```
orr x0, xzr, #7
x 1 2 1 3 0 0   ORR (immediate)
```

```
and x1, x1, xzr
x 1 2 1 2 0 0   AND (immediate)
```

```
add x2, x0, #3
x 1 1 1 0 0 0   ADD (immediate)
```

```
add x3, x1, #4
x 1 1 1 0 0 0   ADD (immediate)
```

```
sub x0, x2, x3
1 1 1 0 1 0 0   SUB (shifted Register)
```