# 3 Sample Circuits

The following sample circuits show the required external components in different operation and supply modes. The connection of the bus interface and further digital signals are left out for clarity.

## 3.1 Standard Application Circuit

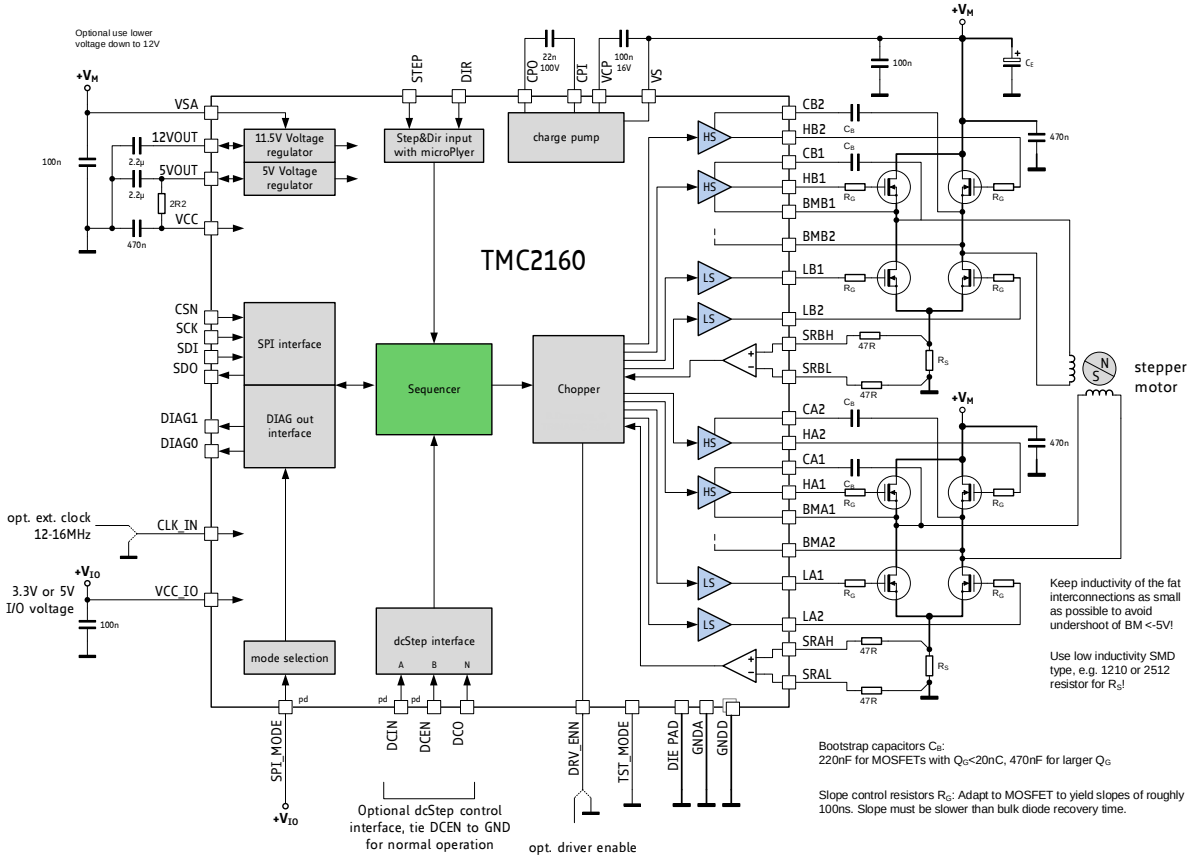



**Figure 3.1 Standard application circuit**

The standard application circuit uses a minimum set of additional components. Eight MOSFETs are selected for the desired current, voltage and package type. Two sense resistors set the motor coil current. See chapter 8 to choose the right value for sense resistors. Use low ESR capacitors for filtering the power supply. A minimum capacity of 100µF per ampere of coil current near to the power bridge is recommended for best performance. The capacitors need to cope with the current ripple caused by chopper operation. Current ripple in the supply capacitors also depends on the power supply internal resistance and cable length. VCC_IO can be supplied from 5VOUT, or from an external source, e.g. a 3.3V regulator. In order to minimize linear voltage regulator power dissipation of the internal 5V and 11.5V voltage regulators in applications where VM is high, a different (lower) supply voltage should be used for VSA (see chapter 3.2).

*Basic layout hints*
Place sense resistors and all filter capacitors as close as possible to the power MOSFETs. Place the TMC2160 near to the MOSFETs and use short interconnection lines in order to minimize parasitic trace inductance. Use a solid common GND for all GND, GNDA and GNDD connections, also for sense resistor GND. Connect 5VOUT filtering capacitor directly to 5VOUT and GNDA pin. See layout hints for more details. Low ESR electrolytic capacitors are recommended for VS filtering.

*Attention*
In case VSA is supplied by a different voltage source, make sure that VSA does not drop out during motor operation. Stop and disable the motor before VSA power down. This is not necessary, when VSA voltage is derived from VS supply, as both supplies go down in parallel in this case.

## 3.2 External Gate Voltage Regulator

At high supply voltages like 48V, the internal gate voltage regulator and the internal 5V regulator have considerable power dissipation, especially with high MOSFET gate charges, high chopper frequency or high system clock frequency >12MHz. A good thermal coupling of the heat slug to the system PCB GND plane is required to dissipate heat. Still, the thermal thresholds will be lowered significantly by self-heating. To reduce power dissipation, supply an external gate driver voltage to the TMC2160. Figure 3.2 shows the required connection. The internal gate voltage regulator becomes disabled in this constellation. 12V +/-1V are recommended for best results.

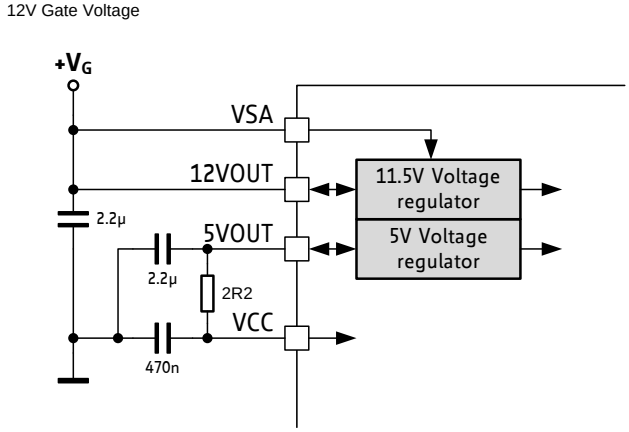



**Figure 3.2 External gate voltage supply**

*Hint*
With MOSFETs above 50nC of total gate charge, chopper frequency >40kHz, or at clock frequency >12MHz, it is recommended to use a VSA supply not higher than 40V.

# 3.3 Choosing MOSFETs and Slope

The selection of power MOSFETs depends on a number of factors, like package size, on-resistance, voltage rating and supplier. It is not true, that larger, lower RDSon MOSFETs will always be better, as a larger device also has higher capacitances and may add more ringing in trace inductance and power dissipation in the gate drive circuitry. Adapt the MOSFETs to the required motor voltage (adding 5-10V of reserve to the peak supply voltage) and to the desired maximum current, in a way that resistive power dissipation still is low for the thermal capabilities of the chosen MOSFET package. The TMC2160 drives the MOSFET gates with roughly 10V, so normal, 10V specified types are sufficient. Logic level FETs (4.5V specified RDSon) will also work, but may be more critical with regard to bridge cross-conduction due to lower $V_{GS(th)}$.

The gate drive current and MOSFET gate resistors $R_G$ (optional) determine switching behavior and should basically be adapted to the MOSFET gate-drain charge (Miller charge). Figure 3.3 shows the influence of the Miller charge on the switching event. Figure 3.4 additionally shows the switching events in different load situations (load pulling the output up or down), and the required bridge brake-before-make time.
The following table shall serve as a thumb rule for programming the MOSFET driver current (*DRVSTRENGTH* setting) and the selection of gate resistors:

| **MOSFET MILLER CHARGE VS. *DRVSTRENGTH* AND $R_G$** | | |
|---|---|---|
| **Miller Charge [nC] (typ.)** | *DRVSTRENGTH* setting | **Value of $R_G$ [Ω]** |
| <10 | 0 | ≤ 15 |
| 10…20 | 0 or 1 | ≤ 10 |
| 20…40 | 1 or 2 | ≤ 7.5 |
| 40…60 | 2 or 3 | ≤ 5 |
| >60 | 3 | ≤ 2.7 |

The TMC2160 provides increased gate-off drive current to avoid bridge cross-conduction induced by high dV/dt. This protection will be less efficient with gate resistors exceeding the values given in the table. Therefore, for larger values of $R_G$, a parallel diode may be required to ensure keeping the MOSFET safely off during switching events.

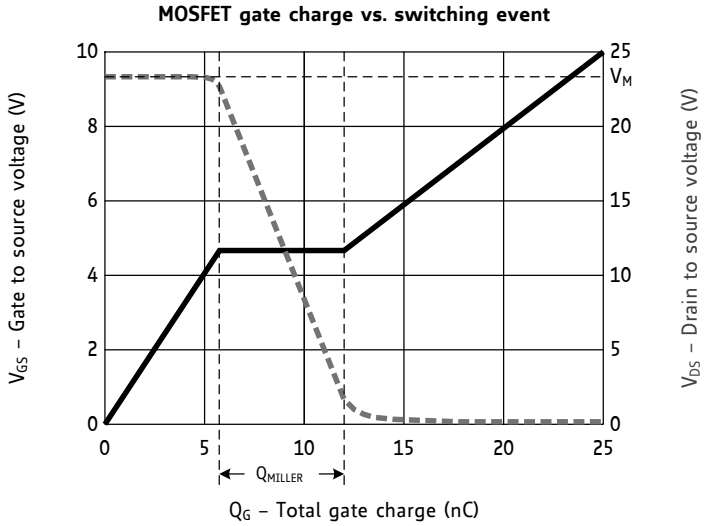



**Figure 3.3 Miller charge determines switching slope**

*Hints*
- Choose modern MOSFETs with fast and soft recovery bulk diode and low reverse recovery charge.
- A small, SMD MOSFET package allows compacter routing and reduces parasitic inductance effects.

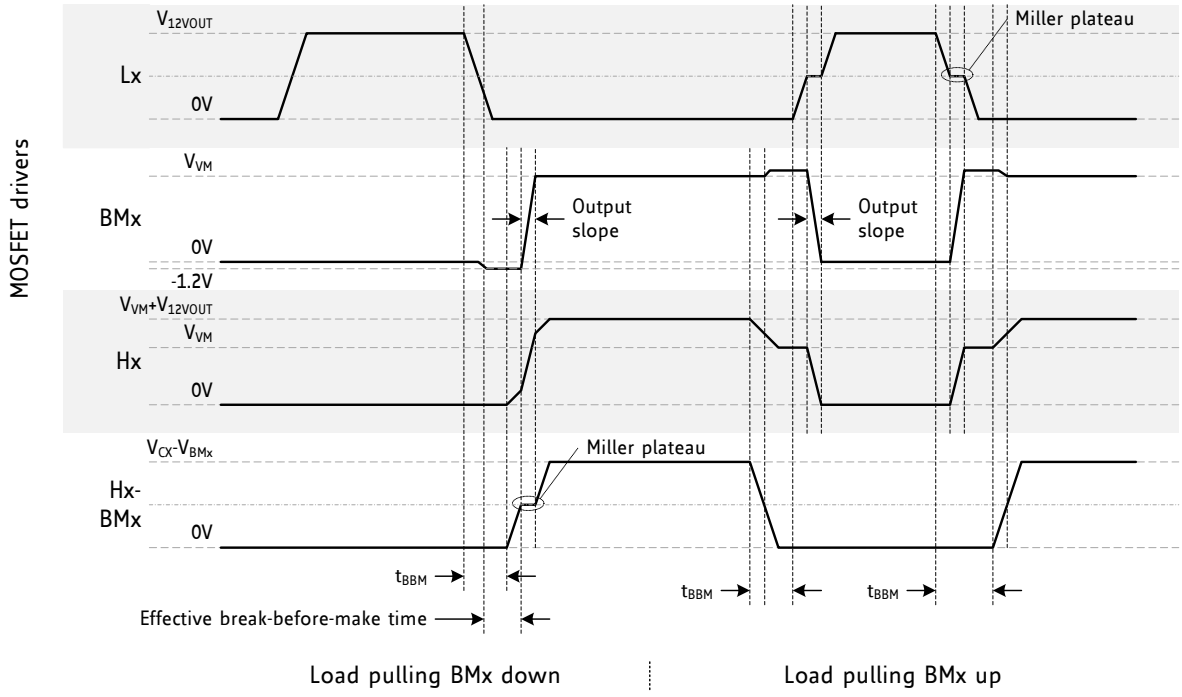



**Figure 3.4 Slopes, Miller plateau and blank time**

The following *DRV_CONF* parameters allow adapting the driver to the MOSFET bridge:

| Parameter | Description | Setting | Comment |
|---|---|---|---|
| *BBMTIME* | Break-before-make time setting to ensure non-overlapping switching of high-side and low-side MOSFETs. *BBMTIME* allows fine tuning of times in increments shorter than a clock period.<br>For higher times, use BBMCLKS. | 0…24 | time[ns]≈ 100ns*32/(32-*BBMTIME*)<br><br>*Ensure ~30% headroom*<br>*Reset Default: 0* |
| *BBMCLKS* | Like *BBMTIME*, but in multiple of a clock cycle.<br>The longer setting rules (*BBMTIME* vs. *BBMCLKS*). | 0…15 | 0: off<br>*Reset Default: OTP 4 or 2* |
| *DRV_ STRENGTH* | Selection of gate driver current. Adapts the gate driver current to the gate charge of the external MOSFETs. | 0…3 | *Reset Default = 2* |
| *FILT_ISENSE* | Filter time constant of sense amplifier to suppress ringing and coupling from second coil operation<br>*Hint:* Increase setting if motor chopper noise occurs due to cross-coupling of both coils.<br>*(Reset Default = %00)* | 0…3 | 00: ~100ns (*reset default*)<br>01: ~200ns<br>10: ~300ns<br>11: ~400ns |

*DRV_CONF Parameters*
Use the lowest gate driver strength setting *DRVSTRENGTH* giving favorable switching slopes, before increasing the value of the gate series resistors. A slope time of nominal 40ns to 80ns is absolutely sufficient and will normally be covered by the shortest possible Break-Before-Make time setting (*BBMTIME*=0, *BBMCLKS*=0).
In case slower slopes have to be used, e.g. with large MOSFETs, ensure that the break-before-make time (*BBMTIME*, optionally use *BBMCLKS* for times >200ns) sufficiently covers the switching event, in order to avoid bridge cross conduction. The shortest break-before-make time, safely covering the switching event, gives best results. Add roughly 30% of reserve, to cover production stray of MOSFETs and driver.

## 3.4 Tuning the MOSFET Bridge

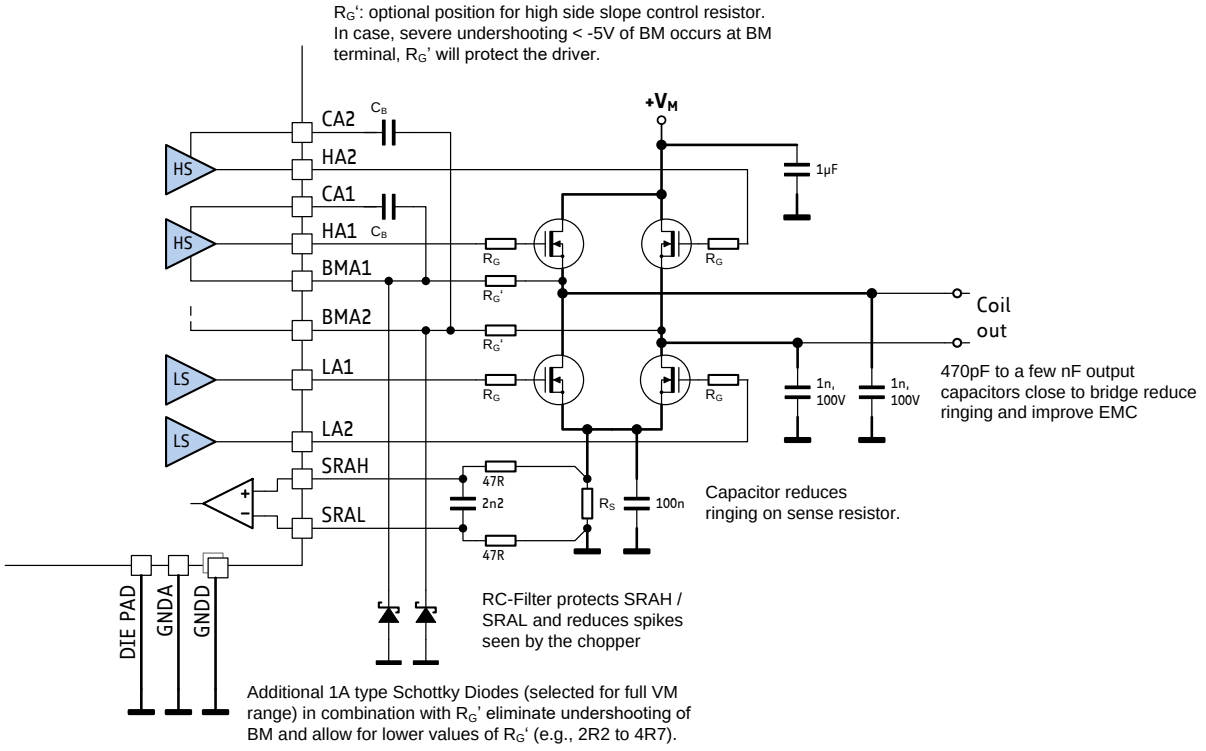
A clean switching event is favorable to ensure low power dissipation and good EMC behavior. Unsuitable layout or components endanger stable operation of the circuit. Therefore, it is important to understand the effect of parasitic trace inductivity and MOSFET reverse recovery.

Stray inductance in power routing will cause ringing whenever the opposite MOSFET is in diode conduction prior to switching on a low-side MOSFET or high-side MOSFET. Diode conduction occurs during break-before make time when the load current is inverse to the prior bridge polarity, i.e. following a fast decay cycle. The MOSFET bulk diode has a certain, type specific reverse recovery time and charge. This time typically is in the range of a few 10ns. During reverse recovery time, the bulk diode will cause high current flow across the bridge. This current is taken from the power supply filter capacitors (see thick lines Figure 3.5). Once the diode opens parasitic inductance tries to keep the current flowing. A high, fast slope results and leads to ringing in all parasitic inductivities (see Figure 3.6). This may lead to bridge voltage undershooting the GND level. It must be ensured, that the driver IC does not see spikes on its BM pins to GND going below -5V. Measure the voltage directly at the driver pins to driver GND. The amount of undershooting depends on energy stored in parasitic inductivities from low side drain to low side source and via the sense resistor RS to GND.

To improve behavior

- Tune MOSFET switching slopes (measure without inductive load) to be slower than the MOSFET bulk diode reverse recovery time. This will reduce cross conduction.
- Add optional resistors and capacitors to ensure clean switching by minimizing ringing and reliable operation. Figure 3.5 shows different options.
- Some MOSFETs eliminate this problem by integrating a Schottky diode from source to drain.

Figure 3.7 shows performance of the basic circuit after adapting switching slope and adding 1nF bridge output capacitors.




*Decide use and value of the additional components based on measurements of the actual circuit using the final layout!*

**Figure 3.5 Bridge protection options for power routing inductivity**

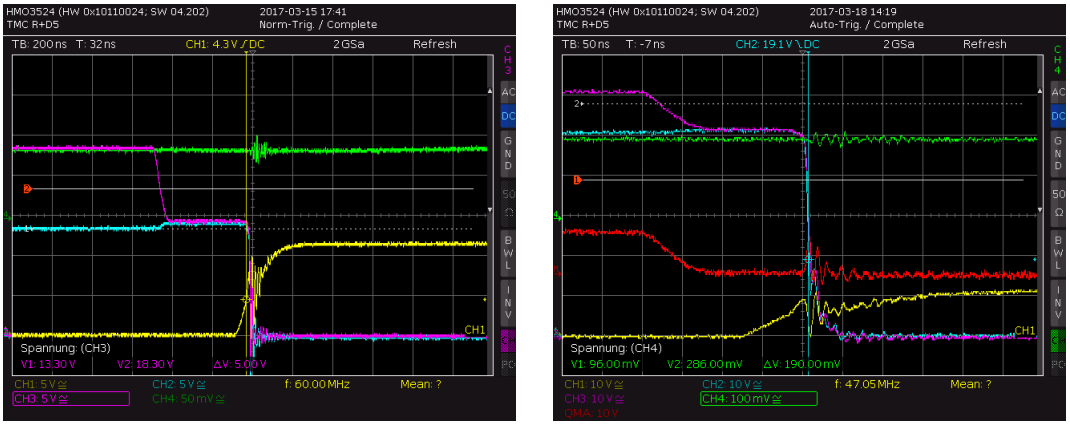



**Figure 3.6 Ringing of output (blue) and Gate voltages (Yellow, Cyan) with untuned brige**

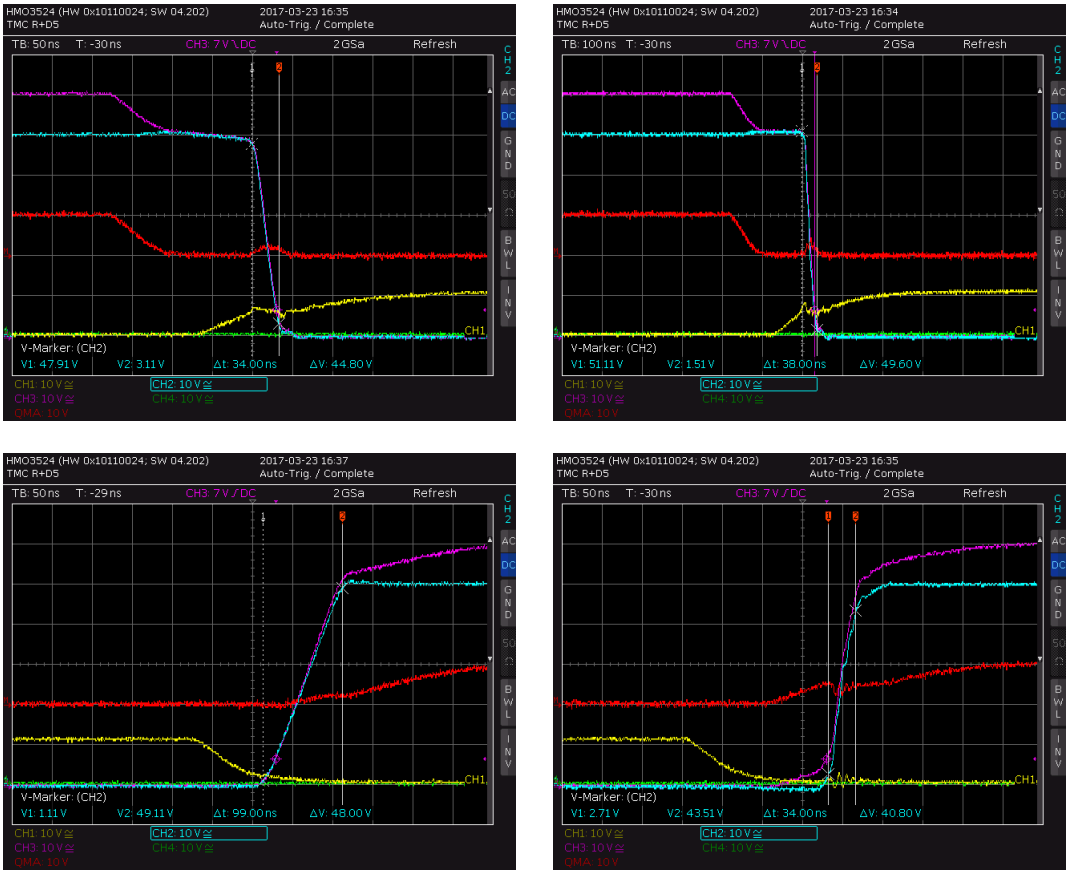



**Figure 3.7 Switching event with optimized components (without / after bulk diode conduction)**

### BRIDGE OPTIMIZATION EXAMPLE

A stepper driver for 6A of motor current has been designed using the MOSFET AOD4126 in the standard schematic.
The MOSFETs have a low gate capacitance and offer roughly 50ns slope time at the lowest driver strength setting. At lowest driver strength setting, switching quality is best (Figure 3.6), but still shows a lot of ringing. Low side gate resistors have been added to slightly increase switching slope time following high-side bulk diode conduction by increasing the effect of Gate-Drain (Miller) charge. High side gate resistors have been added for symmetry. Tests showed, that 1nF output capacitors dramatically reduce ringing of the power bridge following bulk diode conduction (Figure 3.7). Figure 3.8 shows the actual components and values after optimization.

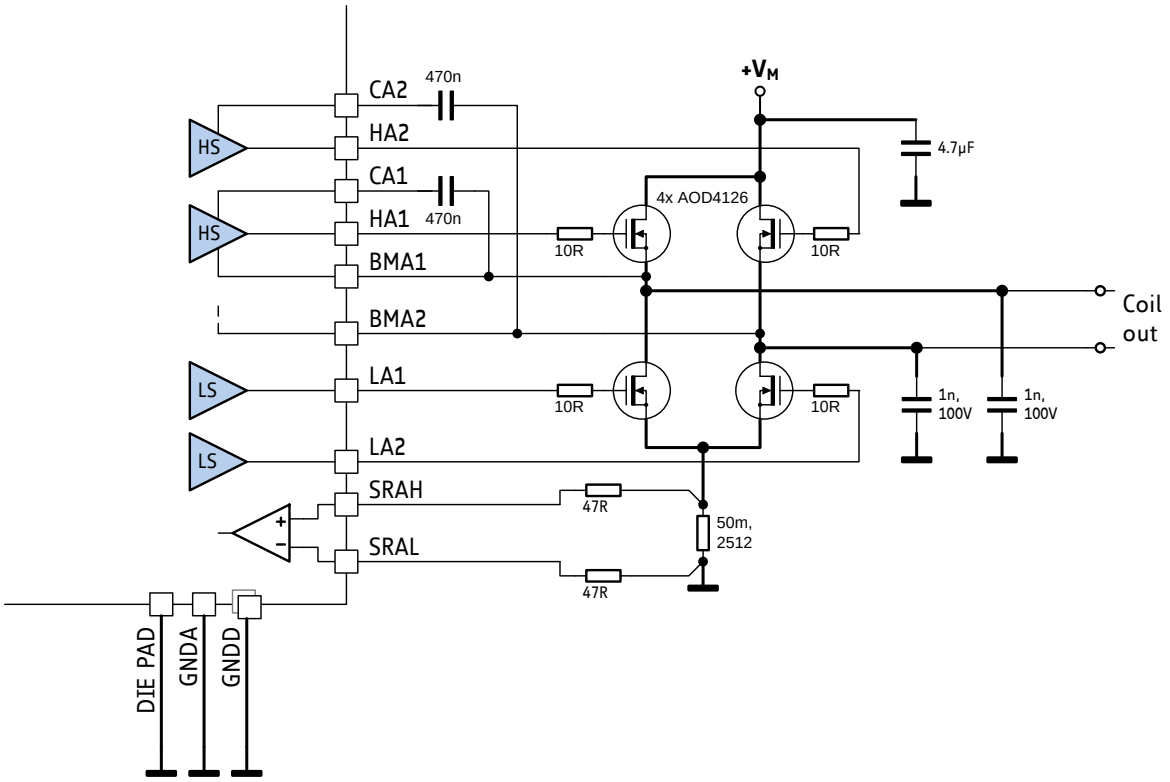



**Figure 3.8 Example for bridge with tuned components (see scope shots)**

*Hints*

- Tune the bridge layout for minimum loop inductivity. A compact layout is best.
- Keep MOSFET gate connections short and straight and avoid loop inductivity between BM and corresponding HS driver pin. Loop inductance is minimized with parallel traces, or adjacent traces on adjacent layers. A wider trace reduces inductivity (don't use minimum trace width).
- Minimize the length of the sense resistor to low side MOSFET source, and place the TMC2160 near the sense resistor's GND connection, with its GND connections directly connected to the same GND plane.
- Optimize switching behavior by tuning gate current setting and gate resistors. Add MOSFET bridge output capacitors (470pF to a few nF) to reduce ringing.
- Measure the performance of the bridge by probing BM pins directly at the bridge or at the TMC2160 using a short GND tip on the scope probe rather than a GND cable, if available.