2 Pin Assignments

2.1 Package Outline

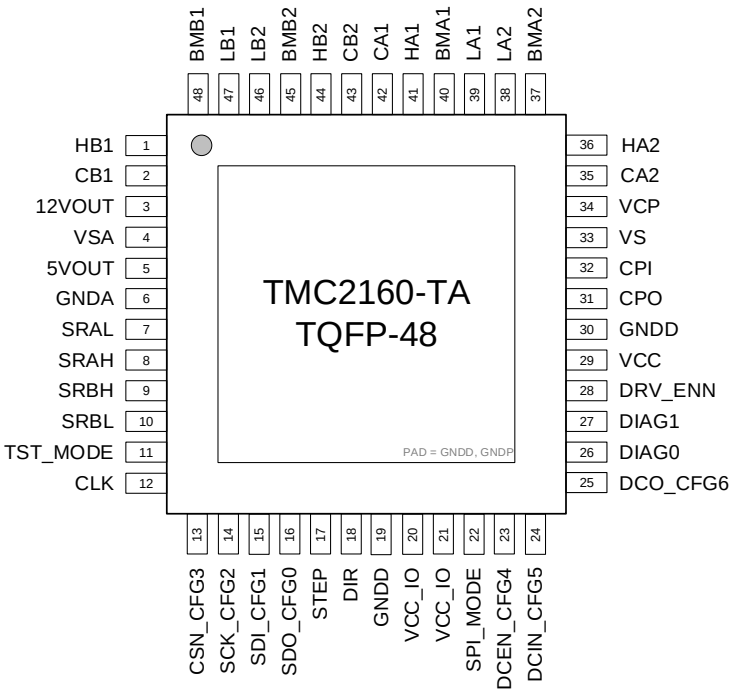

Figure 2.1 TMC2160-TA package and pinning TQFP-EP 48 (7x7mm² body, 9x9mm² with leads)

2.2 Signal Descriptions

Pin	TQFP	Type	Function
HB1	1		High side gate driver output.
CB1	2		Bootstrap capacitor positive connection.
12VOUT	3		Output of internal 11.5V gate voltage regulator and supply pin of low side gate drivers. Attach 2.2µF to 10µF ceramic capacitor to GND plane near to pin for best performance. Use at least 10 times more capacity than for bootstrap capacitors. In case an external gate voltage supply is available, tie VSA and 12VOUT to the external supply.
VSA	4		Analog supply voltage for 11.5V and 5V regulator. Normally tied to VS. Provide a 100nF filtering capacitor.
5VOUT	5		Output of internal 5V regulator. Attach 2.2µF to 10µF ceramic capacitor to GNDA near to pin for best performance. Output for VCC supply of the chip.
GNDA	6		Analog GND. Connect to GND plane near pin.
SRAL	7	AI	Sense resistor GND connection for phase A. Connect to the GND side of the sense resistor in order to compensate for voltage drop on the GND interconnection.

Pin	TQFP	Type	Function
SRAH	8	AI	Sense resistor for phase A. Connect to the upper side of the sense resistor. A Kelvin connection is preferred with high motor currents. Symmetrical RC-Filtering may be added for SRAL and SRAH to eliminate high frequency switching spikes from other drives or switching of coil B.
SRBH	9	AI	Sense resistor for phase B. Connect to the upper side of the sense resistor. A Kelvin connection is preferred with high motor currents. Symmetrical RC-Filtering may be added for SRBL and SRBH to eliminate high frequency switching spikes from other drives or switching of coil A.
SRBL	10	AI	Sense resistor GND connection for phase B. Connect to the GND side of the sense resistor in order to compensate for voltage drop on the GND interconnection.
TST_MODE	11	DI	Test mode input. Tie to GND using short wire.
CLK	12	DI	CLK input. Tie to GND using short wire for internal clock or supply external clock. Internal clock-fail over circuit protects against loss of external clock signal.
CSN_CFG3	13	DI	SPI chip select input (negative active) (SPI_MODE=1) or Configuration input (SPI_MODE=0)
SCK_CFG2	14	DI	SPI serial clock input (SPI_MODE=1) or Configuration input (SPI_MODE=0)
SDI_CFG1	15	DI	SPI data input (SPI_MODE=1) or Configuration input (SPI_MODE=0) or Next address input (NAI) for single wire interface.
SDO_CFG0	16	DIO	SPI data output (tristate) (SPI_MODE=1) or Configuration input (SPI_MODE=0) or Next address output (NAO) for single wire interface.
STEP	17	DI	STEP input
DIR	18	DI	DIR input
GNDD	19, 30		Digital GND. Connect to GND plane near pin.
VCC_IO	20, 21		3.3V to 5V IO supply voltage for all digital pins.
SPI_MODE	22	DI (pd)	Mode selection input. When tied low with SD_MODE=1, the chip is in standalone mode and pins have their CFG functions. When tied high, the SPI interface is enabled. Integrated pull down resistor.
DCEN_ CFG4	23	DI (pd)	dcStep enable input (SD_MODE=1, SPI_MODE=1) – leave open or tie to GND for normal operation in this mode (no dcStep). Configuration input (SPI_MODE=0)
DCIN_ CFG5	24	DI (pd)	dcStep gating input for axis synchronization (SD_MODE=1, SPI_MODE=1) or Configuration input (SPI_MODE=0)
DCO_ CFG6	25	DIO	dcStep ready output (SD_MODE=1). With SD_MODE=0, pull to GND or VCC_IO
DIAG0	26	DO (pu+ pd)	Diagnostics output DIAG0. Interrupt output Use external pullup resistor with 47k or less in open drain mode.
DIAG1	27	DO (pd)	Diagnostics output DIAG1. Use external pullup resistor with 47k or less in open drain mode.
DRV_ENN	28	DI	Enable input. The power stage becomes switched off (all motor outputs floating) when this pin becomes driven to a high level.

Pin	TQFP	Type	Function
VCC	29		5V supply input for digital circuitry within chip. Provide 100nF or bigger capacitor to GND (GND plane) near pin. Shall be supplied by 5VOUT. A 2.2 or 3.3 Ohm resistor is recommended for decoupling noise from 5VOUT. When using an external supply, make sure, that VCC comes up before or in parallel to 5VOUT or VCC_IO, whichever comes up later!
CPO	31		Charge pump capacitor output.
CPI	32		Charge pump capacitor input. Tie to CPO using 22nF, 100V capacitor.
VS	33		Motor supply voltage. Provide filtering capacity near pin with short loop to GND plane. Must be tied to the positive bridge supply voltage.
VCP	34		Charge pump voltage. Tie to VS using 100nF capacitor.
CA2	35		Bootstrap capacitor positive connection.
HA2	36		High side gate driver output.
BMA2	37		Bridge Center and bootstrap capacitor negative connection.
LA2	38		Low side gate driver output.
LA1	39		Low side gate driver output.
BMA1	40		Bridge Center and bootstrap capacitor negative connection.
HA1	41		High side gate driver output.
CA1	42		Bootstrap capacitor positive connection.
CB2	43		Bootstrap capacitor positive connection.
HB2	44		High side gate driver output.
BMB2	45		Bridge Center and bootstrap capacitor negative connection.
LB2	46		Low side gate driver output.
LB1	47		Low side gate driver output.
BMB1	48		Bridge Center and bootstrap capacitor negative connection.
Exposed die pad	-		Connect the exposed die pad to a GND plane. Provide as many as possible vias for heat transfer to GND plane. Serves as GND pin for the low side gate drivers. Ensure low loop inductivity to sense resistor GND.

*(pd) denominates a pin with pulldown resistor
* All digital pins DI, DIO and DO use VCC_IO level and contain protection diodes to GND and VCC_IO
* All digital inputs DI and DIO have internal Schmitt-Triggers