21 External Reset

The chip is loaded with default values during power on via its internal power-on reset. In order to reset the chip to power on defaults, any of the supply voltages monitored by internal reset circuitry (VSA, +5VOUT or VCC_IO) must be cycled. VCC is not monitored. Therefore, VCC must not be switched off during operation of the chip. As +5VOUT is the output of the internal voltage regulator, it cannot be cycled via an external source except by cycling VSA. It is easiest and safest to cycle VCC_IO in order to completely reset the chip. Also, current consumed from VCC_IO is low and therefore it has simple driving requirements. Due to the input protection diodes not allowing the digital inputs to rise above VCC_IO level, all inputs must be driven low during this reset operation. When this is not possible, an input protection resistor may be used to limit current flowing into the related inputs.

In case, VCC becomes supplied by an external source, make sure that VCC is at a stable value above the lower operation limit once the reset ends. This normally is satisfied when generating a 3.3V VCC_IO from the +5V supply supplying the VCC pin, because it will then come up with a certain delay.

22 Clock Oscillator and Input

The clock is the timing reference for all functions: the chopper, dcStep, blank time, etc. Many parameters are scaled with the clock frequency; thus, a precise reference allows a more deterministic result. The factory-trimmed on-chip clock oscillator provides a good and stable timing for most use cases.

22.1 Using the Internal Clock

Directly tie the CLK input to GND near to the IC if the internal clock oscillator is to be used. It will be sufficient for applications, where a velocity precision of roughly +-4% is tolerable.

22.2 Using an External Clock

When an external clock is available, a frequency of 10 MHz to 16 MHz is recommended for optimum performance. The duty cycle of the clock signal is uncritical, as long as minimum high or low input time for the pin is satisfied (refer to electrical characteristics). Up to 18 MHz can be used, when the clock duty cycle is 50%. Make sure, that the clock source supplies clean CMOS output logic levels and steep slopes when using a high clock frequency. The external clock input is enabled with the second positive polarity seen on the CLK input.

Hint
Switching off the external clock frequency prevents the driver from operating normally. Therefore, an internal watchdog switches back to internal clock in case the external signal is missing for more than roughly 32 internal clock cycles.

22.2.1 Considerations on the Frequency

A higher frequency allows faster step rates, faster SPI operation and higher chopper frequencies. On the other hand, it causes more power dissipation in the TMC2160 digital core and 5V voltage regulator. Generally a frequency of 10 MHz to 12 MHz should be sufficient for most applications. At higher clock frequency, the VSA supply voltage should be connected to a lower voltage for applications working at more than 24V nominal supply voltage. For reduced requirements concerning the motor dynamics, a clock frequency of down to 8 MHz (or even lower) can be considered.

23 Absolute Maximum Ratings

The maximum ratings may not be exceeded under any circumstances. Operating the circuit at or near more than one maximum rating at a time for extended periods shall be avoided by application design.

Parameter	Symbol	Min	Max	Unit
Supply voltage operating with inductive load	V_{VS}, V_{VSA}	-0.5	60	V
Supply and bridge voltage short time peak (limited by peak voltage on charge pump output and Cxx pins*)	V_{VSMAX}		64	V
VSA when different from VS	V_{VSAMAX}	-0.5	60	V
Peak voltages on Cxx bootstrap pins and VCP	V_{CxCP}		76	V
Supply voltage V12	V_{12VOUT}	-0.5	14	V
Peak voltages on BM pins (due to stray inductivity)	V_{BMx}	-6	V_{VS}+6	V
Peak voltages on Cxx bootstrap pins relative to BM	V_{CxBMx}	-0.5	16	V
I/O supply voltage on VCC_IO	V_{VIO}	-0.5	5.5	V
digital VCC supply voltage (normally supplied by 5VOUT)	V_{VCC}	-0.5	5.5	V
Logic input voltage	V_I	-0.5	V_{VIO}+0.5	V
Maximum current to / from digital pins and analog low voltage I/Os (short time peak current)	I_{IO}		+/-500	mA
5V regulator output current (internal plus external load)	I_{5VOUT}		30	mA
5V regulator continuous power dissipation (V_{VSA}-5V) * I_{5VOUT}	P_{5VOUT}		1	W
12V regulator output current (internal plus external load)	I_{12VOUT}		20	mA
12V regulator continuous power dissipation (V_{VSA}-12V) * I_{12VOUT}	P_{12VOUT}		0.5	W
Junction temperature	T_J	-50	150	°C
Storage temperature	T_{STG}	-55	150	°C
ESD-Protection for interface pins (Human body model, HBM)	V_{ESDAP}		4	kV
ESD-Protection for handling (Human body model, HBM)	V_{ESD}		1	kV

*) Stray inductivity of power routing will lead to ringing of the supply voltage when driving an inductive load. This ringing results from the fast switching slopes of the driver outputs in combination with reverse recovery of the body diodes of the output driver MOSFETs. Even small trace inductivities as well as stray inductivity of sense resistors can easily generate a few volts of ringing leading to temporary voltage overshoot. This should be considered when working near the maximum voltage.

24 Electrical Characteristics

24.1 Operational Range

Parameter	Symbol	Min	Max	Unit
Junction temperature	T_J	-40	125	°C
Supply voltage for motor and bridge	V_{VS}	10	55	V
Supply voltage VSA	V_{VSA}	10	50	V
Supply voltage for VSA and 12OUT (internal gate voltage regulator bridged)	V_{12VOUT}, V_{VSA}	10	13	V
Lower Supply voltage (reduced spec, short to GND protection not functional), lower limit depending on MOSFETs gate threshold voltage and load current	V_{VS}	8		V
I/O supply voltage on VCC_IO	V_{VIO}	3.00	5.25	V

24.2 DC and Timing Characteristics

DC characteristics contain the spread of values guaranteed within the specified supply voltage range unless otherwise specified. Typical values represent the average value of all parts measured at +25°C. Temperature variation also causes stray to some values. A device with typical values will not leave Min/Max range within the full temperature range.

Power supply current	**DC-Characteristics** V_{VS} = V_{VSA} = 24.0V					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Total supply current, driver disabled I_{VS} + I_{VSA}	I_S	f_{CLK}=12MHz / internal clock		18	24	mA
VSA supply current (VS and VSA separated)	I_{VSA}	f_{CLK}=12MHz / internal clock, driver disabled		15		mA
Total supply current, operating, MOSFETs AOD4126, I_{VS} + I_{VSA}	I_S	f_{CLK}=12MHz, 23.4kHz chopper, no load		25		mA
Internal current consumption from 5V supply on VCC pin	I_{VCC}	f_{CLK}=12MHz		10		mA
Internal current consumption from 5V supply on VCC pin	I_{VCC}	f_{CLK}=16MHz		12.5		mA
IO supply current on VCC_IO (typ. at 5V)	I_{VIO}	no load on outputs, inputs at V_{IO} or GND Excludes pullup / pull-down resistors		15	30	µA

Motor driver section	**DC- and Timing-Characteristics** V_{VS} = 24.0V; Tj=50°C					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
RDS_{ON} lowside off driver	R_{ONL}	Gate off		1.8	3	Ω
RDS_{ON} highside off driver	R_{ONH}	Gate off		2.2	3.5	Ω
Gate drive current low side MOSFET turning on at 2V V_{GS}	I_{SLPON0}	*DRVSTRENGTH*=0		200		mA
	I_{SLPON2}	*DRVSTRENGTH*=2		400		mA
	I_{SLPON3}	*DRVSTRENGTH*=3		600		mA
Gate drive current high side MOSFET turning on at 2V V_{GS}	I_{SLPON0}	*DRVSTRENGTH*=0		150		mA
	I_{SLPON2}	*DRVSTRENGTH*=2		300		mA
	I_{SLPON3}	*DRVSTRENGTH*=3		450		mA
BBM time via internal delay (start of gate switching off to start of gate switching on)	t_{BBM0}	*BBMCLKS*=0 *BBMTIME*=0	75	100		ns
	t_{BBM16}	*BBMTIME*=16		200		ns
	t_{BBM16}	*BBMTIME*=24		375	500	ns

Charge pump	**DC-Characteristics**					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Charge pump output voltage	V_{VCP}-V_{VS}	operating	V_{12VOUT} - 2	V_{12VOUT} - 1		V
Charge pump voltage threshold for undervoltage detection	V_{VCP}-V_{VS}	rising, using internal 5V regulator voltage	4.5	5	6.5	V
Charge pump frequency	f_{CP}			1/16 f_{CLKOSC}		

Linear regulator	**DC-Characteristics** V_{VS} = V_{VSA} = 24.0V					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Output voltage	V_{5VOUT}	T_J = 25°C	4.80	5.0	5.20	V
Deviation of output voltage over the full temperature range	$V_{5VOUT(DEV)}$	drivers disabled T_J = full range		+/-30	+/-100	mV
Deviation of output voltage over the full supply voltage range	$V_{5VOUT(DEV)}$	drivers disabled, internal clock T_A = 25°C V_{VSA} = 10V to 30V			+/-50	mV / 10V
Output voltage	V_{12VOUT}	operating, internal clock T_J = 25°C	10.8	11.5	12.2	V

Clock oscillator and input	**Timing-Characteristics**					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Clock oscillator frequency (factory calibrated)	f_{CLKOSC}	t_J=-50°C		11.7		MHz
	f_{CLKOSC}	t_J=50°C	11.5	12.0	12.5	MHz
	f_{CLKOSC}	t_J=150°C		12.1		MHz
External clock frequency (operating)	f_{CLK}		4	10-16	18	MHz
External clock high / low level time	t_{CLKH} / t_{CLKL}	CLK driven to 0.1 V_{VIO} / 0.9 V_{VIO}	10			ns
External clock timeout detection in cycles of internal f_{CLKOSC}	t_{CLKH1}	CLK driven high	32		48	cycles f_{CLKOSC}

Short detection	**DC-Characteristics**					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Short to GND / Short to VS detector delay (Start of gate switch on to short detected) Including 100ns filtering time	t_{SD0}	*FILT_ISENSE*=0 *S2xx_LEVEL*=6 *shortdelay*=0	0.5	0.85	1.1	µs
	t_{SD1}	*shortdelay*=1	1.1	1.6	2.2	µs
Short detector level S2VS (measurement includes drop in sense resistor)	V_{BM}	*S2VS_LEVEL*=15	1.4	1.56	1.72	V
		S2VS_LEVEL=6	0.55	0.625	0.70	V
Short detector level S2G	V_S - V_{BM}	*S2G_LEVEL*=15; VS<52V	1.2	1.56	1.9	V
		S2G_LEVEL=15; VS<55V	0.85			V
		S2G_LEVEL=6; VS<52V	0.46	0.625	0.80	V

Detector levels	**DC-Characteristics**					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
V_{VSA} undervoltage threshold for RESET	V_{UV_VSA}	V_{VSA} rising	3.6	4	4.6	V
V_{5VOUT} undervoltage threshold for RESET	V_{UV_5VOUT}	V_{5VOUT} rising		3.5		V
V_{VCC_IO} undervoltage threshold for RESET	V_{UV_VIO}	V_{VCC_IO} rising (delay typ. 10µs)	2.0	2.5	3.0	V
V_{VCC_IO} undervoltage detector hysteresis	$V_{UV\_VIOHYST}$			0.3		V
Overtemperature prewarning 120°C	T_{OTPW}	Temperature rising	100	120	140	°C
Overtemperature shutdown 136 °C	T_{OT136}	Temperature rising		136		°C
Overtemperature shutdown 143 °C	T_{OT143}	Temperature rising		143		°C
Overtemperature shutdown 150 °C	T_{OT150}	Temperature rising	135	150	170	°C

Sense resistor voltage levels	**DC-Characteristics** **f_{CLK}=16MHz**					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Sense input peak threshold voltage (low sensitivity) (V_{SRxH}-V_{SRxL})	V_{SRT}	*GLOBALSCALER*=0 *csactual*=31 *sin_x*=248 Hyst.=0; I_{BRxy}=0		325		mV
Sense input tolerance / motor current full scale tolerance -using internal reference	I_{COIL}	*GLOBALSCALER*=0	-5		+5	%

Digital pins	**DC-Characteristics**					
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Input voltage low level	V_{INLO}		-0.3		0.3 V_{VIO}	V
Input voltage high level	V_{INHI}		0.7 V_{VIO}		V_{VIO}+0.3	V
Input Schmitt trigger hysteresis	V_{INHYST}			0.12 V_{VIO}		V
Output voltage low level	V_{OUTLO}	I_{OUTLO} = 2mA			0.2	V
Output voltage high level	V_{OUTHI}	I_{OUTHI} = -2mA	V_{VIO}-0.2			V
Input leakage current	I_{ILEAK}		-10		10	µA
Pullup / pull-down resistors	R_{PU}/R_{PD}		132	166	200	kΩ
Digital pin capacitance	C			3.5		pF

24.3 Thermal Characteristics

The following table shall give an idea on the thermal resistance of the package. The thermal resistance for a four-layer board will provide a good idea on a typical application. Actual thermal characteristics will depend on the PCB layout, PCB type and PCB size. The thermal resistance will benefit from thicker CU (inner) layers for spreading heat horizontally within the PCB. Also, air flow will reduce thermal resistance.

Parameter	Symbol	Conditions	Typ	Unit
Typical power dissipation	P_D	stealthChop or spreadCycle, 40 or 20kHz chopper, 24V, internal supply regulators	0.6	W
Thermal resistance junction to ambient on a multilayer board	R_{TMJA}	Dual signal and two internal power plane board (2s2p) as defined in JEDEC EIA JESD51-5 and JESD51-7 (FR4, 35µm CU, 70mm x 133mm, d=1.5mm)	21	K/W
Thermal resistance junction to board	R_{TJB}	PCB temperature measured within 1mm distance to the package leads	8	K/W
Thermal resistance junction to case	R_{TJC}	Junction temperature to heat slug of package	3	K/W

Table 24.1 Thermal characteristics TQFP48-EP

The thermal resistance in an actual layout can be tested by checking for the heat up caused by the standby power consumption of the chip. When no motor is attached, all power seen on the power supply is dissipated within the chip.

25 Layout Considerations

25.1 Exposed Die Pad

The TMC2160 uses its die attach pad to dissipate heat from the gate drivers and the linear regulator to the board. For best electrical and thermal performance, use a reasonable amount of solid, thermally conducting vias between the die attach pad and the ground plane. The printed circuit board should have a solid ground plane spreading heat into the board and providing for a stable GND reference.

25.2 Wiring GND

All signals of the TMC2160 are referenced to their respective GND. Directly connect all GND pins under the device to a common ground area (GND, GNDP, GNDA and die attach pad). The GND plane right below the die attach pad should be treated as a virtual star point. For thermal reasons, the PCB top layer shall be connected to a large PCB GND plane spreading heat within the PCB.

Attention
Place the TMC2160 near to the MOSFET bridge and sense resistor GND in order to avoid ringing leading to GND differences and to dangerous inductive peak voltages.

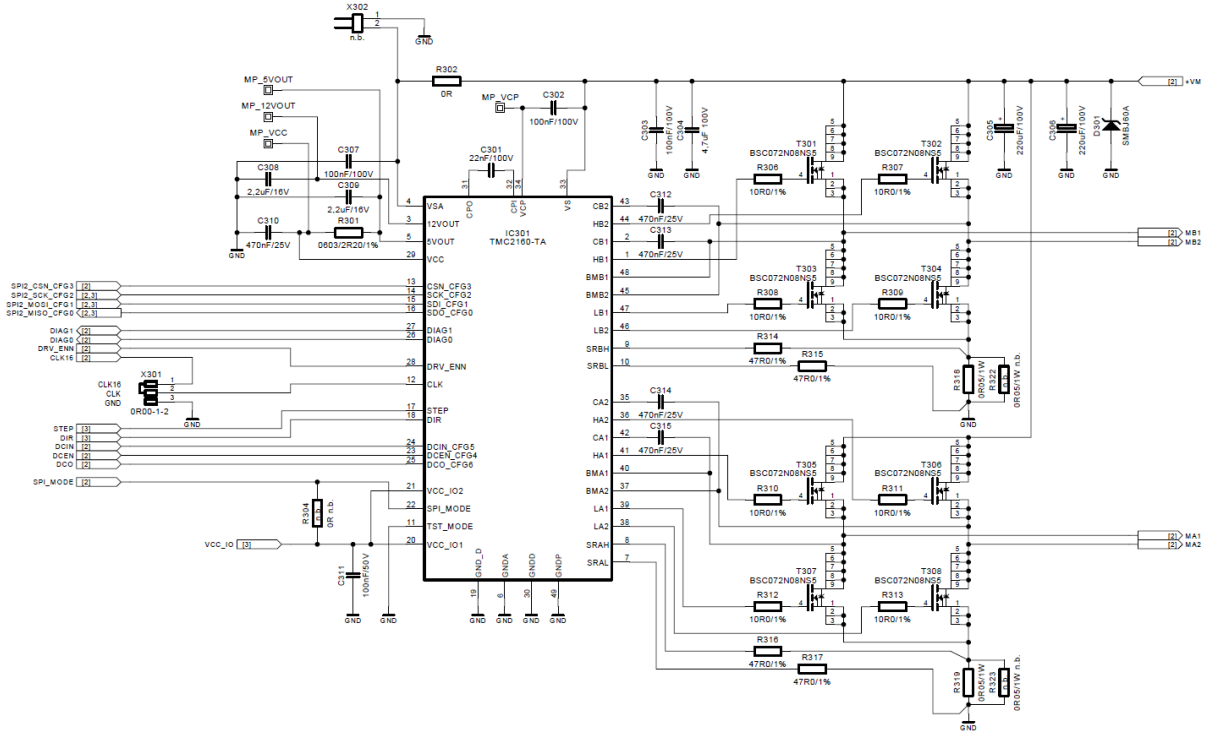
25.3 Supply Filtering

The 5VOUT output voltage ceramic filtering capacitor (2.2 to 4.7 µF recommended) should be placed as close as possible to the 5VOUT pin, with its GND return going directly to the GNDA pin. This ground connection shall not be shared with other loads or additional vias to the GND plane. Use as short and as thick connections as possible. For best microstepping performance and lowest chopper noise an additional filtering capacitor should be used for the VCC pin to GND, to avoid digital part ripple influencing motor current regulation. Therefore, place a ceramic filtering capacitor (470nF recommended) as close as possible (1-2mm distance) to the VCC pin with GND return going to the ground plane. VCC can be coupled to 5VOUT using a 2.2 Ω or 3.3 Ω resistor in order to supply the digital logic from 5VOUT while keeping ripple away from this pin. A 100 nF filtering capacitor should be placed as close as possible to the VSA pin to ground plane.

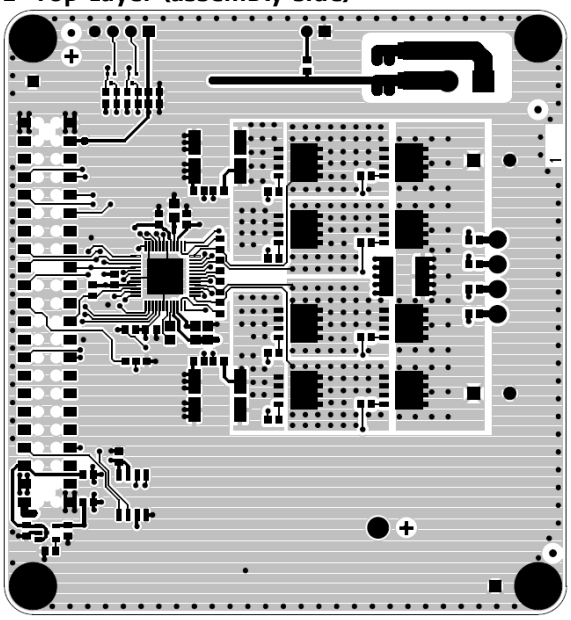
Please carefully read chapters 3.3 and 3.4 to understand the special considerations with regard to layout and component selection for the external MOSFET power bridges.

25.4 Layout Example

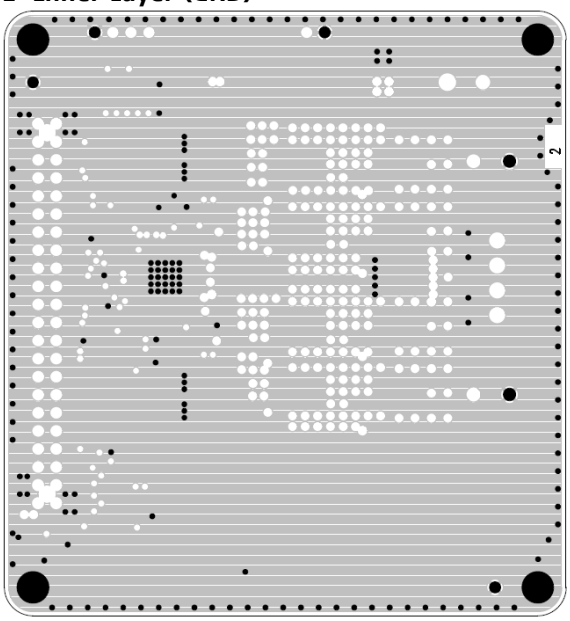
Schematic (TMC2160+MOSFETs shown)



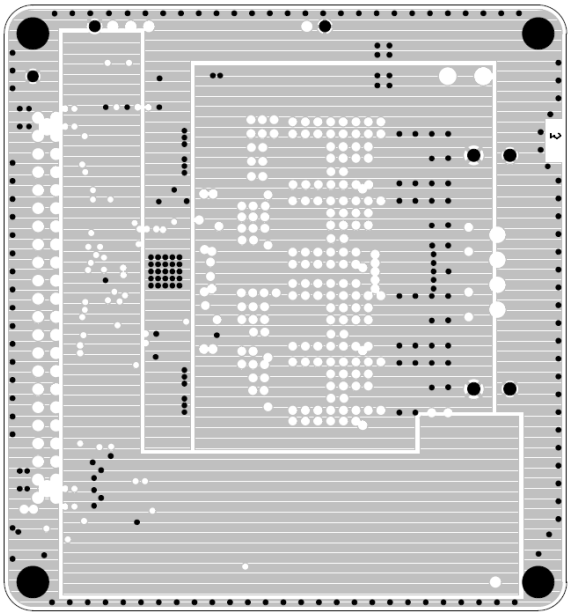
1- Top Layer (assembly side)



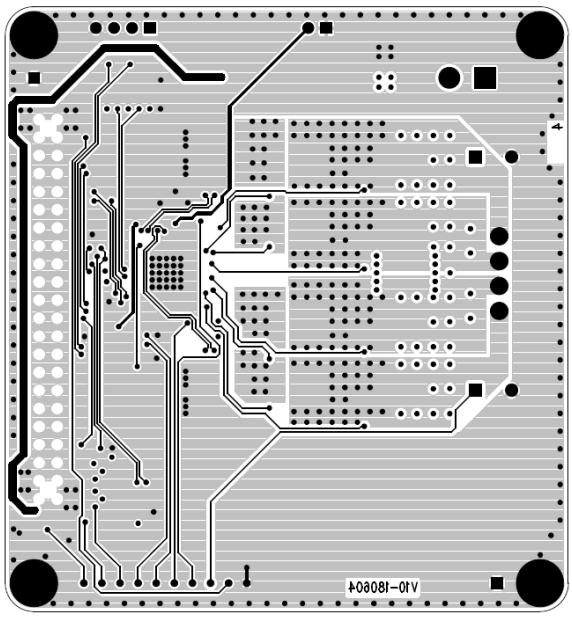
2- Inner Layer (GND)



3- Inner Layer (supply VS)



4- Bottom Layer



Components

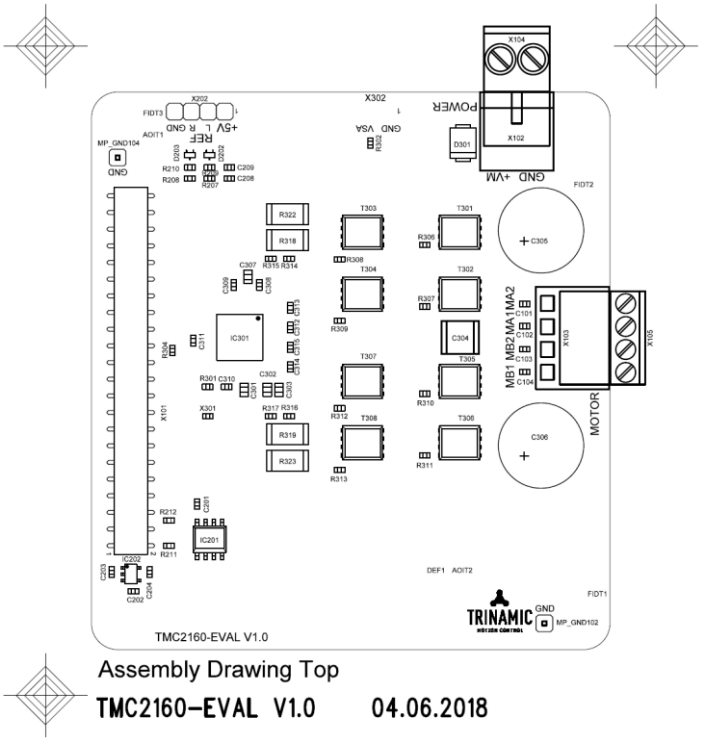


Figure 25.1 Layout example

26 Package Mechanical Data

26.1 Dimensional Drawings TQFP48-EP

Drawings not to scale.

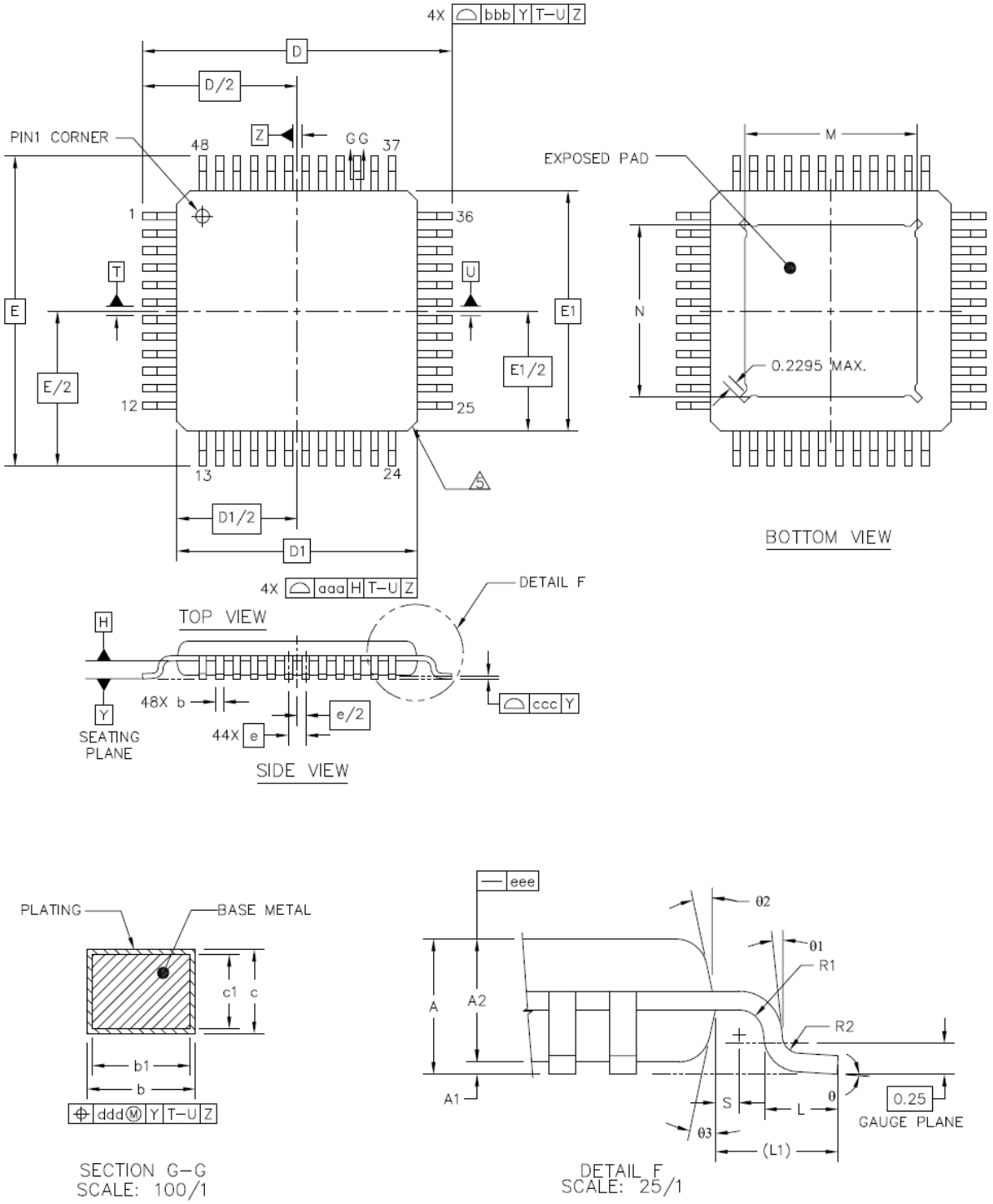


Figure 26.1 Dimensional drawings TQFP48-EP

Parameter	Ref	Min	Nom	Max
total thickness	A	-	-	1.2
stand off	A1	0.05	-	0.15
mold thickness	A2	0.95	1	1.05
lead width (plating)	b	0.17	0.22	0.27
lead width	b1	0.17	0.2	0.23
lead frame thickness (plating)	c	0.09	-	0.2
lead frame thickness	c1	0.09	-	0.16
body size X (over pins)	D		9.0	
body size Y (over pins)	E		9.0	
body size X	D1		7.0	
body size Y	E1		7.0	
lead pitch	e		0.5	
lead	L	0.45	0.6	0.75
footprint	L1		1 REF	
	Θ	0°	3.5°	7°
	Θ1	0°	-	-
	Θ2	11°	12°	13°
	Θ3	11°	12°	13°
	R1	0.08	-	-
	R2	0.08	-	0.2
	S	0.2	-	-
exposed die pad size X	M	4.9	5	5.1
exposed die pad size Y	N	4.9	5	5.1
package edge tolerance	aaa			0.2
lead edge tolerance	bbb			0.2
coplanarity	ccc			0.08
lead offset	ddd			0.08
mold flatness	eee			0.05

26.2 Package Codes

Type	Package	Temperature range	Code & marking
TMC2160-TA	TQFP-EP48 (RoHS)	-40°C … +125°C	TMC2160-TA

27 Disclaimer

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28 ESD Sensitive Device

The TMC2160 is an ESD sensitive CMOS device sensitive to electrostatic discharge. Take special care to use adequate grounding of personnel and machines in manual handling. After soldering the devices to the board, ESD requirements are more relaxed. Failure to do so can result in defect or decreased reliability.

29 Table of Figures

30 Revision History

Version	Date	Author BD= Bernhard Dwersteg	Description
V0.91	2018-MAY-25	BD	First version of datasheet based on datasheet TMC5160 V1.04
V1.00	2018-JUN-06	BD	Added errata / limitations for initial tuning of AT#1 / AT#2 phase Minor wording, added evaluation board drawing
V1.01	2018-OKT-29	BD	Minor changes, added -T suffix option, S2G >52V hints/limits updated

Table 30.1 Document Revisions

31 References

[TMC2160-EVAL] TMC2160-EVAL Manual
[AN001] Trinamic Application Note 001 - Parameterization of spreadCycle™, www.trinamic.com
[AN002] Trinamic Application Note 002 - Parameterization of stallGuard2™ & coolStep™, www.trinamic.com
[AN003] Trinamic Application Note 003 - dcStep™, www.trinamic.com
Calculation sheet TMC2160_Calculations.xlsx