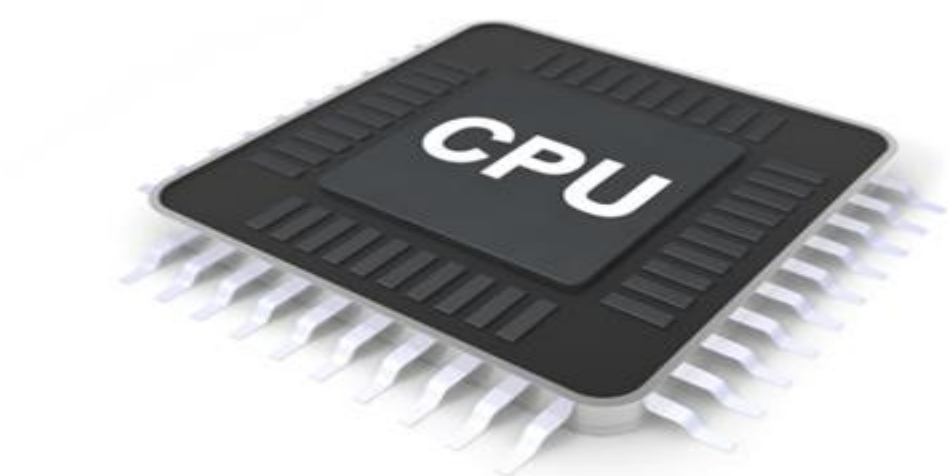


Memory Organization

ENEE 3582

Microp

Memory Terminology

- Memory type: 2 major types: ROM/RAM
- Memory capacity
  - Amount of data that can be stored
  - Measured in bytes. Units: KB (KiB), MB (MiB), GB (GiB)
- Memory operations
  - Read (aka load): data transfers from mem to cpu
  - Write (aka store): data transfers from cpu to mem
- Memory Busses
  - Address Bus: carries address to mem
  - Data Bus: carries data contents to (write op) and from (read op) mem
  - Control
- Memory Architecture: How memory chips are interfaced with CPU

RAM

- Random-access memory (RAM):
  - Allows read and writing of memory
  - Same amount of time is required to access any location on the same chip
  - Volatile: information is lost without power.
  - Used to store user's programs
- Dynamic RAM (DRAM):
  - Uses 1 transistor and 1 capacitor for 1 bit.
  - Periodic refresh is required to maintain the contents of chip.
  - Asynchronous
  - SDRAM: synchronous DRAM (edge triggered)
- Static RAM (SRAM):
  - No periodic refresh is required
  - Uses 4-6 transistors for 1 bit

ROM

- Read-only memory (ROM):
  - Can only be read but not written by the processor
  - Nonvolatile
- Mask-programmed ROM (MROM):
  - Programmed when being manufactured
- Programmable ROM (PROM):
  - Programmed by the end user
- Erasable programmable ROM (EPROM)
  - Electrically programmable many times
  - Erased by ultraviolet light
  - Erasable in bulk (whole chip in one erasure operation)

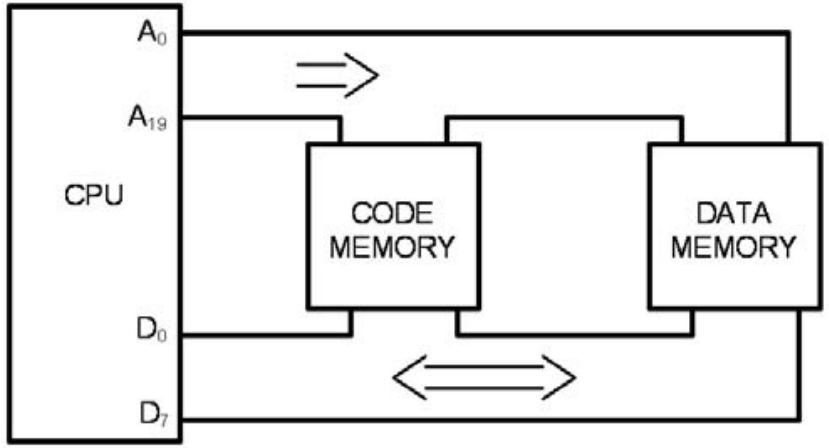
ROM

- Electrically erasable programmable ROM (EEPROM)
  - Electrically programmable many times
  - Electrically erasable many times
  - Erased one location, one row, or whole chip in one operation
  - Erased without removing unit from device.
- Flash EEPROM
  - Electrically programmable many times
  - Electrically erasable many times
  - Erased in bulk/large blocks => faster than EEPROM

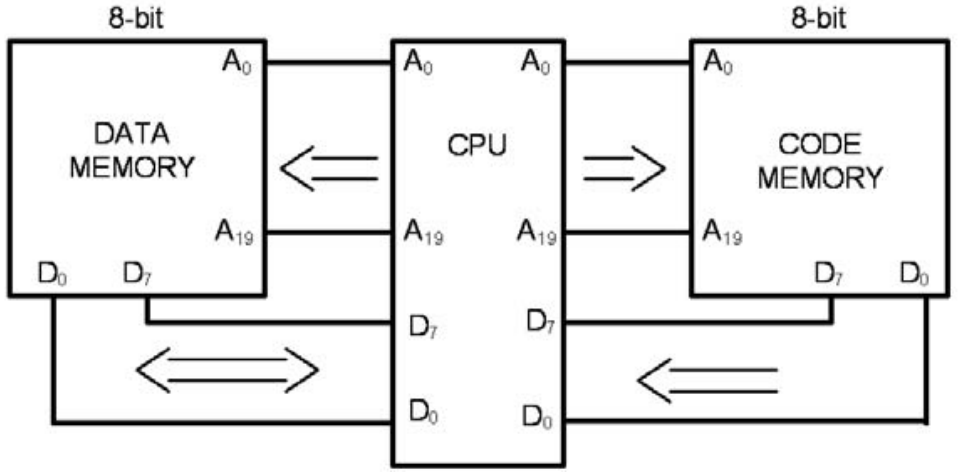
Harvard vs Princeton Memory Architectures

- Von Neumann (Princeton) architecture
  - One memory, one bus
  - Code and Data accessed on the same bus
  - Memory “collisions”
- Harvard architecture
  - Separate memory for code and data memory
  - Separate busses
  - Expensive: Double memory pins for external memory
- AVR Solution:
  - Harvard internal memory
  - Von Neumann for external memory
  -

von Neumann Architecture



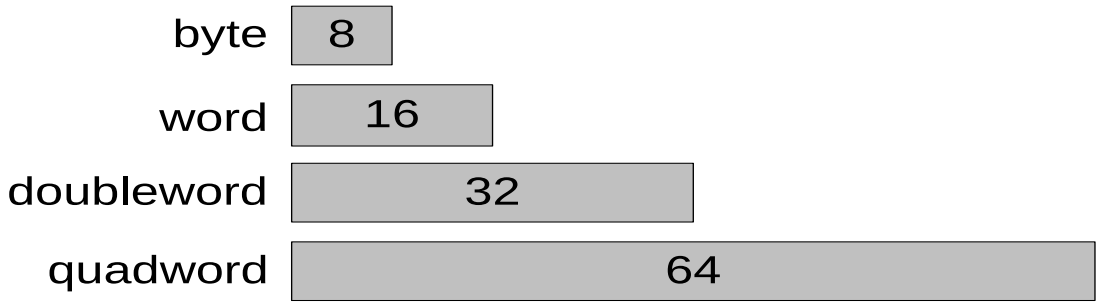
Harvard Architecture



A. Mazidi

Data Sizes

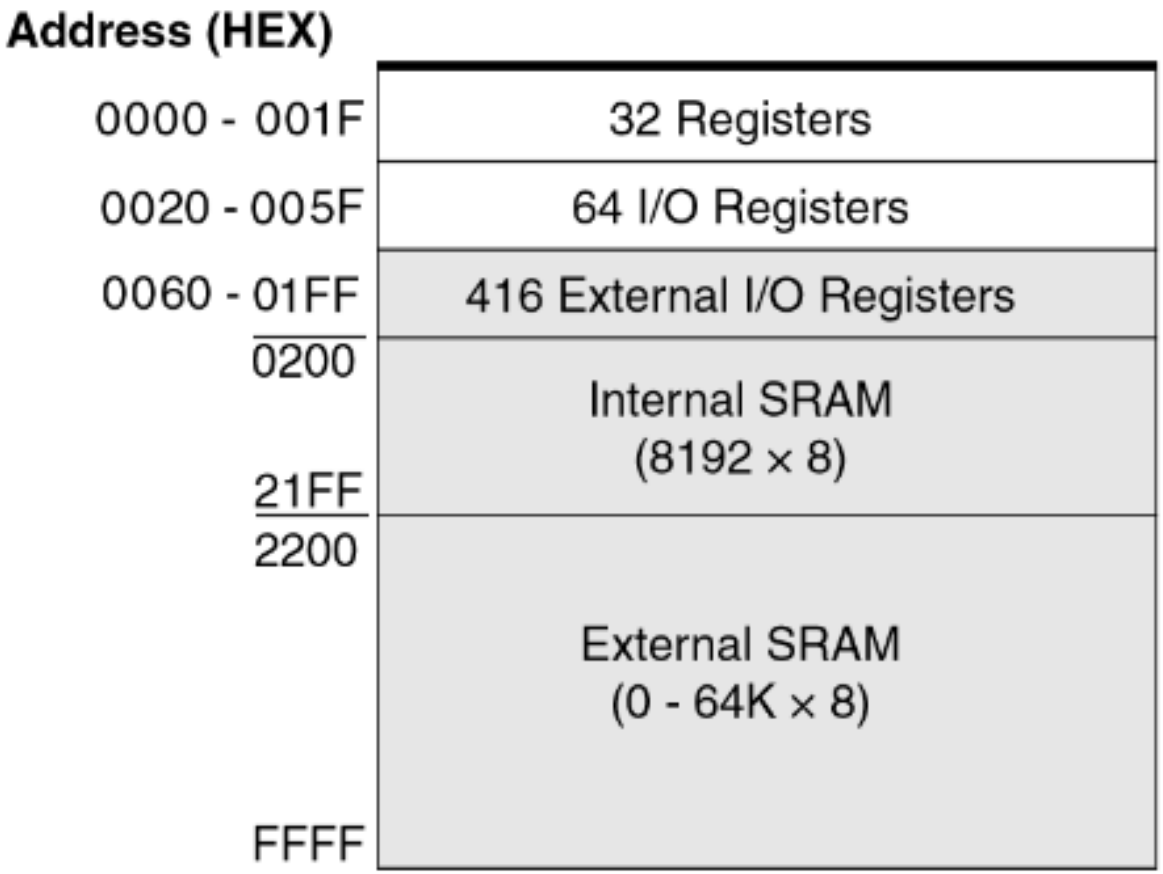
- Bit: singe binary unit
- Byte: 8-bits, unit: B
- Word: 16-bits, 2B
- Doubleword: 32-bits, 4B
- Quadword: 64-bits, 8B



Memory Organization

- Memory is organized by addresses
  - Each address points to a memory location
  - n bit address = 2^n locations
- Memory is grouped (measured) into byte locations
- Program Memory:
  - Mega2560: 256KB Flash
  - Address in PC (17bits)
  - Each location is 2B
  - Starting location = 0x00000
- Data Memory:
  - Mega2560: 8KB internal SRAM, 0-64KB external SRAM
  - Each location is a 1B
  - Starting address = 0x0200 (internal), 0x2200 (external)

Mega 2560


Address (HEX)
0000 - 001F
32 Registers
0020 - 005F
64 I/O Registers
0060 - 01FF
416 External I/O Registers
0200
Internal SRAM
(8192 × 8)
21FF
2200
External SRAM
(0 - 64K × 8)
FFFF

Accessing Data

- Use index regs to access program data
  - X, Y, Z
- Program Data:
  - 256KB flash for program data
  - Data stored in 2B
    - Each address points to a word
    - Address must be scaled by 2
- RAM data:
  - **I**nternal/e**X**trernal S**RAM**
  - 8KB for IRAM
  - Data stored in B
    - No need for scaling