8-bit vs 16-bit Timers

- 2x8-bit Timer 0,1
- 8-bit counter
- 2 output compares per timer
  - OCA, OCB
- PWM per timer
  - Fast, Phase correct

- 4x16-bit Timers 1,3,4,5
- 16-bit counter: higher delay times
- 3 output compares per timer
  - OCA, OCB, OCC
- PWM per timer
  - fast, phase correct, freq&phase correct
- 1 input capture per timer
  - ICP

Pins

Pin Name	OC/IC	Mapped
PB7	OC0A/OC1C	Digital pin 13 PWM
PG5	OC0B	Digital pin 4 PWM
PB5	OC1A	Digital pin 11 PWM
PB6	OC1B	Digital pin 12 PWM
PB7	OC1C/OC0A	Digital pin 13 PWM
PD4	ICP1	No pin connection
PB4	OC2A	Digital pin 10 PWM
PH6	OC2B	Digital pin 9 PWM
PE3	OC3A	Digital pin 5 PWM
PE4	OC3B	Digital pin 2 PWM
PE5	OC3C	Digital pin 3 PWM
PE7	ICP3	No pin connection
PH3	OC4A	Digital pin 6 PWM
PH4	OC4B	Digital pin 7 PWM
PH5	OC4C	Digital pin 8 PWM
PL0	ICP4	Digital pin 49
PL3	OC5A	Digital pin 46 PWM
PL4	OC5B	Digital pin 45 PWM
PL5	OC5C	Digital pin 44 PWM
PL1	ICP5	Digital pin 48

8-bit Timer Registers

- Timer **n** = 0,2
- Registers:
  - TCNT**n**: 8-bit counter register
  - TCCR**n**A: timer/counter control register A
  - TCCR**n**B: timer/counter control register B
  - ASSR: timer asynchronous status register
  - OCR**n**A: output compare register A
  - OCR**0**B: output compare register B
  - TIMSK**n**: timer counter interrupt mask register
  - TIFR**n**: timer counter interrupt flag register

8-bit Timer: TCCR**n**A

7	6	5	4	3	2	1	0	
COMnA1	COMnA0	COMnB1	COMnB0	—	—	WGMn1	WGMn0	Reset value = 0x00
R/W	R/W	R/W	R/W	R	R	R/W	R/W	

- **COM**n**A1:COM**n**A0**: Compare match output mode A (n = timer 0 or 2)
  - Controls behavior of output
- **COM**n**B1:COM**n**A0**: Compare match output mode B (n = timer 0 or 2)
- **WGM**n**1:0**: Waveform generation mode bits
  - Helps control the counting sequence,
  - source for maximum (TOP) counter value,
  - type of waveform generation,
  - modes of operation

8-bit Timer: TCCR0B

7	6	5	4	3	2	1	0	
FOC0A	FOC0B	—	—	WGM02	CS02	CS01	CS00	Reset value = 0x00
W	W	R	R	R/W	R/W	R/W	R/W	

- **FOC0A**: Force output compare A
  - Force a change in output when a 1 is written to this bit (non-PWM mode)
  - No interrupt will be generated.
  - This bit is read as 0.
- **FOC0B**: Force output compare B
- **WGM02**: Waveform generation mode bit 2
- **CS02-CS00**: Clock select
  - 000: No clock source (Timer/Counter stops)
  - 001: clkI/O (no prescaling)
  - 010: clkI/O /8 (from prescaler)
  - 011: clkI/O /64 (from prescaler)
  - 100: clkI/O /256 (from prescaler)
  - 101: clkI/O /1024 (from prescaler)
  - 110: External clock source on T0 pin. Clock on falling edge
  - 111: External clock source on T0 pin. Clock on rising edge

8-bit Timer Modes (TCCR)

- Normal operation: no output compare
  - Typically used for creating variable time delays
  - OC Mode: Generating binary output at specific counts
- CTC: Clear time on compare
  - Typically used for creating periodic time delays/functions
- PWM Mode: Pulse-width modulation
  - Fast PWM: high frequency PWM
  - Phase-correct PWM: high resolution PWM

Mode	WGM2	WGM1	WGM0	Timer/Counter mode of operation	TOP	Update of OCRx at	TOV flag set on[1)2)]
0	0	0	0	Normal	0xFF	immediate	MAX
1	0	0	1	PWM, phase correct	0xFF	TOP	BOTTOM
2	0	1	0	CTC	OCRnA	immediate	MAX
3	0	1	1	Fast PWM	0xFF	TOP	MAX
4	1	0	0	Reserved	—	—	—
5	1	0	1	PWM, phase correct	OCRnA	TOP	BOTTOM
6	1	1	0	Reserved	—	—	—
7	1	1	1	Fast PWM	OCRnA	BOTTOM	TOP

Notes: 1. MAX = 0xFF.
2. BOTTOM = 0x00.

8-bit TCCR**n**A : COM**nx**1:COM**nx**2

- n = 0 or 2
- x = A or B

Compare match output behavior in **non-PWM** mode (8-bit timer)

COMnx1	COMnx0	Description
0	0	Normal PORT operation, OCnx flip-flop disconnected from OCnx pin
0	1	Toggle OCnx signal on compare match
1	0	Clear OCnx signal on compare match
1	1	Set OCnx signal on compare match

Compare match output behavior in **Fast-PWM** mode (**WGMn2:0 = 011**, TOP = 0xFF)

COMnx1	COMnx0	Description
0	0	Normal PORT operation, OCnx flip-flop disconnected from OCnx pin
0[1]	1[1]	Normal PORT operation, OCnA flip-flop disconnected from OCnA pin
1	0	Clear OCnx signal on compare match, set OCnx at BOTTOM (non-inverting mode)
1	1	Set OCnx signal on compare match, clear OCnx at BOTTOM (inverting mode)

Note: 1. This option is not available for OCnB (n = 0 or 2) module.

Compare match output behavior in **Fast-PWM** mode (**WGMn2:0 = 111**, TOP = OCRnA)

COMnx1	COMnx0	Description
0	0	Normal PORT operation, OCnx flip-flop disconnected from OCnx pin
0[1]	1[1]	Toggle OCnA on compare match
1	0	Set OCnx at BOTTOM (non-inverting mode)
1	1	Clear OCnx at BOTTOM (inverting mode)

Note: 1. This option is not available for OCnB (n = 0 or 2) module.

Compare match output behavior in **Phase-Correct-PWM** mode[1] (8-bit timer)

COMnx1	COMnx0	Description
0	0	Normal PORT operation, OCnx flip-flop disconnected from OCnx pin
0[2]	1[2]	WGMn2=0: normal PORT operation, OCnA flip-flop disconnected from OCnA pin WGMn2=1: Toggle OCnA on compare match
1	0	Clear OCnx flip-flop on compare match during up-counting Set OCnx flip-flop on compare match during down-counting
1	1	Set OCnx flip-flop on compare match during up-counting Clear OCnx flip-flop on compare match during down-counting

Notes: 1. A special case occurs when OCRnx equals TOP and COMnx1 is set to 1. In this case, the compare match is ignored, but the set or clear is done at the TOP.
2. This option is not available for OCnB (n = 0 or 2) module.

8-bit Timer: TIFR0,2

7	6	5	4	3	2	1	0	
—	—	—	—	—	OCFnB	OCFnA	TOVn	Reset va = 0x00
R	R	R	R	R	R	R	R	

- **OCF<u>n</u>B**: Timer/Counter n output compare match B flag (**<u>n</u>**=0 or 2)
  - 0 = Compare match between TCNT<u>n</u> and OCR<u>n</u>B did not occur.
  - 1 = Compare match between TCNT<u>n</u> and OCR<u>n</u>B has occurred.
- **OCF<u>n</u>A**: Timer/Counter n output compare match A flag
  - 0 = Compare match between TCNT<u>n</u> and OCR<u>n</u>A did not occur.
  - 1 = Compare match between TCNT<u>n</u> and OCR<u>n</u>A has occurred.
- **TOV<u>n</u>**: Timer/Counter n overflow interrupt enable
  - 0 = TCNT<u>n</u> hasn't overflown since this flag was last cleared.
  - 1 = TCNT<u>n</u> has overflown since this flag was last cleared.
- To clear flags write a 1 into the flag

8-bit Timer: TIMSK0,2

7	6	5	4	3	2	1	0	
—	—	—	—	—	OCIEnB	OCIEnA	TOIEn	Reset value = 0x00
R	R	R	R	R	R/W	R/W	R/W	

- **OCIE<u>n</u>B**: Timer/Counter n output compare match B interrupt enable (**<u>n</u>** = 0 or 2)
  - 0 = Disable the OCnB match interrupt
  - 1 = Enable the OCnB match interrupt
- **OCIE<u>n</u>A**: Timer/Counter n output compare match A interrupt enable (**<u>n</u>** = 0 or 2)
  - 0 = Disable the OCnA match interrupt
  - 1 = Enable the OCnA match interrupt
- **TOIE<u>n</u>**: Timer/Counter n overflow interrupt enable (**<u>n</u>** = 0 or 2)
  - 0 = Disable Timer/Counter n overflow interrupt
  - 1 = Enable Timer/Counter n overflow interrupt

16-bit Timer Registers

- Timer **<u>n</u>** =1,3,4,5
- Registers:
  - TCNT**<u>n</u>**H/TCNT**<u>n</u>**L: High and Low 16-bit counter registers (8-bit each)
  - TCCR**<u>n</u>**A: timer/counter control register A
  - TCCR**<u>n</u>**B: timer/counter control register B
  - TCCR**<u>n</u>**C: timer/counter control register C
  - OCR**<u>n</u>**AH, OCR**<u>n</u>**AL: High and Low output compare register A
  - OCR**<u>n</u>**BH, OCR**<u>n</u>**BL: High and Low output compare register B
  - OCR**<u>n</u>**CH, OCR**<u>n</u>**CL: High and Low output compare register C
  - ICR**<u>n</u>**H, ICR**<u>n</u>**L: High and Low input capture register
  - TIMSK**<u>n</u>**: timer counter interrupt mask register
  - TIFR**<u>n</u>**: timer counter interrupt flag register

16-bit : TCCR1A, TCCR3A, TCCR4A, TCCR5A,

7	6	5	4	3	2	1	0	
COMnA1	COMnA0	COMnB1	COMnB0	COMnC1	COMnC0	WGMn1	WGMn0	Reset value = 0x00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- **COM<u>n</u>A1:0**: Compare output mode for channel A (**<u>n</u>** = 1, 3, 4, or 5)
- **COM<u>n</u>B1:0**: Compare output mode for channel B
- **COM<u>n</u>C1:0**: Compare output mode for channel C
  - Controls the compare match behavior.
- **WGMn1:0**: Waveform generation mode bits
  - Helps control the counting sequence,
  - source for maximum (TOP) counter value,
  - type of waveform generation,
  - modes of operation

16-bit: TCCR1B, TCCR3B, TCCR4B, TCCR5B

7	6	5	4	3	2	1	0	
ICNCn	ICESn	—	WGMn3	WGMn2	CSn2	CSn1	CSn0	Reset value = 0x00
R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	

- **ICNC<u>n</u>**: Input-capture noise canceler (**<u>n</u>** = 1,3,4,5)
  - 0 = Disable input-capture noise canceler.
  - 1 = Enable input-capture noise canceler.
- **ICES<u>n</u>**: Input-capture edge select
  - 0 = Falling edge triggers input capture.
  - 1 = Rising edge triggers input capture.
  - (If ICRn is used as TOP value, then the ICPn is disconnected and input capture is disabled).
- **WGM<u>n</u>3:2**: Waveform generation mode bits 3 and 2
- **CS<u>n</u>2-CS<u>n</u>0**: Clock select
  - 000 = No clock source (Timer/Counter stopped)
  - 001 = clkI/O (no prescaling)
  - 010 = clkI/O /8 (from prescaler)
  - 011 = clkI/O /64 (from prescaler)
  - 100 = clkI/O /256 (from prescaler)
  - 101 = clkI/O /1024 (from prescaler)
  - 110 = External clock source on Tn pin. Clock on falling edge
  - 111 = External clock source on Tn pin. Clock on rising edge

16-bit Timer Modes

Mode	WGMn3	WGMn2	WGMn1	WGMn0	Timer/Counter mode of operation	TOP	Update of OCRx at	TOV flag set on
0	0	0	0	0	Normal	0xFFFF	Immediate	MAX
1	0	0	0	1	PWM, phase correct, 8-bit	0x00FF	TOP	BOTTOM
2	0	0	1	0	PWM, phase correct, 9-bit	0x01FF	TOP	BOTTOM
3	0	0	1	1	PWM, phase correct, 10-bit	0x03FF	TOP	BOTTOM
4	0	1	0	0	CTC	OCRnA	Immediate	MAX
5	0	1	0	1	Fast PWM, 8-bit	0x00FF	BOTTOM	TOP
6	0	1	1	0	Fast PWM, 9-bit	0x01FF	BOTTOM	TOP
7	0	1	1	1	Fast PWM, 10-bit	0x03FF	BOTTOM	TOP
8	1	0	0	0	PWM, phase and frequency correct	ICRn	BOTTOM	BOTTOM
9	1	0	0	1	PWM, phase and frequency correct	OCRnA	BOTTOM	BOTTOM
10	1	0	1	0	PWM, phase correct	ICRn	TOP	BOTTOM
11	1	0	1	1	PWM, phase correct	OCRnA	TOP	BOTTOM
12	1	1	0	0	CTC	ICRn	Immediate	MAX
13	1	1	0	1	(Reserved)	–	–	–
14	1	1	1	0	Fast PWM	ICRn	BOTTOM	TOP
15	1	1	1	1	Fast PWM	OCRnA	BOTTOM	TOP

16-bit TCCR**n**A : COM**nx**1,COM**nx**2

- **n** = 1,3,4,5
- **x** = A,B,C

Compare match output behavior in **non-PWM** mode (16-bit timer)

COMnx1	COMnx0	Description
0	0	Normal PORT operation, OCnA/OCnB/OCnC disconnected
0	1	Toggle OCnA/OCnB/OCnC on compare match
1	0	Clear OCnA/OCnB/OCnC (pull low) on compare match
1	1	Set OCnA/OCnB/OCnC (pull high) on compare match

Compare match output behavior in **Fast-PWM** mode (16-bit timer)

COMnx1	COMnx0	Description
0	0	Normal PORT operation, OCnA/OCnB/OCnC disconnected
0	1	WGMn 3:0 = 14 or 15: toggle OCnA on compare match, OCnB and OCnC disconnected (normal PORT operation). For all other PWM WGMn settings, normal PORT operation, OCnA/OCnB/OCnC disconnected.
1	0	Clear OCnA/OCnB/OCnC (pull low) on compare match, set OCnA/OCnB/OCnC at BOTTOM (non-inverting mode)
1	1	Set OCnA/OCnB/OCnC (pull high) on compare match, clear OCnA/OCnB/OCnC at BOTTOM (inverting mode)

Compare output mode, **Phase Correct** and **Phase-and-Frequency-Correct PWM** mode (16-bit)

COMnx1	COMnx0	Description
0	0	Normal PORT operation, OCnA/OCnB/OCnC disconnected
0	1	WGMn 3:0 = 9 or 11: toggle OCnA on compare match, OCnB and OCnC disconnected (normal PORT operation). For all other PWM WGMn settings, normal PORT operation, OCnA/OCnB/OCnC disconnected.
1	0	Clear OCnA/OCnB/OCnC (pull low) on compare match when up-counting, set OCnA/OCnB/OCnC on compare match when down-counting
1	1	Set OCnA/OCnB/OCnC (pull high) on compare match when up-counting. Clear OCnA/OCnB/OCnC on compare match when down-counting.

16-bit : TCCR1C, TCCR3C TCCR4C, TCCR5C

7	6	5	4	3	2	1	0	
FOCnA	FOCnB	FOCnC	—	—	—	—	—	Reset value = 0x00
R/W	R/W	R/W	R	R	R	R	R	

- **FOC**n**A**: Force output compare for channel A (**n**= 1,3,4,5)
- **FOC**n**B**: Force output compare for channel B
- **FOC**n**C**: Force output compare for channel C
  - These bits are active only when WGMn3:0 bits specify a non-PWM mode.
  - FOC**n**A/FOCnB/FOCnC = 1 => OCnA/OCnB/OCnC output is changed

16-bit: TIFR**n**

7	6	5	4	3	2	1	0	
—	—	ICFn	—	OCFnC	OCFnB	OCFnA	TOVn	Reset va = 0x00
R	R	R/W	R	R/W	R/W	R/W	R/W	

- **ICF**n: Timer/Counter n, input-capture flag (**n** = 1,3,4,5)
  - 0 = No capture event occurred on the ICPn pin.
  - 1 = A capture event has occurred on the ICPn pin.
- **OCF**n**C**: Timer/Counter n output compare C match flag
  - 0 = TCNTn has not matched the OCRnC register since this flag was last cleared.
  - 1 = TCNTn has matched the OCRnC register.
- **OCF**n**B**: Timer/Counter n output compare B match flag
  - 0 = TCNTn has not matched the OCRnB register since this flag was last cleared.
  - 1 = TCNTn has matched the OCRnB register.
- **OCF**n**A**: Timer/Counter n output compare A match flag
  - 0 = TCNTn has not matched the OCRnA register since this flag was last cleared.
  - 1 = TCNTn has matched the OCRnA register.
- **TOV**n: Timer/Counter n, overflow interrupt flag
  - 0 = TCNTn has not overflowed since this flag was last cleared.
  - 1 = TCNTn has overflowed.

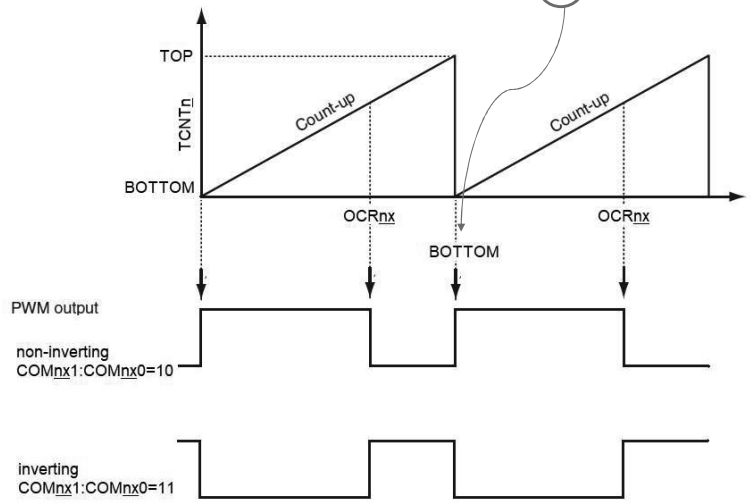
16-bit: TIMSK1,3,4,5

7	6	5	4	3	2	1	0	
—	—	ICIEn	—	OCIEnC	OCIEnB	OCEnA	TOIEn	Reset val = 0x00
R	R	R/W	R	R/W	R/W	R/W	R/W	

- **ICIE<u>n</u>**: Timer/Counter n, input-capture interrupt enable (<u>n</u> = 1,3,4,5)
  - 0 = Disable Timer/Counter n input-capture interrupt
  - 1 = Enable Timer/Counter n input-capture interrupt
- **OCIE<u>n</u>C**: Timer/Counter n output compare C match interrupt enable
  - 0 = Disable Timer/Counter n output compare C match interrupt
  - 1 = Enable Timer/Counter n output compare C match interrupt
- **OCIE<u>n</u>B**: Timer/Counter n output compare B match interrupt enable
  - 0 = Disable Timer/Counter n output compare B match interrupt
  - 1 = Enable Timer/Counter n output compare B match interrupt
- **OCIE<u>n</u>A**: Timer/Counter n output compare A match interrupt enable
  - 0 = Disable Timer/Counter n output compare A match interrupt
  - 1 = Enable Timer/Counter n output compare A match interrupt
- **TOIE<u>n</u>**: Timer/Counter n, overflow interrupt enable
  - 0 = Disable Timer/Counter n overflow interrupt
  - 1 = Enable Timer/Counter n overflow interrupt

Fast PWM: Single Slope

$$f_{fastPWM} = \frac{f_{CLK}}{prescaler * (TOP + 1)}$$



Fast PWM

- TCNT<u>n</u> counts BOTTOM to TOP, repeats
  - Output: OC<u>n</u>A, OC<u>n</u>B, OC<u>n</u>C
- 8-bit fast PWM: Timer <u>n</u>: <u>n</u>=0,2
  - BOTTOM: 0
  - TOP: 0xFF, OCR<u>n</u>A
- 16-bit fast PWM: Timer <u>n</u>: <u>n</u>=1,3,4,5
  - BOTTOM: 0
  - TOP: 0x00FF, 0x01FF, 0x3FF, ICR<u>n</u>, OCR<u>n</u>A
- Can't use OC<u>n</u>A when TOP=OCR<u>n</u>A
- Can't use IC<u>n</u> when TOP=ICR<u>n</u>

Interrupt.h: ISR Symbolic Name

Interrupt source	Vector no.	ISR name	Interrupt source	Vector no.	ISR name
INT0	2	(INT0_vect)	ADC	30	(ADC_vect)
INT1	3	(INT1_vect)	EE READY	31	(EE_READY_vect)
INT2	4	(INT2_vect)	TIMER3 CAPT	32	(TIMER3_CAPT_vect)
INT3	5	(INT3_vect)	TIMER3 COMPA	33	(TIMER3_COMPA_vect)
INT4	6	(INT4_vect)	TIMER3 COMPB	34	(TIMER3_COMPB_vect)
INT5	7	(INT5_vect)	TIMER3 COMPC	35	(TIMER3_COMPC_vect)
INT6	8	(INT6_vect)	TIMER3 OVF	36	(TIMER3_OVF_vect)
INT7	9	(INT7_vect)	USART1 RX	37	(USART1_RX_vect)
PCINT0	10	(PCINT0_vect)	USART1 UDRE	38	(USART1_UDRE_vect)
PCINT1	11	(PCINT1_vect)	USART1 TX	39	(USART1_TX_vect)
PCINT2	12	(PCINT2_vect)	TWI	40	(TWI_vect)
WDT	13	(WDT_vect)	SPM READY	41	(SPM_READY_vect)
TIMER2 COMPA	14	(TIMER2_COMPA_vect)	TIMER4 CAPT	42	(TIMER4_CAPT_vect)
TIMER2 COMPB	15	(TIMER2_COMPB_vect)	TIMER4 COMPA	43	(TIMER4_COMPA_vect)
TIMER2 OVF	16	(TIMER2_OVF_vect)	TIMER4 COMPB	44	(TIMER4_COMPB_vect)
TIMER1 CAPT	17	(TIMER1_CAPT_vect)	TIMER4 COMPC	45	(TIMER4_COMPC_vect)
TIMER1 COMPA	18	(TIMER1_COMPA_vect)	TIMER4 OVF	46	(TIMER4_OVF_vect)
TIMER1 COMPB	19	(TIMER1_COMPB_vect)	TIMER5 CAPT	47	(TIMER5_CAPT_vect)
TIMER1 COMPC	20	(TIMER1_COMPC_vect)	TIMER5 COMPA	48	(TIMER5_COMPA_vect)
TIMER1 OVF	21	(TIMER1_OVF_vect)	TIMER5 COMPB	49	(TIMER5_COMPB_vect)
TIMER0 COMPA	22	(TIMER0_COMPA_vect)	TIMER5 COMPC	50	(TIMER5_COMPC_vect)
TIMER0 COMPB	23	(TIMER0_COMPB_vect)	TIMER5 OVF	51	(TIMER5_OVF_vect)
TIMER0 OVF	24	(TIMER0_OVF_vect)	USART2 RX	52	(USART2_RX_vect)
SPI STC	25	(SPI_STC_vect)	USART2 UDRE	53	(USART2_UDRE_vect)
USART0 RX	26	(USART0_RX_vect)	USART2 TX	54	(USART2_TX_vect)
USART0 UDRE	27	(USART0_UDRE_vect)	USART3 RX	55	(USART3_RX_vect)
USART0 TX	28	(USART0_TX_vect)	USART3 UDRE	56	(USART3_UDRE_vect)
ANALOG COMP	29	(ANALOG_COMP_vect)	USART3 TX	57	(USART3_TX_vect)