Automatic *Voltage Regulator* (AVR) System Compensation of Synchronous Generators Using Bode Plot Analysis

Nahiza Hazim Valensi Miriandran
Electrical Power Engineering
Bandung Institute of Technology
Bandung, West Java, Indonesia
18023021@std.stei.itb.ac.id

Adhindamuthia Ramadhiani
Electrical Power Engineering
Bandung Institute of Technology
Bandung, West Java, Indonesia
18023023@std.stei.itb.ac.id

Gabriella Surjana
Electrical Power Engineering
Bandung Institute of Technology
Bandung, West Java, Indonesia
18023043@std.stei.itb.ac.id

***Abstract*—An Automatic Voltage Regulator (AVR) is a control system to control the output voltage of a generator to remain stable by regulating excitation. However, achieving voltage stability is not enough to guarantee optimal control system performance. A reliable control system must meet the appropriate performance specifications and within the limits. The analysis was then carried out on the AVR system to test the performance of the system using step response, bode plot, root locus, and nyquist plot. The results of the analysis are then used to determine the compensation needs. In addition, a diskritisation process is carried out to see the characteristics of the discrete time system. Based on the results of the analysis, the AVR system without compensation showed a fairly poor system performance, especially in overshoot of 65.2%, settling time of 5.5744 seconds, and steady state error of 0.0907. This indicates that the AVR system needs compensation to improve system performance. The compensator used is the Lag-Lead Compensator via bode plot because it uses passive components that are more practical and able to improve system performance well. The results of the AVR system analysis with compensation showed much better system performance with an overshoot of 2.7349%, a settling time of 2.532s, and a steadily lower error of 0.0467 than the system before compensation so that the Lag-Lead Compensator succeeded in improving the system response. Discrete systems have the characteristics of response, time and frequency, close to continuous systems, with small differences appearing in the transient phase at high frequencies due to sampling and ZOH. The system was declared stable with a fairly wide stable sampling time range, namely 0.0010 s⩽Ts⩽ 0.1610 s.**

Keywords—transient response, stability, lag-lead, plot bode, disscription

I. Introduction

In an electric power system, the stability of the output voltage in the generator is an important factor that determines the electrical power produced. Changes in load that occur dynamically can cause fluctuations in the voltage of the generator terminals, if not controlled can reduce the efficiency of the system and damage the electronic equipment. Therefore, a control mechanism is needed that can maintain the voltage of the generator terminals so that it remains at nominal value despite changes in load or disturbances in operating conditions. The voltage controller in the generator is through excitation control using *the Automatic Voltage Regulator* (AVR). The AVR serves as a *feedback control system* that monitors the output voltage of the generator and automatically adjusts the excitation current to keep the terminal voltage stable in such a way that when the load increases, the voltage tends to decrease and the AVR will increase the excitation current. Meanwhile, when the load is reduced, the voltage rises and the AVR will reduce the excitation.

In the control system. AVR is modeled so that it is possible to analyze the stability of *controller* designs such as Root Locus, Bode Plot, and Nyquist Plot, as well as the design of a control system for a system. This major task is aimed at modeling, analyzing, and designing the AVR generator control system in the domains of continuous and discrete time. The analysis is carried out to evaluate the stability of the uncompensated system, then the appropriate controller design is carried out to achieve the desired performance. Next, the system will be analyzed to assess the effect of domain changes on the stability and performance of the system.

II. Literature Study

A. *Systems Modeling*

The system to be reviewed is a generator voltage control system using an Automatic Voltage Regulator (AVR) with *a closed-loop feedback system,* as shown in the following block diagram.

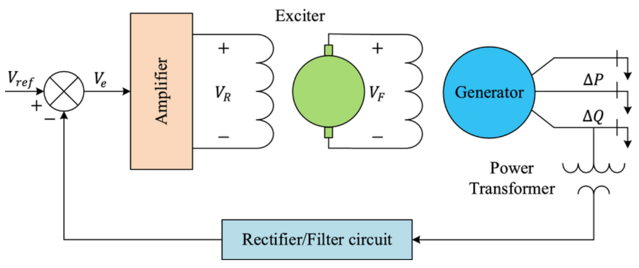

Figure 1 AVR System Modeling on Generators

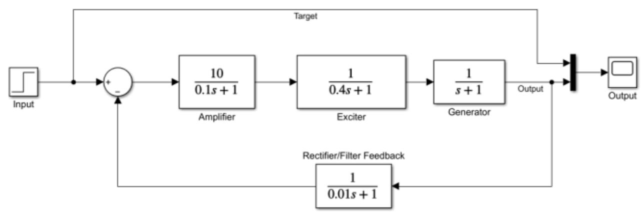

Figure 2 AVR Transfer Function Block Diagram on Generator

The input signal represents the desired reference voltage and then the output voltage will be compared to the reference voltage to produce an error signal. The error signal is processed by the PID controller to correct the error, and it passes through a series of AVR systems consisting of amplifiers, exciters, and generators. The output voltage of the generator will be measured by the sensor and returned as *negative feedback*.

The AVR system seen in Figure 1 consists of several subsystems modeled using a first-order switching function.

1) Amplifier: The amplifier model is represented by the gain with the symbol Ka and the time constant with the symbol τ_a

$$G_A(s) = \frac{k_a}{\tau_a s + 1}$$

The gain (has a value of 10 and a time constant () of 0.1 s.[3]K_a)T_a

2) Exciter: The Transfer function of *the Exciter* can be represented by gain with the symbol To and the time constant with the symbol . Modeling the transfer function becomes:τ_e

$$G_E(s) = \frac{k_e}{\tau_e s + 1}$$

G_eThe gain has a value of 1 and a time constant of 0.4s. [3]

3) Generator: The generator has a transfer function represented by gain with the symbol Kg and the time constant with the symbol . The transfer function can be seen as follows:τ_g

$$G_{gen}(s) = \frac{k_g}{\tau_g s + 1}$$

$K_g \tau_g$The gain has a value of 1 and the time constant () has a value of 1s.[3]

4) Sensor: The sensor has a transfer function represented by gain with the symbol Ks and the time constant with the symbol . Here is the transfer function of the sensor:τ_s

$$G_S(s) = \frac{k_s}{0.01s + 1}$$

τ_sGain Ks has a value of 1 and a time constant of 0.01s. [3]

Based on the four sub-systems of the AVR control system, the transfer of the open loop function (OLTF) is obtained as follows:

$$\mathrm{OLTF}(s) = \frac{k_a\, k_e\, k_g\, k_s}{(T_a s + 1)(T_e s + 1)(T_g s + 1)(T_s s + 1)}$$

$$OLTF(s) = \frac{K}{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + 1}$$

With coefficients:

$K = k_a k_e k_g k_s$

$a_4 = T_a T_e T_g T_s$

$a_3 = T_a T_e (T_g + T_s) + T_g T_s (T_a + T_e)$

$a_2 = T_a T_e + (T_a + T_e)(T_g + T_s) + T_g T_s$

$a_1 = T_a + T_e + T_g + T_s$

In addition, the transfer of closed loop functions (CLTF) from the system is obtained as follows:

$$\mathrm{CLTF}(s) = \frac{\mathrm{OLTF}(s)}{1 + \mathrm{OLTF}(s)}$$

$$CLTF(s) = \frac{K}{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + (1 + K)}$$

$K = k_a k_e k_g k_s$

$a_4 = T_a T_e T_g T_s$

$a_3 = T_a T_e (T_g + T_s) + T_g T_s (T_a + T_e)$

$a_2 = T_a T_e + (T_a + T_e)(T_g + T_s) + T_g T_s$

$a_1 = T_a + T_e + T_g + T_s$

By entering the gain value and the time constant of each sub-system, the CLTF transfer function equation is obtained as follows:

$$\mathrm{CLTF}(s) = \frac{10}{0.0004s^4 + 0.0454s^3 + 0.555s^2 + 1.51s + 11}$$

B. Compensation Analysis with Bode Plots

The method of analysis and design of a frequency response-based control system is one of the important approaches in control system engineering, especially through the use of Bode diagrams. This approach is used to analyze the stability, transient response, and *steady state error* of a system based on the frequency characteristics of the open-loop switching function. In contrast to the root locus method that works in time domains and complex domains, the frequency response method provides a direct relationship between frequency parameters such as gain margin, phase margin, and bandwidth to the performance of the closed control system.

In general, the relationship between phase margin (PM) and percent overshoot (%OS) comes from a dominant second-order system approach. In a linear system, the increase in phase margin is directly proportional to the increase in the damping ratio (ζ), which directly decreases the overshoot percentage .

$$\phi_M = \tan^{-1}\left(\frac{2\zeta}{\sqrt{-2\zeta^2 + \sqrt{1 + 4\zeta^4}}}\right)$$

III. METHODOLOGY

The general steps of working on this big task are as follows.

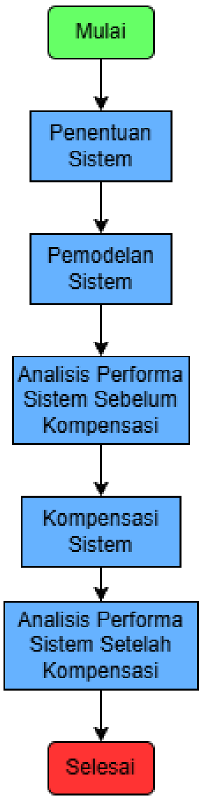

Figure 3 Large Task Workflow

IV. RESULTS ANALYSIS

A. System Performance Before Compensation

The Automatic Voltage Regulator (AVR) control system is used to regulate and stabilize the output voltage of the generator to keep it stable. However, achieving voltage stability is not enough to guarantee optimal system performance. A reliable control system must meet the appropriate performance specifications and within the limits. The following are the results of the analysis of the performance of the AVR system before compensation.

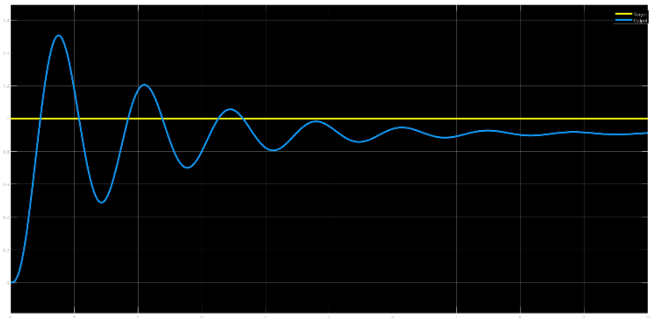

Figure 4 Time Before Compensation Domain Response

Some of the time parameters of the simulation results are shown in the following table.

TABLE I
TIME DOMAIN SIMULATION RESULTS WITH STEP FUNCTION INPUT BEFORE COMPENSATION

Criteria	Value
Peak Time (Tp)	0.75 s
Rise Time (Tr)	0.2613 s
Settling Time (Ts)	5.5744 s
Error Steady State (ess)	0,0907
%Overshoot (%OS)	65,2%

As can be seen in table 1, the system has a rise time of 0.2613 s and a peak time of 0.75 s, which shows that the system is able to respond to input changes relatively quickly. However, a fairly high percentage overshoot value of 65.2%, indicates that the system is underdamped so that there is a significant surge in response before reaching a state of default.

Furthermore, the *settling time* with the 5% criterion has a value of 5.5744 s indicating that although the initial response is fast, it takes a considerable amount of time for the system to actually reach stable conditions within the specified tolerance limits. Overall, the system has been stable but still requires compensation improvements to reduce overshoot and speed up set-up times without sacrificing stability.

In addition to using time domain simulations, analysis of system performance before compensation can be performed through frequency domain simulation. The following are the results of the simulation of the system in the frequency domain using Bode Plot.

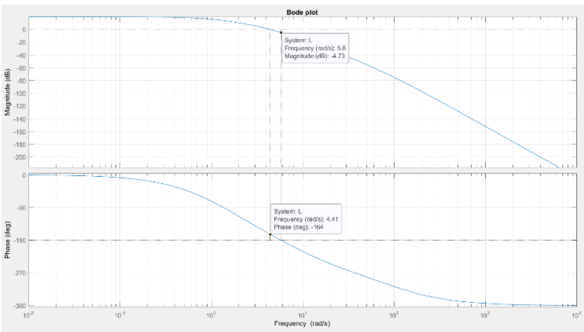

Figure 5 AVR System Frequency Response before Compensation

Some of the parameters of the frequency response simulation can be seen in the following table.

TABLE 2
FREQUENCY DOMAIN SIMULATION RESULTS BEFORE COMPENSATION

Frequency Response	**Value**
Gain Margin (G_m)	4.62 dB
Phase Margin ()ϕ_m	16,103o
Phase Crossover (ω_{G_m})	5,767 rad/s
Gain Crossover (ω_{ϕ_m})	4,403 rad/s

As can be seen in table 2, the system has a *gain margin* of 4.62 dB at a frequency of 5.767 rad/s and a *phase margin* of 16.103° at a frequency of 4.403 rad/s. A gain *margin* value greater than "one" and *a phase margin* of positive value indicate that the system is in a stable condition, but the margin of stability is relatively small. *The low phase margin* indicates that the system is quite sensitive to parameter variations and interference, and has the potential to generate a transient response with a considerable overshoot.

System performance analysis can also be performed using the root locus. The following are the results of the simulation of the location of the close loop pole based on the gain variation in the system using the root locus graph.

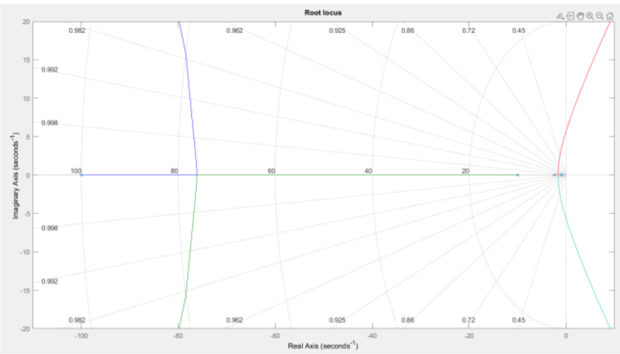

Figure 6 AVR System Root Locus Simulation before Compensation

Based on the root locus plot, the system has four poles on the open-loop transfer function (OLTF) and has no zeros, so the entire root locus trajectory starts at these poles and moves towards zero as gains increase. The absence of zero causes the trajectory of the closed pole to follow the asymptotic determined by the number of poles and the asymptotic angle of the system.

From the observations, the intersection with the imaginary axis (jw-axis crossing) occurs at the gain value, which indicates the stability limit of the system. At this gain value, the system is in a marginally stable condition, with a pure complex pole pair at a natural oscillation frequency of about 5.76 rad/s. In addition, the position of the dominant pole very close to the imaginary axis indicates very small damping. Therefore, although the system can be made stable for a given gain value, increased damping through the addition of a compensator is still required to improve the transient performance of the system.$K = 1{,}7$

Nyquist plots can also be used to analyze system performance. The following is the result of the simulation with the Nyquist graph.

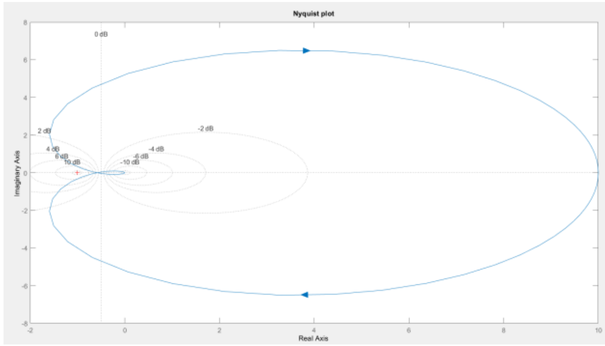

Figure 7 Nyquist Simulation Plot of AVR system before Compensation

Based on the Nyquist diagram, the system's frequency response curve does not surround the critical point $-1 + j0$, so according to Nyquist's stability criteria, the closed system is in a stable state. Nevertheless, the distance of the Nyquist curve to the critical point -1 is relatively small, which reflects a limited margin of stability. This condition is in line with *low margin gain and phase margin* values , as well as time response that indicates a large overshoot. Thus, even if the system meets the stability criteria, it still has a transient response that is not good.

Overall, the AVR system can indeed regulate and restore the voltage back to stability. However, this system still has a transient response that is bad enough to affect the system's performance. Therefore, the AVR system requires improvements made by adding compensators to the system so that the AVR system can work more optimally when overcoming interference.

B. System Compensation with Bode Plot Analysis

Based on the results of system simulations before compensation that have been carried out previously, the performance of the Automatic Voltage Regulator (AVR) system has not met the optimal design specifications. The system response showed poor transient characteristics with *large overshoots*, slow *settling times*, and considerable *steady state errors*. This can be a problem for AVR systems because large *overshoots* signal high voltage spikes that can damage insulation, components, and even cause trips because the protection system considers voltage spikes to be interference. In addition, a slow *settling time* signifies that the voltage reaches stability over a long period of time and can cause synchronous discharge in the generator. *A large enough steady state error* also indicates that the voltage does not match the nominal voltage so that it can cause component damage due to overheating.

To improve the performance response of the system so that the AVR works more optimally, compensation is carried out using the Lag-Lead Compensator based on the analysis of the bode plot. The Lag-Lead Compensator was chosen because it uses a more economical passive component and does not require additional power supply, making it much simpler in terms of the circuit than PID. A simple circuit minimizes the risk of component failure due to high temperatures and eliminates the need for additional operational power, making the Lag-Lead compensator a reliable and economical solution with optimal compensation results.

The lead compensator works to reduce *overshoot* by increasing *the phase margin* of the target and accelerating *the settling time* by shifting the crossover frequency to a higher frequency so that bandwidth is greater and accelerates system response. The lead compensator will cause the magnitude to rise so that the lag compensator is used to decrease the magnitude so that the crossover frequency stays at the desired point without damaging the phase margin.

The target of improvement with the desired compensator is as follows.

TABLE 3
SYSTEM REPAIR TARGET PARAMETERS

Criteria	Value
Peak Time (Tp)	0.6s
Error Steady State (ess)	5%
%Overshoot (%OS)	10%

The desired peak time is smaller than the result before compensation so that *the settling time* is also smaller and the voltage returns in a faster time when a fault occurs so that the system remains stable. The steady *state error* target of less than 5% is adjusted to the voltage range limit of 5% in PM ESDM No. 20 of 2020 (Grid Code). Meanwhile, the $\pm$*overshoot* target is less than 10% where the voltage only jumps small and is still within reasonable limits so it is safe for other components.

The following is the calculation process to obtain the Lag-Lead Compensator with bode plot analysis.

Open loop transfer function

$$KG(s)H(s) = \frac{10K}{(0.1s+1)(0.4s+1)(s+1)(0.01s+1)}$$

Target *error steady state* 5% = 0.05

$$e_{ss} = \frac{1}{1+K_p}$$

$$K_p = 19 \approx 20$$

$$\lim_{s\to 0} G(s) = 20$$

$$K = 2$$

Gain of 2 is obtained to achieve the *steady state error* target. Next, calculations are made to make a lead compensator.

The target overshoot is 10% so that *the damping ratio* is as follows.

$$\zeta = \frac{-\ln\left(\frac{OS}{100}\right)}{\sqrt{\pi^2 + \ln^2\left(\frac{OS}{100}\right)}} = \frac{-\ln\left(\frac{10}{100}\right)}{\sqrt{\pi^2 + \ln^2\left(\frac{10}{100}\right)}} \approx 0.591$$

$$\zeta = \tan^{-1}\left(\frac{2\zeta}{\sqrt{-2\zeta^2 + \sqrt{1+4\zeta^4}}}\right) = 58.58°$$

The target *peak time* is 0.6s so that the bandwidth is obtained as follows.

$$T_p = 0.6s$$

$$\omega_{bw} = \frac{\pi}{T_{p\sqrt{1-\zeta^2}}}\sqrt{(1-2\zeta^2) + \sqrt{4\zeta^4 - 4\zeta^2 + 2}}$$

$$\omega_{bw} = 7.53018\, rad/s$$

For the calculation of the lead compensator, a crossover frequency close to the bandwidth, which is 5 rad/s, is chosen.

$$\omega_{max} = 5\, rad/s$$

At a frequency of 5 rad/s, the following *phase margin* is obtained on the uncompensated plot bode of the system which will be used for the calculation *of the target phase margin*.

$$\emptyset_m = -180° + 171.55° = 8.45°$$

$$\emptyset_{max} = 58.58° - 8.45° + 10° = 60.13°$$

The following is a calculation to obtain the lead compensator equation.

$$\sin(60.13°) = \frac{1-\beta}{1+\beta}$$

$$\beta = 0.0711466$$

$$\omega_{max} = \frac{1}{T\sqrt{\beta}}$$

$$T = 0.749813$$

$$G_{c\,lead}(s) = \frac{1}{\beta}\frac{\left(s+\frac{1}{T}\right)}{\left(s+\frac{1}{\beta T}\right)}$$

$$G_{c\,lead}(s) = 14.0555\frac{(s + 1.3337)}{(s + 18.7453)}$$

The lead compensator causes an increase in magnitude, so a compensator lag is created so that the crossover frequency remains in line with the target. Here is the calculation for lag compensators.

When the frequency is 5 rad/s,

$$|G(j\omega)| = 5.8747$$

$$20\log(5.8747) = 15.38dB$$

The lag compensator should provide an attenuation of -15.38 dB with the compensator equation as follows.

$$z_{lag} = \frac{\omega_{max}}{10} = \frac{5}{10} = 0.5$$

$$p_{lag} = \frac{z_{lag}}{\alpha} = \frac{0.5}{5.8747} = 0.0851$$

$$G_{c\,lag}(s) = \frac{1}{\alpha}\frac{(s + z_{lag})}{(s + p_{lag})}$$

$$G_{c\,lag}(s) = 0.1702\frac{(s + 0.5)}{(s + 0.0851)}$$

$$G_c(s) = \frac{47.8449(s + 1.3337)(s + 0.5)}{(0.1s + 1)(0.4s + 1)(s + 1)(0.01s + 1)(s + 18.7453)(s + 0.0851)}$$

The lag-lead compensator will be used in the AVR system so that it provides more optimal results.

C. System Performance After Compensation

System compensation with Lag-Lead Compensator is expected to improve system performance according to predetermined targets. To measure the effectiveness of the compensation, the following are the results of the performance of the AVR system after compensation is applied.

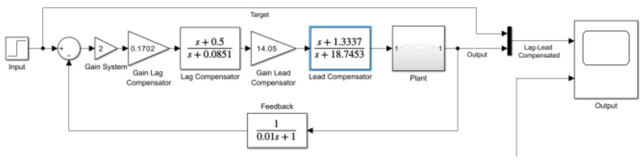

Figure 8 System Block Diagram with Lag-Lead Compensator

System simulation with Lag-Lead Compensator was carried out on SIMULINK so that *the following step response* results were obtained.

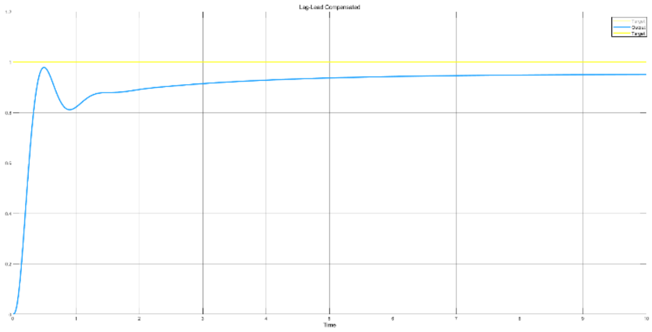

Figure 9 Step System Response with Lag-Lead Compensator

Based on the results of the system response step with the compensator, the following is the response data obtained.

TABLE 4
STEP RESPONSE RESULTS AFTER COMPENSATOR

Criteria	Value
Peak Time (Tp)	0.4983s
Rise Time (Tr)	0.256s
Settling Time (Ts)	2,532s
Error Steady State (ess)	0,0476
%Overshoot (%OS)	2,7349%

Based on the data from the step response, the system with the Lag-Lead Compensator shows a fast response shown by *peak time*, *rise time*, and *settling time*. This indicates that AVR causes the system to stabilize faster when there is a fault or voltage drop. In addition, although the system has a fast response, but the stability of the system is maintained which is indicated by a *very small overshoot of 2.7349%.* A small *overshoot* indicates that the voltage surge is still within safe limits so that it will not damage other components due to overvoltage. *The steady state error* shows a fairly small figure of 4.76% where the system voltage is still within the safe limit of voltage.

The results of the AVR system with Lag-Lead Compensator show that the compensator design is successful because the performance of the system that matches the target is even better than the desired target. The performance improvements are very clearly seen in *the settling time*, *overshoot*, and *steady state errors*, which indicates that the addition of a Lag-Lead Compensator is very effective in improving the system's ability to dampen oscillations and accelerate voltage recovery to *steady state conditions*.

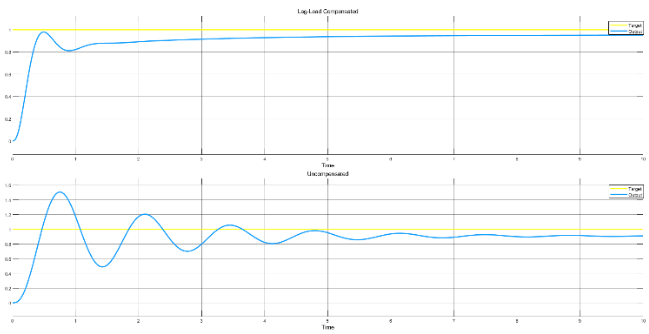

Figure 10 Comparison of Uncompensated System and Compensated System Response Steps

Based on figure 10, it can be seen that systems with compensators show better results than before compensation. This is shown by the decrease in *overshoot* in the system with compensation. In an uncompensated system, the response jumps to quite a bit above the target, while the compensated system experiences a much smaller spike. In addition, the uncompensated system experiences oscillations that last quite a long time when compared to the compensated system response that goes directly to the target value indicating that there is a much shorter *settling time*. In *the steady state* condition, the compensated system has a value that is closer to the target so that it has a smaller *steady state error* value . Overall, the simulation results show that the design of the Lag-Lead Compensator works effectively according to its function to improve transient response and *steady state errors* so that the AVR system works more optimally when overcoming voltage disturbances.

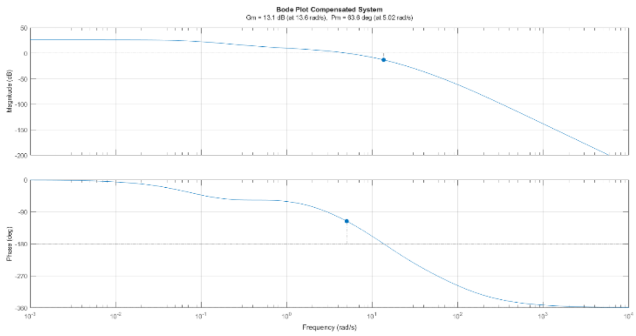

Figure 11 Bode Plot System with Compensation

The following are the results of the frequency domain simulation on the system with the Lag-Lead Compensator.

TABLE 5
FREQUENCY DOMAIN SIMULATION RESULTS AFTER COMPENSATION

Frequency Response	Value
Gain Margin (G_m)	13.1 dB
Phase Margin ()ϕ_m	63,6°
Phase Crossover (ω_{G_m})	13,6 rad/s
Gain Crossover (ω_{ϕ_m})	5,02 rad/s

Based on the results of the frequency response simulation, *the phase margin* and *gain margin* have positive values which indicates that the system is stable. The phase margin is valued at 63.6 in accordance with the desired °*phase margin* target in the compensator design of 60.13. This causes the °*target overshoot* to be below 10%. In addition, a considerable margin gain of 13.1 dB indicates that the system has greater tolerance for unexpected system changes in the real world or can remain stable within a given range of changes. The shape of the bode plot that decreases and then increases slightly indicates that there is a lag compensator that decreases the magnitude and a lead compensator that increases *the phase margin* so that the transient response becomes better.

When compared to the simulation results on the system without compensation, *the phase margin* and *gain margin* of the system with the Lag-Lead Compensator were larger. This increase *in phase margin* and *gain margin* indicates that the compensated system is able to minimize *overshoot* and oscillation and has a high tolerance for the uncertainty of system parameters. The different shape of the plot bode also indicates that the compensator is working to improve the system according to the desired target. Overall, this comparison of bode plots shows that a system with compensation is more stable than without compensation.

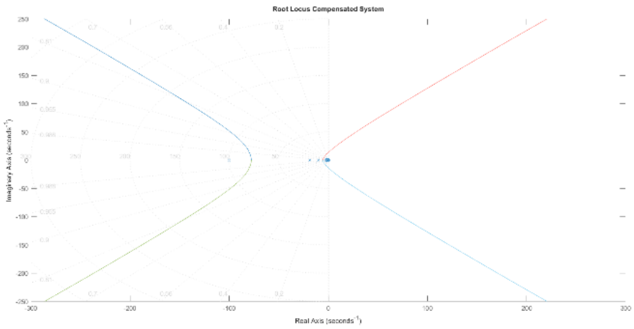

Figure 12 Root Locus System with Compensation

Based on figure 12, all *zeros* and *poles* are on the left side of the s-plane which indicates that the system is stable. The root locus of the compensated system shifted more to the left than it did initially. The location of the dominant pole has also changed so that it produces an optimal damping ratio to minimize oscillations and *overshoots* according to the desired target. Changes in the root locus graph that shifted to the left after compensation indicate a change due to the presence of a compensator. Before compensation, *the poles* tend to be parallel to the imaginary axis and are near the stability limit.which indicates that the system has a slow response as well as a small margin of stability. Meanwhile, after compensation, the addition of *zeros* and *poles* to the controller successfully shifts the root locus graph further to the left indicating that the compensated system has a faster response and a greater margin of stability. Overall, the compensated system showed better results at the root locus just as before.

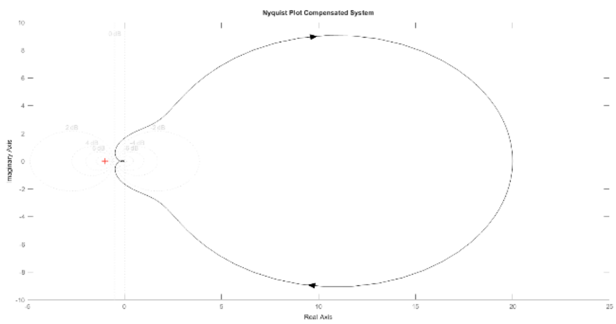

Figure 13 Nyquist Plots Systems with Compensation

Based on figure 13, the nyquist curve of the system plot after compensation does not cover the critical point (-1, j0). According to the stability criteria in nyquist, this indicates that the system is stable. The uncompensated system also shows stable results on the nyquist plot, but there is a difference in the fact that the compensated system has a curve loop that magnifies towards the positive real axis. This is caused by the increase in DC gain by the lag compensator so that the steady state error is small. In addition, when compared to a system without compensation, nyquist plots of a system with compensation are more avoidant of the left or location of the critical point (-1, j0) which indicates that the stability margin of the system is larger so that it is not easy to oscillate. Overall, just like the previous analysis, the compensated system showed better results on nyquist plots.

Overall, AVR systems with Lag-Lead Compensator show much better performance than pre-compensated systems. This is shown by a much better transient response than before. With the compensation done, the AVR system can work better in controlling the voltage so that

D. System Description

System dissection is carried out to see the influence of the AVR system in the discrete domain, because continuous signals need to be processed by digital computers that work discretely. Therefore, modeling is carried out on discrete models to see its effect on stability, system performance, and as a comparison with the continuous domain. The diskritisation process is carried out using *the zero-order hold* (ZOH) method, where the value of the sampling signal is held constant for one sampling period (Ts) before the signal is updated again. The ZOH model is generated from *a staircase approximation* to a continuous signal and is mathematically represented by the following switching function,

$$G_h(s) = \frac{1 - e^{-T_s s}}{s}$$

which is used in the discrete mobile function decrease of the system. The discrete switching function is obtained using MATLAB software. The continuous model of *the plant, controller*, and sensor was analyzed using the ZOH method using *sampling time* Ts=0.01 s, resulting in the following equation.

$$G_{plant}(z) = \frac{0.00004029z^2 + 0.0001558\,z + 0.00003766}{z^3 - 2.87z^2 + 2.744z - 0.8737}$$

$$G_c(z) = \frac{4.784z^2 - 9.489z + 4.704}{z^2 - 1.828z + 0.8284}$$

$$H(z) = \frac{0.6321}{z - 0.3679}$$

Furthermore, a step response simulation was carried out to compare the performance of the AVR system in the domains of continuous and discrete time.

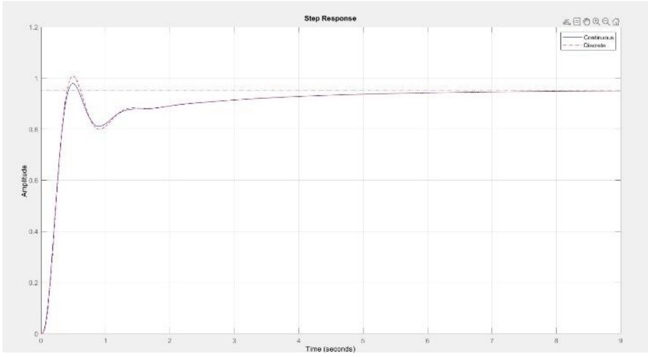

Figure 14 Step Response on the Domains of Continuous and Discrete Time.

With a relatively small *sampling time*, discrete signals are able to describe a continuous system with minimal differences. When the sampling interval is close enough, the approximation becomes closer to a continuous signal, so the difference in response becomes very small. There is a small difference in the initial transient, around the peak of the response, where the discrete system shows a slightly larger overshoot than the continuous system. This is due to the retention of signals in the sampling process using the ZOH method.

The performance of discrete systems shows a response quite similar to that of continuous systems, as seen in the following table.

TABLE 6
FEATURES OF STEP-RESPONSE DISCRETE SYSTEM

Criteria	Value
Peak Time (Tp)	0,49 s
Rise Time (Tr)	0,25 s
Settling Time (Ts)	2.51 s
Error Steady State (ess)	0,0476
%Overshoot (%OS)	5,7 %

Values that do not experience this difference too far indicate that the dyskritisation process does not significantly change the speed of the system's response. For example, the *settling time* of the discrete system of 2.51 s is very close to the value of the settling time of the continuous system of .532 s which indicates that the rate of response to the state of tune, is almost similar in both systems. The obvious difference is that in the *overshoot*, in the continuous system, *the overshoot* is obtained by 2.73% while in the discrete system the greater value is seen at 5.7%. This increase can occur due to the *effect* of sampling and signal retention by *zero-order hold* (ZOH). However, this value is still within the initial system design target limit of <10%.

In addition, the stability of the discrete system is no longer determined by the position of the pole in the *left-half plane* as in the continuous system, but by the position of the *closed loop* pole *of the system in the z<-plane.* Due to the pole mapping relationship from the continuous domain to the discrete domain through the equation. $z = e^{sT_s}$

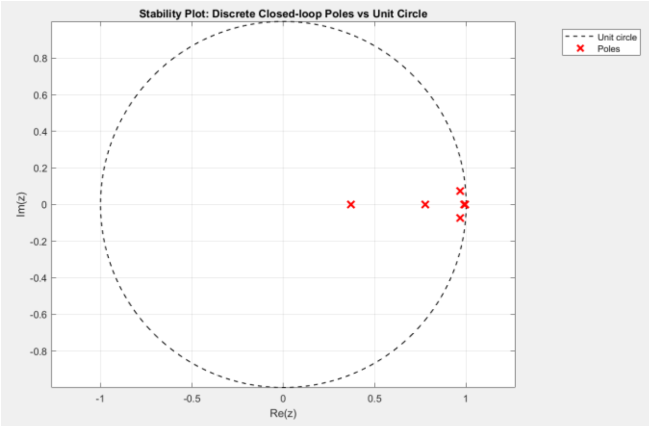

Figure 15 Discrete Pole Stability Plot in Unit Circle

Through calculations using MATLAB, the discrete system of the AVR will be stable over the *sampling time range* $0{,}0010\ s \leq Ts \leq 0{,}1610\ s$. In addition, through simulations, the pole locations were also obtained at 0.9675±0.0730i, 0.9888, 0.9955, 0.7771, and 0.3699. In the image above, the location *of the closed loop pole* system has been mapped with *sampling time* Ts=0.01 s and is entirely in a *circle unit,* which indicates that the discrete system is in a stable condition and supports the range of sampling time results needed for the system to be stable.

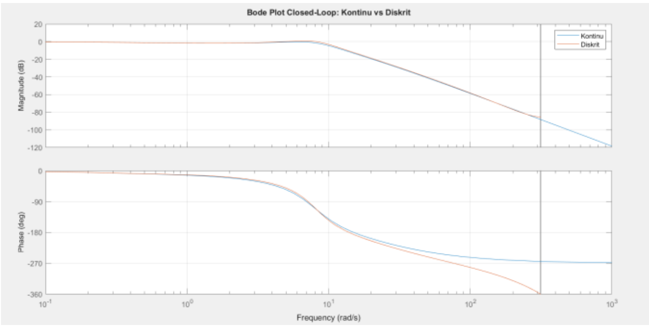

Figure 16 Bode Plots of Continuous and Discrete Systems

In the comparison of the bode plots above, it can be seen that the two are almost similar in the range of low to medium frequencies, meaning that the dyskritisation process maintains the characteristics of the closed loop gain at its working frequency. Signal components at low frequencies, discrete models show continuous systems fairly accurately, so that they are consistent with the step response results with minimal differences. However, as the frequency increases, the magnitude of both systems decreases (attenuation increases), meaning that the closed loop system acts as a *low pass* and is able to effectively dampen the high-frequency components.

Quite a difference can be seen in phase plots, discrete curves show phases that lag compared to continuous curves at medium to high frequencies. This difference is an effect of sampling and ZOH, which adds *phase lag* to the discrete system. At the low-medium frequency the two curves are still very similar, the effect of dykritisation does not change the characteristics of the system on the frequency of the working operation.

V. Conclusion

After modeling and analysis of the control system on the Automatic Voltage Regulator (AVR) in the continuous and discrete domains, it is found that the system without compensation has poor transient performance, seen in high *overshoot*, long *settling time*, and small stability margin. Through frequency domain analysis, the system remains stable but sensitive to interference. As an improvement, a lag-lead compensator is designed through bode plot analysis. The simulation results show that the compensator can increase *the phase margin* and *gain margin*, so that the transient response of the system improves. After compensation, *the system overshoot* decreased to 2.7349%, the system's *settling time* was shorter, and the *steady state error* met the design target. A comparison of the response before and after compensation showed that the addition of *lag-lead compensators* was effective in improving system attenuation and increasing stability margins.

Furthermore, the *compensated* AVR system was analyzed using *the zero-order hold* (ZOH) method with *sampling time* Ts = 0.01 s. The results showed that the discrete system had response characteristics, time and frequency, close to a continuous system, with small differences that appeared in the transient phase at high frequencies due to *sampling* and ZOH. Through stability analysis in the discrete domain, the entire *closed loop pole* is located inside the *circle unit*, so the system is declared stable. In addition, it was obtained that the sampling time range was stable quite wide, namely . Overall, the design of $0{,}0010\ s \leq Ts \leq 0{,}1610\ s$ *lag-lead compensators* based on bode plot analysis has succeeded in improving the performance of the AVR system, both in the domains of continuous and discrete time.

References

[1] A. R. Ibrahima, N. Basila, and M. I. Mahdib, “Implementation enhancement of AVR control sistem within optimization techniques,” *International Journal of Nonlinear Analysis and Applications*, vol. 12, no. 2, pp. 2021–2027, 2021, doi: 10.22075/ijnaa.2021.5339.

[2] N. S. Nise, Control systems engineering. New York: John Wiley & Sons, 2004.

[3] Y. R. Mohammed, N. Basil, O. Bayat, and A. H. Mohammed, “A new novel optimization techniques implemented on the AVR control sistem using MATLAB-SIMULINK,” Electrical and Electronic Engineering, vol. 2, no. 4, pp. 199–207, 2012, doi: 10.5923/j.eee.20120204.05.

[4] H. Shayeghi and J. Dadashpour, “Anarchic society optimization based PID control of an automatic voltage regulator (AVR) sistem,” Electrical and Electronic Engineering, vol. 2, no. 4, pp. 199–207, 2012, doi: 10.5923/j.eee.20120204.05.

[5] E. Köse, “Optimal control of AVR sistem with tree seed algorithm-based PID controller,” IEEE Access, vol. 8, 2020, doi: 10.1109/ACCESS.2020.2993628.