EXAM

1TE717 Digital Technologies and Electronics
Faculty of Electrical Engineering

2020–10–22, 14:00–19:00

Take-home Exam - Studium

Aids:

- Mathematics and / or Physics handbook,
- a small graphical calculator (e.g. TI-83 and similar),
- one A4 paper (two sides) with handwritten formulas or notes.

Note that exercise materials (exercise tasks, old exams, and solutions) are **NOT** allowed.

Observe: Do not treat more than one problem on each page.
Each step in your solutions must be motivated.
Lacking motivation will results in point deductions.
Write a clear answer to each question and clearly indicate which formulas are used.
Mark the total number of pages on the cover or first page

The exam consists of Part A and Part B, for a total of 50 points. The points for each problem are also indicated.

Passing Grade: To pass the course, you need to successfully attain the learning goals of the course. This means that you would pass the exam if you obtain **at least 50%** of the points at **each question of part A**.

Part A has a total of 5 questions.

Exam Grade: Passing the exam would grant the grade 3. Grades 4 and 5 are obtained based on the **total score** obtained in the exam (Parts A and B).

Responsible: André Teixeira (see Studium for contact information)

Good Luck!

Part A

A.1

Consider the network in Fig. 1, where $R_1 = R_2 = R_3 = 40\,\Omega$, $R_4 = R_5 = 20\,\Omega$, $V_1 = 6\,V$ and $V_2 = 3\,V$. Determine the current passing through R_3 (magnitude and direction).

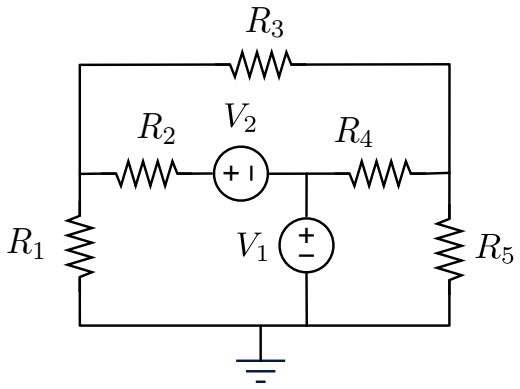

Figure 1: Circuit for Question A.1.

(Sub-Total A.1: 5 pt)

A.2

Consider the amplifier circuit in Fig. 2, where $R_1 = 200\,\Omega$, $R_2 = 400\,\Omega$, $R_3 = 100\,\Omega$, $V_r = 1V$, and $V_{in} = 5V$.
Assume that the OpAmp is ideal and that the supply voltages are sufficiently large. **Using Ohm's and Kirchoff's laws** (possibly through the Nodal or Mesh method), **derive the expression** for the output voltage V_o as a function of V_{in} and V_r and determine the current passing through R_3 (magnitude and direction).
Note: merely identifying and writing down the correct formula, without including the supporting derivations based on circuit analysis, will give no points.

(Sub-Total A.2: 5 pt)

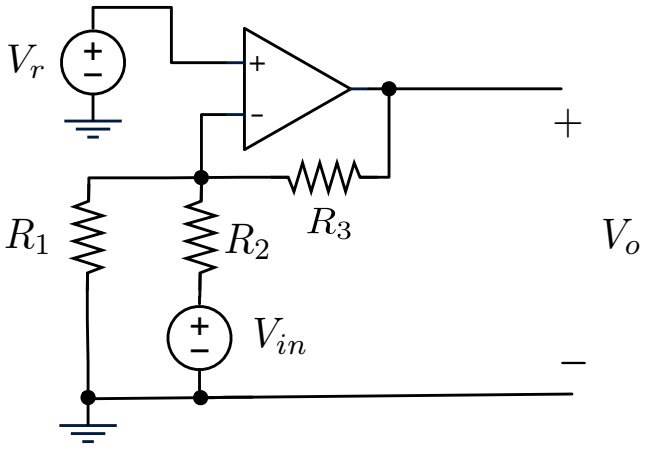

Figure 2: Circuit for Question A.2.

A.3

Consider the circuit in Fig. 3, where the bipolar transistor has the following characteristics: $\beta = h_{FE} = 300$, $V_{CE_{sat}} = 0.2\,V$, and $V_{BE} = 0.6\,V$. Suppose that $V_s = 12\,V$, and $V_{in} = 5\,V$. The diode shown in the circuit is an LED with $V_D = 1.5V$ and internal resistance $R_D = 20\Omega$.

Design R and R_B so that the BJT works as a switch, no more than 20 mA pass through the LED, and the current provided by the voltage source V_{in} is smaller than 1 mA.

(Sub-Total A.3: 5pt)

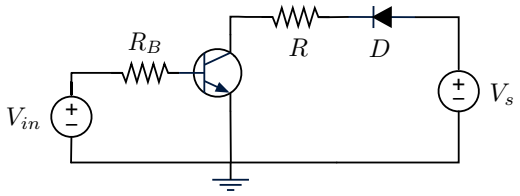

Figure 3: Circuit for Question A.3.

A.4

This question is about designing a sequential machine that detects a given sequence within a stream of bits x_i. The circuit normally gives $y = 0$ as the output, until the sequence 0110 is detected. Every time that the sequence is detected, the output y should be set to 1 for one clock cycle, and then return to zero when a new input bit x_i is read and continue to detect possible sequences (i.e., **possibly with overlapping** a previous sequence).

A.4.a) Perform the first steps of the design of the sequential network: i) derive the state-diagram, ii) choose the state-coding, and iii) write the truth tables determining the behavior of the sequential network and its outputs.

Given your design choice, indicate whether it is a Mealy or Moore type, and how many D flip-flops would be needed to implement your circuit. Motivate your answer!

*Note: you need **not** derive the minimal SP-form Boolean expressions, nor to draw the final circuit diagrams with gates and flip-flops.*

A.4.b) Suppose that one of the D flip-flops as the following Boolean function for determining its next state:

$$q_0^+ = f(\,q_2,\, q_1,\, q_0,\, x_i) = \Sigma(2,\, 3,\, 4,\, 10,\, 12) + d(0,\, 6,\, 11).$$

Design a combinatorial network that implements the logical function f in minimal SP-form using only NAND gates. Draw the logical circuit with the corresponding D flip-flop.

(Sub-Total A.4: 5pt)

A.5

Consider the filter in Fig. 4. Suppose that $V_{in}(t)$ is a sinusoidal voltage signal with $v_{in}(t) = 2\sin(100000\pi t - \frac{\pi}{3})$. Using the methods of AC circuit analysis and complex impedances, derive the expression of the output voltage signal $v_{out}(t)$ for $R_1 = R_2 = 50\,\Omega$, $C = 0.1\,\mu F$, and $L = 1\,mH$, and classify this circuit as either a low-pass, high-pass, band-pass, or a band-stop filter.

(Sub-Total A.5: 5pt)

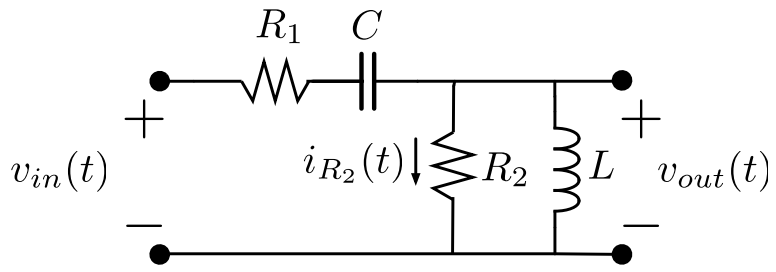

Figure 4: Circuit for Question A.5.

Part B

B.1

Consider the amplifier circuit in Fig. 5, where D_1 has $V_d = 0.5\,V$, and $V_{out}(t)$ is the voltage measured across the terminals of the capacitor. Let $V_{in}(t)$ be a sinusoidal voltage with amplitude $V_p = 6\,V$. Describe the behavior of the circuit, motivated by the operation of its components, and sketch the shape of the output voltage. Supposing that the OpAmp is supplied with +15V and -15V, what is the maximum reverse voltage that the diode must be able to withstand?

(Sub-Total B.1: 8pt)

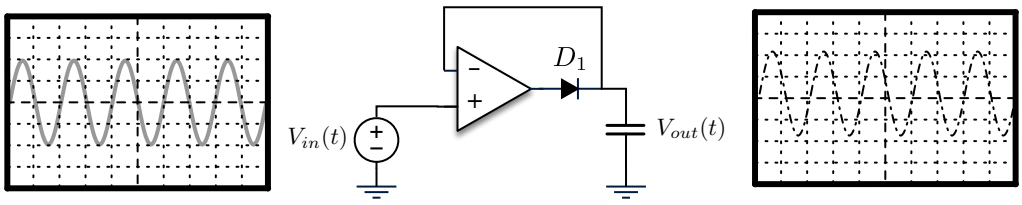

Figure 5: Circuit for Question B.1.b).

B.2

Consider the AC amplifier circuit in Fig. 6, where $R_1 = R_2 = 10\,k\Omega$, $C_1 = 2C_2$, and $C_2 = 10\,nF$. Assume that the OpAmp is ideal and that the supply voltages are sufficiently large. **Using AC circuit analysis**, **derive the transfer function** of the circuit. Based on the transfer function, determine the gain at $w = 14000\,\text{rad/s}$, and state whether the circuit is a low-pass, high-pass, band-pass, or band-stop filter.
Note: merely identifying and writing down the correct formula, without including the supporting derivations based on circuit analysis, will give no points.

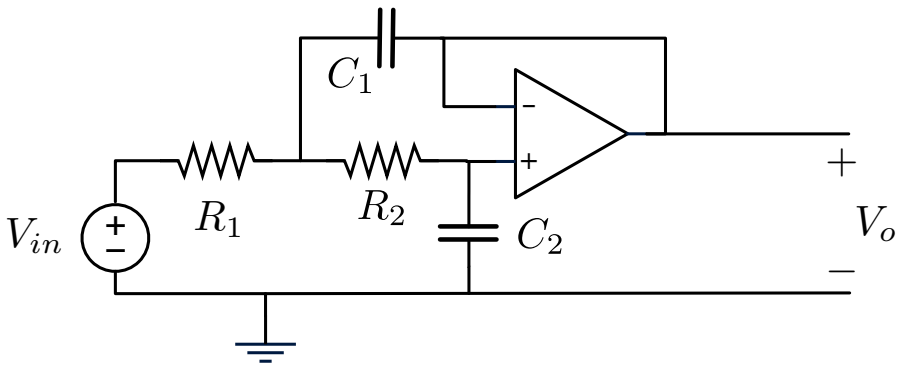

Figure 6: Circuit for Question A.3.b).

(Sub-Total B.2: 9pt)

B.3

In this question, you are asked to design a generator of a given sequence of two bits, (x_1, x_2). The desired sequence is composed of binary numbers, in the following order: $(0, 0)$, $(1, 1)$,

$(0,1)$, $(1,0)$, $(0,0)$, $(1,1)$, ... (the sequence repeats itself) ...

The circuit shall be designed based on 1 D flip-flop and a 4-bit counter. The counter has the output (z_3, z_2, z_1, z_0) corresponding to the current number is the counter. It also has an enable bit E and an asynchronous reset bit R. When $E = 1$, the counter continues to count in the positive direction . When $E = 0$, the counter freezes its operation. When R is set to 1, the counter immediately sets its current number to 0 and resumes counting from that number when $E = 1$.
The 4-bit output of the counter is translated onto the respective elements of the sequence.
The purpose of the D flip-flop is to control the operation of the counter.

Design the behavior of the D flip-flop, by drawing the state diagram of a sequential network that controls the counter as desired. Given your design choice, indicate whether it is a Mealy or Moore type.
Briefly describe how the 4-bit output of the counter could be translated onto the elements of the sequence. Motivate your answer (e.g., by using a truth table)!
(***Note**: Karnaugh diagrams are not needed for this answer.*)

(Sub-Total B.3: 8pt)