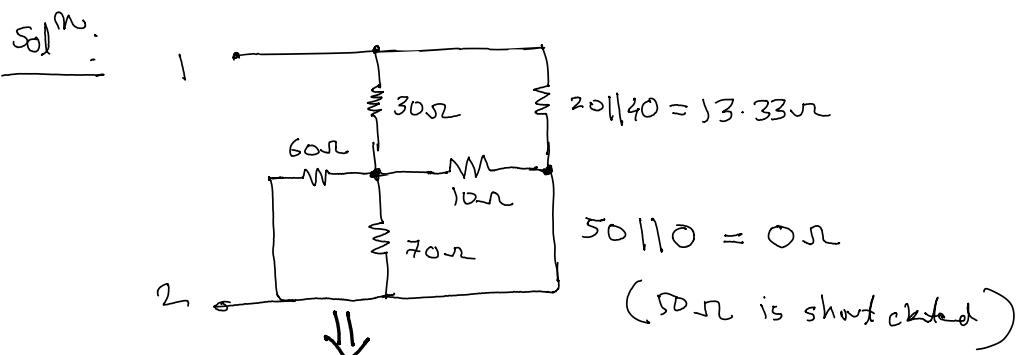
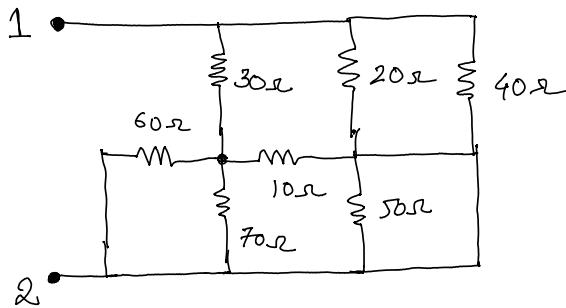
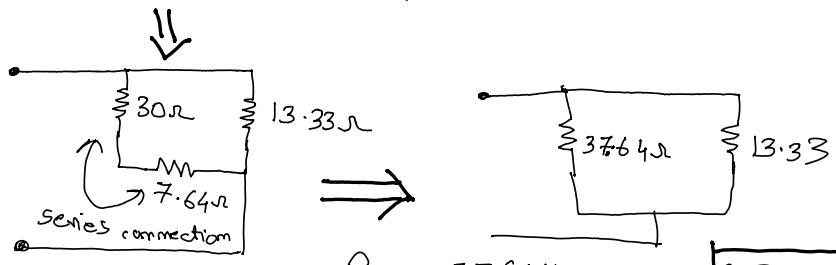


① Find the total resistance between 1 & 2  
as shown in figure

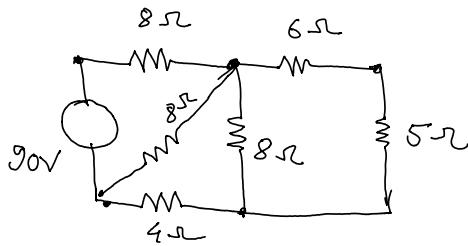


$$10\Omega \parallel 70\Omega \parallel 60\Omega = 7.64\Omega$$

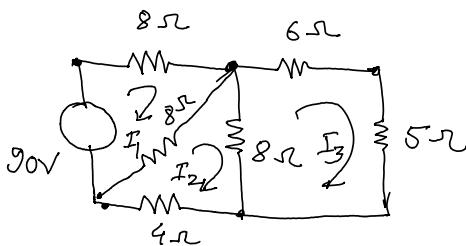


$$\therefore R_{12} = 37.64 \parallel 13.33 = 9.844\Omega$$

1. b. Find the current flowing through the  $5\Omega$  resistor.



Sol<sup>n</sup>



Mesh eq<sup>n</sup>

$$90 - 8I_1 - 8(I_1 - I_2) = 0 \quad \dots \textcircled{1}$$

$$4I_2 + 8(I_2 - I_1) + 8(I_2 - I_3) = 0 \quad \dots \textcircled{2}$$

$$6I_3 + 5I_3 + 8(I_3 - I_2) = 0 \quad \dots \textcircled{3}$$

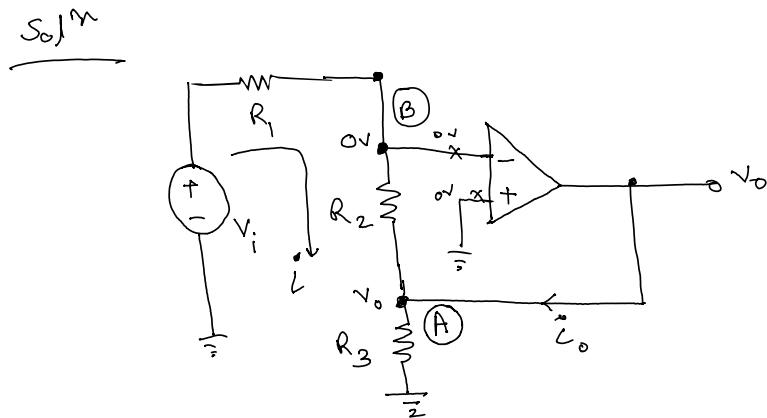
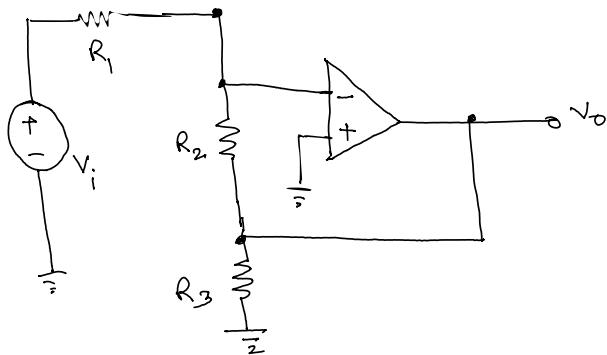
simplify  $\rightarrow 8I_1 - 9I_2 = 45$

$$-2I_1 + 5I_2 - 2I_3 = 0$$

$$-8I_2 + 19I_3 = 0$$

$$\Rightarrow I_3 = 1.5 A$$

2. a. Assuming the op-Amp is ideal, the voltage gain of the amplifier shown below is,



Applying KVL,

$$V_i - R_1 i = 0, \Rightarrow i = \frac{V_i}{R_1} \quad \textcircled{1}$$

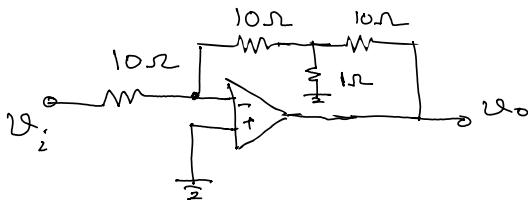
For the path (B)  $\rightarrow$  (A)  $\rightarrow$  ground,

$$i = \frac{0 - V_o}{R_2} \quad \textcircled{2}$$

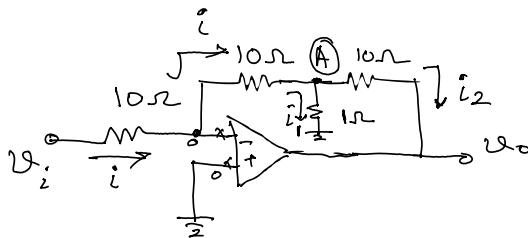
Applying ① in ②,  $\frac{V_i}{R_1} = -\frac{V_o}{R_2}$ ,

$$\boxed{\frac{V_o}{V_i} = -\frac{R_2}{R_1}}$$

2.b Assuming that the op-amps in the circuit is ideal, then the  $\frac{V_o}{V_i} = ?$



Sol<sup>m</sup>



$$i = \frac{V_i - 0}{10} = \frac{0 - V_A}{10} \quad \dots \textcircled{1}$$

At node A, say the potential is  $V_A$

$$\therefore \frac{V_A}{1} + \frac{V_A - V_o}{10} = \frac{0 - V_A}{10}$$

$$\Rightarrow 10V_A + V_A - V_o = -V_A$$

$$\Rightarrow 12V_A = +V_o$$

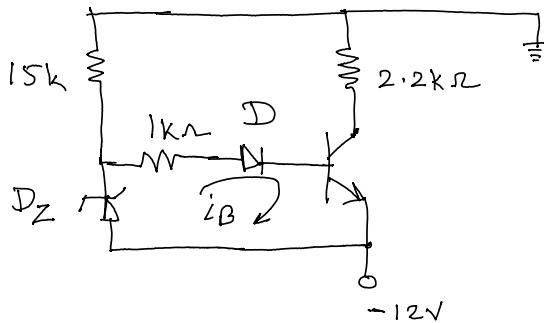
$$\Rightarrow V_A = +\frac{1}{12}V_o \quad \dots \textcircled{2}$$

using  $\textcircled{2}$  in  $\textcircled{1}$

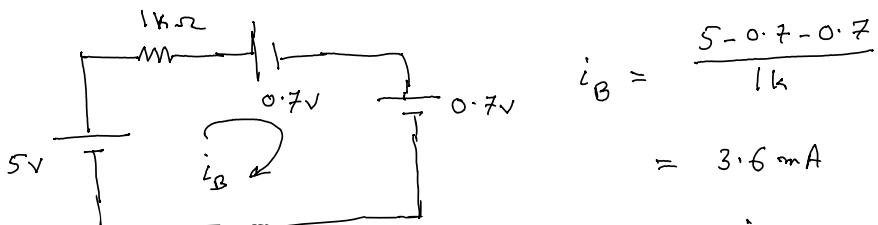
$$\frac{V_i}{10} = -\frac{V_o}{10 \times 12}, \therefore \boxed{\frac{V_o}{V_i} = -12}$$

3. A.

Find the current through the collector for the following circuit.  $V_{BE} = 0.7V$ ,  $V_f = 0.7V$ ,  $V_{CE(sat)} = 0.2V$   
 $\beta = 30$ , (current gain),  $V_Z = 5V$



Sol<sup>n</sup>: Assume, the transistor is Active. Diode is forward biased &  $D_z$  is reverse biased. Then, the Base-Emitter cut current  $i_B$ ,



$$\therefore I_C = \beta i_B = 108mA$$

∴ for the C-E ckt

$$-2.2 \times 10^3 - V_{CE} + 12 = 0$$

$$V_{CE} = -ve$$

That means the transistor is not in the active region,  
 But the BE is forward biased,  $\therefore$  the transistor is  
 in the saturation region

$$V_{CE} = 0.2V$$

$\therefore$  for the C-E ckt

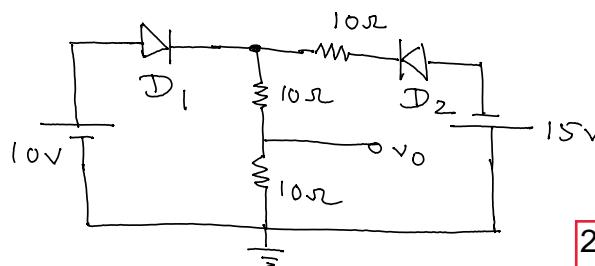
$$-2.2 \times I_C - V_{CE} + 12 = 0$$

$$I_C = \frac{12 - 0.2}{2.2} = 5.3636 \text{ mA.}$$

6 pts

3.b.

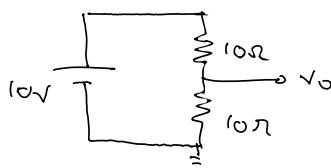
Assume the diodes are ideal. Find  $V_o$ .



2pts

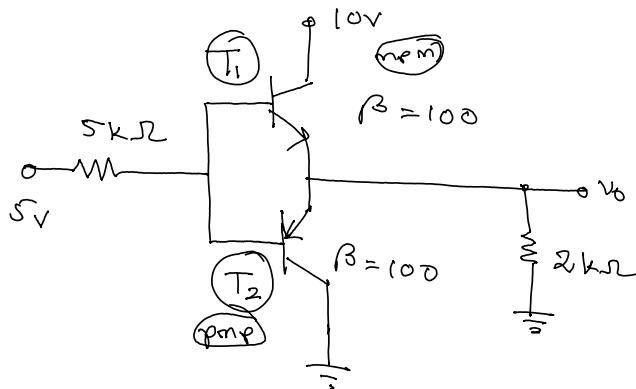
Soln:

Assume  $D_1$  is forward &  $D_2$  is reverse biased.



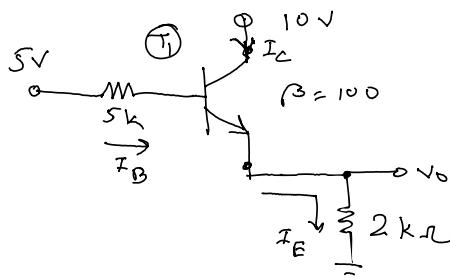
$$V_o = \frac{10}{10+10} \times 10V = 5V$$

3. C. The output voltage of the ckt is —



Soln

$T_2$  will be cut-off, since the BE junction is reverse biased for the pnp transistor.



$$5 - 5I_B - V_{BE} - 2I_E = 0$$

$$\Rightarrow 5 - 5I_B - 0.7 - 2(\beta + 1)I_B = 0$$

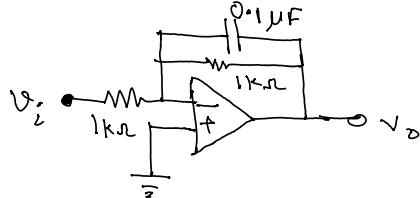
$$\Rightarrow 207I_B = 4.3$$

$$\Rightarrow I_B = \frac{4.3}{207} \text{ mA}, \quad I_E = \frac{101 \times 4.3}{207} \text{ mA.}$$

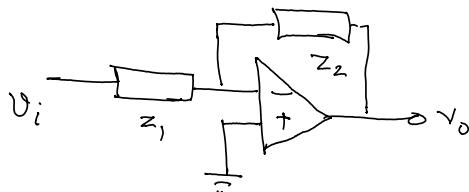
2 pts

$$V_o = 2I_E = 4.19 \text{ V}$$

5. A. The operational amplifier shown in the figure is ideal.  $v_i = 2 \sin(2\pi \times 2000t)$ . The amplitude of the output voltage  $v_o$  (in volt) is —



Sol<sup>M</sup>



$$z_1 = 1k$$

$$\begin{aligned} z_2 &= 1k \parallel \frac{1}{j\omega C} & \frac{1}{j\omega C} &= -j \frac{1}{4000\pi \times 0.1 \times 10^{-6}} \\ &= -\frac{1000 \times 795.8j}{1000 - 795.8j} & &= -j \frac{10^4}{4\pi} \\ & & &= -795.8j \Omega \end{aligned}$$

$$= + \frac{1000 \times 795.8 \angle -90^\circ}{1278 \angle 0^\circ}$$

$$\therefore |z_2| = 0.6227 \text{ k}\Omega$$

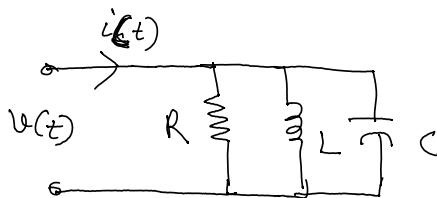
5 pts

$$\therefore \text{Amp at } v_o = \frac{|z_2|}{|z_{11}|} \cdot |v_i| = \frac{0.6227}{1} \times 2 = 1.2454 \text{ V}$$

5.b. Find the value of  $i(t)$  in sinusoidal expression for the following ckt, where

$$R = \frac{1}{3} \Omega, \quad L = \frac{1}{4} H \quad \text{&} \quad C = 3 F.$$

$$v(t) = \sin 2t ..$$



Sol<sup>no</sup>

$$\omega = 2 \text{ rad/s}$$

$$I = I_R + I_L + I_C$$

$$= \frac{V}{R} + \frac{V}{j\omega L} + \frac{V}{-\frac{j}{\omega C}}$$

$$= V [3 + 6j - 2j]$$

$$= 120^\circ \times (3+j4)$$

$$= (120^\circ) \times 5 \angle 53.13^\circ \quad \boxed{5 \text{ pts}}$$

$$= 5 \angle 53.13^\circ \Rightarrow \boxed{5 \sin(2t + 53.13)}$$

#### 4.A. Combinational Logic ckt problem.

A lawn sprinkling system is controlled automatically by certain combinations of the following variables.

i) Season,  $S$  ( $S=1$  if summer,  $S=0$  otherwise)

ii) Moisture content of soil,  $M$  ( $M=1$  if high,  $M=0$  if low)

iii) Outside temperature,  $T$ , ( $T=1$  if high,  $T=0$  if low)

iv) Outside humidity,  $H$ , ( $H=1$  if high,  $H=0$  if low)

The sprinkler should turn on under any of the following circumstances.

i) The moisture content is low in winter.

ii) the temp is high and the moisture content is low in summer.

iii) The temperature is high and the humidity is high in summer.

iv) the temperature is low and the moisture content is low in summer.

v) the temperature is high and the humidity is low in all seasons.

Design the simplest possible logic circuit involving the variables S, M, T & H for turning on the sprinkler system, using only 2 or 3 inputs NAND gates.

Sol<sup>n</sup>

The given circumstances (i)  $\rightarrow$  (v) are expressed in terms of the defined variables S, M, T & H as  $\rightarrow \bar{M}\bar{S}$ ,  $T\bar{M}S$ ,  $THS$ ,  $\bar{T}\bar{M}S$  &  $T\bar{H}$ , respectively.

The Boolean expression of the output  $\rightarrow$

$$\begin{aligned} & \bar{S}\bar{M} + S\bar{M}T + STH + S\bar{M}\bar{T} + T\bar{H} \\ & = 00XX + 101X + 1X11 + 100X + XX10 \end{aligned}$$

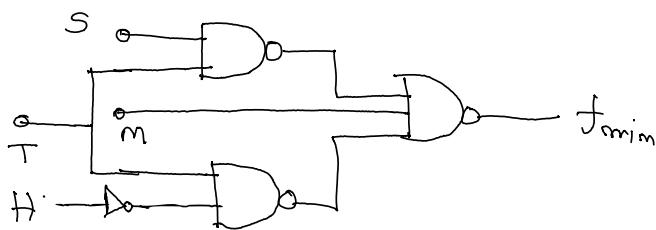
the expression in terms of minterms is,

$$\sum m(0, 1, 2, 3, 6, 8, 9, 10, 11, 14, 15)$$

The K-map in the SOP will be as follows,

$T$	$H$	00	01	11	10	
$S$	M	00	1	1	1	1
		01				1
		11		1	1	
		10	1	1	1	1

$$f_{\text{min}} = \overline{M} + ST + T\overline{H}$$

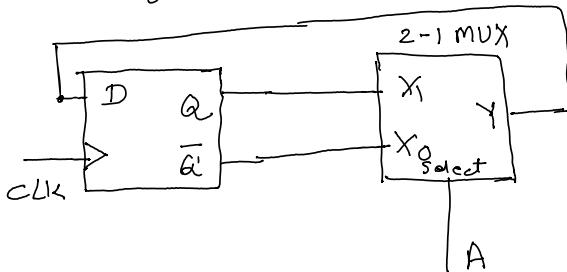


6 pts

## Sequential Ckt.

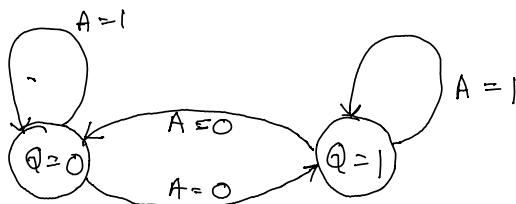
7.b.

Draw the state transition diagram for the logic circuit shown below. Show the intermediate steps for your work



Input  $\rightarrow A,$

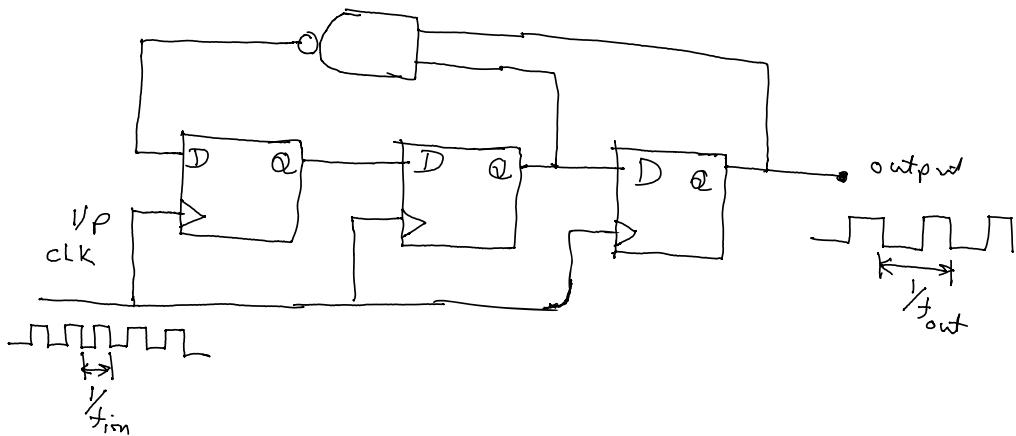
Ans .



2 pts

4.C.

For the sequential ckt shown below, if the input clock freq is  $f_{in}$ . what will be the frequency at the output, i.e.  $f_{out}$ .



Sol<sup>n</sup>

Hints : find out how many clock pulse needed to change the opp from 1 to 0 or 0 to 1.

$$f_{out} = \frac{1}{5} \cdot f_{in}$$

2 pts

