Introduction to Computer Architecture, 1DT093 Spring 2016 RETAKE, Answers

5. Multiple choice

1. How do you negate a two's complement number?
    a. Invert the most significant bit
    b. Invert
    c. Invert and add 1
    d. Invert and shift 1 step to the left

2. How many additions are needed for a serial multiplier to multiply 1010 times 1000?
    a. 1
    b. 2
    c. 4
    d. 16

3. The combinational logic does what in a sequential circuit?
    a. Store the current value
    b. Store the next value
    c. Calculate the current value
    d. Calculate the next value

4. What limits the speed of a sequential circuit?
    a. The slowest latch
    b. The slowest path through the combinational logic
    c. The slowest latch + the slowest path through the combinational logic
    d. The longest instruction

5. Which is faster, and why? DRAM or SRAM?

    a. DRAM: each bit is stored in a powered feedback loop so it can be read quickly
    b. DRAM: each bit is stored in a passive capacitor so it can be read quickly
    c. SRAM: each bit is stored in a powered feedback loop so it can be read quickly
    d. SRAM: each bit is stored in a passive capacitor so it can be read quickly

6. What happens if you activate two rows in a memory array at the same time?
    a. You corrupt the data you are reading
    b. You can read out twice as much data

c. You can read and write at the same time
d. You can read and write at the same time as long as it is to different rows

7. Double-pumping the register file fixed what kind of hazard?
   a. Data hazard
   b. Control hazard
   c. Pipeline Register hazard
   d. Structural hazard

8. When can we forward data in a pipeline?
   a. When the data is in the wrong place
   b. When we need the data from an instruction before us
   c. When multiple instructions need the same hardware at once
   d. All of the above

9. What is the minimum number of simultaneous reads and writes needed for a register file to work with the MIPS ISA?
   a. 0 writes, 2 reads
   b. 1 write, 2 reads
   c. 1 write, 3 reads
   d. 2 writes, 3 reads

10. What are the two key performance metrics for I/O?
   a. Throughput and latency
   b. Throughput and longevity
   c. Latency and longevity
   d. Density and longevity

11. Direct Memory Access (DMA) allows the I/O device to do what?
   a. Directly trigger interrupts when data is available
   b. Directly get access to the bus master
   c. Directly transfer data to the CPU's memory
   d. Directly modify the program's data

12. What is the benefit of polling?
   a. Simpler to program
   b. Uses more the processor for I/O
   c. Higher data throughput
   d. All of the above

13. If I have an Intel Xeon Phi processor with 62 cores, what is the best speedup I could get from a program that is 99% parallelizable?

a. 38.5
b. 58.4
c. 61.4
d. 62.0

14. Do page tables need a dirty bit? (hint: is Virtual Memory Write-Through or Write-back ?)

a. No, they don't store data, just VA-to-PA mappings
b. No, they are read only
c. Yes, the bit indicates if the data is on disk
d. Yes, the bit indicates if the page has been changed since it was loaded from disk

15. Writing to which address with the following page table would result in a page being loaded from disk?

e. 3
f. 4
g. 8
h. 12