EXAM

1TE717 Digital Technologies and Electronics
Faculty of Engineering Sciences

2023–06–09, 08:00 - 13:00

Location: Råbyvägen 95, sal 3

Aids: The following aids are allowed:

- Mathematics and / or Physics handbook,
- a small graphical calculator (e.g. TI-83 and similar),
- one A4 paper (two sides) with formulas or notes.

Note that exercise materials (exercise tasks, old exams, and solutions) are **NOT** allowed.

Observe: Do not treat more than one problem on each page and write a clear answer to each question. Each step in your solutions must be motivated. Lacking motivation will results in point deductions. Mark the total number of pages on the cover or first page

Grades: The *preliminary* grading criterium is

Grade 3: ≥ 4 points on each problem and total score of $20 - 29$ points.

Grade 4: ≥ 4 points on each problem and total score of $30 - 39$ points.

Grade 5: ≥ 4 points on each problem and total score of $40 - 50$ points.

Responsible: Isaac Skog, mobile phone 0708186805.

Good Luck!

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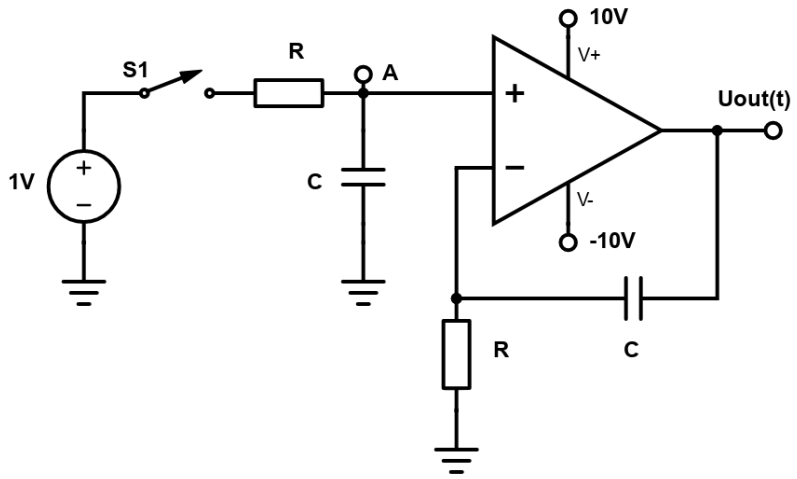

Figure 1: Circuit for problem 1.

Consider the circuit in figure 1. The switch S1 is closed at $t = 0$. Assume that the OpAmp is ideal and do the following.

1.a) Derive an expression for the voltage at point A. (3 pt)

1.b) What is the maximum and minimum values that $u_{out}(t)$ can take on? (1 pt)

1.c) Derive an expression for $u_{out}(t)$. (5 pt)

1.d) What mathematical operator does the circuit implement? (1 pt)

2

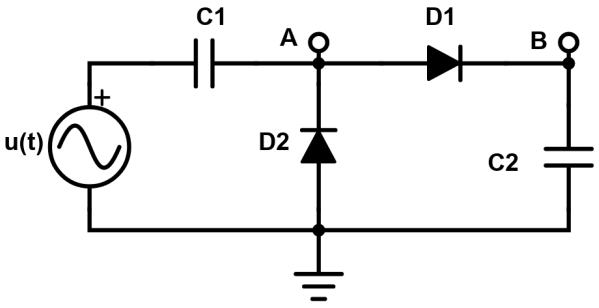

Figure 2: Circuit for problem 2.

2.a) Consider the circuit shown in figure 2. If the input voltage $u(t) = 5\sin(2\pi t)$ $[V]$ then draw a figure of the following things:

- The voltage at point (A). (2 pt)
- The voltage at point (B). (2 pt)
- What does the circuit do? (1 pt)

You can assume the diodes and capacitors to be ideal components, and that the circuit has been turned on for a long time.

2.b) This problem is about using the transistor as a switch. Use two npn-transistors and as many resistor you want to design an NAND-gate.

- Draw the circuit diagram of your circuit. (2 pt)
- Specify the values of the resistors in your circuit given the following component characteristics. Assume the circuit should work with 5V logics and the maximum input and output current of the OR-gate is 1 mA. Further, assume that the transistor has a DC-gain $h_{FE} = 100$, a base-emitter saturation voltage $V_{BE}(sat) = 700\ [mV]$, a collector-emitter saturation voltage $V_{CE}(sat) = 100\ [mV]$, and a maximum allowed collector current $I_{c_{max}} = 10\ [mA]$. Moreover, for a logical high signal the voltage should be $\geq 4\ [V]$ and for a logical low signal the voltage should be $\leq 1\ [V]$. (3 pt)

3

3.a) Design a sequence detector that detects the sequence 101 and outputs a logical 1 every time the sequence appears. For example, for the input 0110101011001 the output should be 0000101010000.

- Specify the state diagram for the sequential circuit. (3 pt)
- Specify the Boolean expressions for the circuit. (4 pt)

3.b) Show that the NAND-gate is a universal gate, i.e., show that one or more NAND-gates can be used to implement the AND, OR, and NOT operations. (3 pt)

4

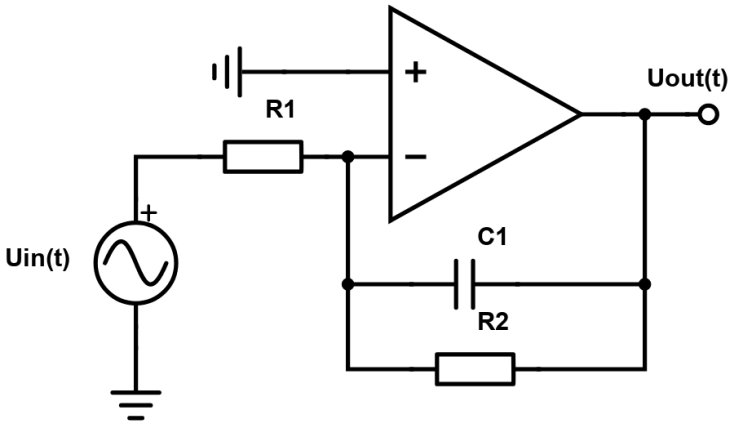

Figure 3: Circuit for problem 4.

Consider the active filter in figure 3 and assume that input $u_{in}(t) = cos(\omega t)\ [V]$.

4.a) Determine the frequency function $H_{u_{in},u_{out}}(j\omega)$ from u_{in} to u_{out}. (4 pt)

4.b) What type of filter is this? Motivate your answer. (2 pt)

4.c) If $R_1 = 1\ [k\Omega]$, $R_2 = 10\ [k\Omega]$, $C_1 = 10\ [\mu F]$, and $\omega = 10\ [rad/s]$, determine an expression for $u_{out}(t)$ (4 pt)

5

5.a) Determine the voltage across R_1 in the circuit shown in figure 4. (4pt)

5.b) Determine the resistance between point A and B in the circuit shown in figure 5. (6pt)

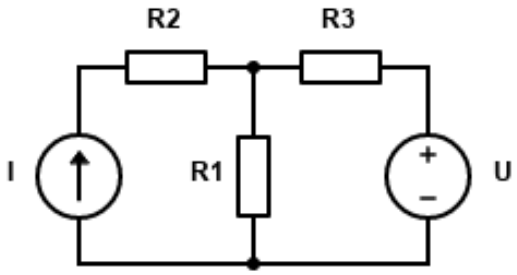

Figure 4: Circuit for problem 5a.

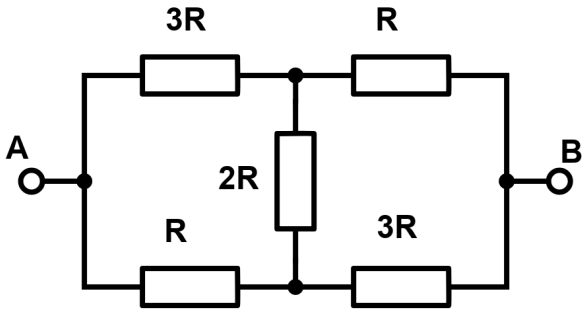

Figure 5: Circuit for problem 5b.