EXAM

1TE717 Digital Technologies and Electronics
Faculty of Engineering Sciences

2018–05–31, 14:00–19:00

Location: Polacksbacken, Skrivsalen

Aids:

- Mathematics and / or Physics handbook,
- a small graphical calculator (e.g. TI-83 and similar),
- one A4 paper (two sides) with handwritten formulas or notes.

Note that exercise materials (exercise tasks, old exams, and solutions) are **NOT** allowed.

Observe: Do not treat more than one problem on each page.
Each step in your solutions must be motivated.
Lacking motivation will results in point deductions.
Write a clear answer to each question and clearly indicate which formulas are used.
Mark the total number of pages on the cover or first page

The exam consists of Part A and Part B, for a total of 50 points. The points for each problem are also indicated.

Passing Grade: To pass the course, you need to successfully attain the learning goals of the course. This means that you would pass the exam if you obtain **at least 50%** of the points at **each question of part A**.

Exam Grade: Passing the exam would grant the grade 3. Grades 4 and 5 are obtained based on the total score obtained in the exam (Parts A and B). Bonus points obtained in the course may be used in the questions of Part B.

Responsible: André Teixeira, office phone 018 471 7003, mobile phone 073 429 7831.

Good Luck!

Part A

A.1

Design a combinatorial network that implements the following logical function $f(x_3, x_2, x_1, x_0) = \Sigma(0, 2, 4, 5, 6, 7) + d(8, 10, 12, 14)$ in minimal SP-form using only NAND gates. Draw the logical circuit. (Sub-Total A.1: 4 pt)

A.2

This question is about designing a sequential machine that compares two 2-bit binary numbers, $x = (x_1, x_0)$ and $y = (y_1, y_0)$, where x_1 and y_1 are the MSB. The sequential network should give a three bit output $z = (z_2, z_1, z_0)$ such that $z = (0, 0, 0)$ if the comparison is still ongoing, $z = (0, 0, 1)$ if $x < y$, $z = (1, 0, 0)$ if $x > y$, and $z = (0, 1, 0)$ if $x = y$.
The binary numbers x and y are both fed as bit streams, i.e., they have been loaded into shift registers from where they are read one bit at a time per clock cycle, MSB first. Therefore, you may consider that the input to the sequential machine are two bit streams, x_i and y_i, MSB first.

Perform the first steps of the design of the sequential network: i) derive the state-diagram, ii) choose the state-coding, and iii) write the truth tables determining the behavior of the sequential network and its outputs.
Given your design choice, state whether you have used a Mealy or a Moore type of network, and indicate how many D flip-flops would be needed to implement your circuit.
Note: you need ***not*** *to derive the minimal SP-form Boolean expressions, nor to draw the final circuit diagrams with gates and flip-flops.*

(Sub-Total A.2: 6pt)

A.3

A.3.a) Consider the network in Fig. 1, where $R_1 = R_2 = R_3 = R_4 = 10\Omega$, $V_1 = 5\,V$ and $V_2 = 2\,V$. Determine the current passing through R_2 (magnitude and direction). (4 pt)

A.3.b) Consider the amplifier circuit in Fig. 2, where $R_1 = 100\,\Omega$, $R_2 = 200\,\Omega$, and $V_r = 2V$. Assuming an ideal OpAmp and sufficiently large supply voltages and using Ohm's and Kirchoff's laws, derive the expression for the output voltage V_o as a function of V_{in}. (4 pt)

(Sub-Total A.3: 8 pt)

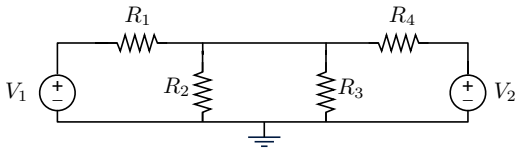

Figure 1: Circuit for Question A.3.a).

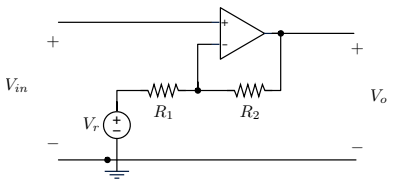

Figure 2: Circuit for Question A.3.b).

A.4

A.4.a) Consider the circuit in Fig. 3, where the Zener diode has $V_z = 5V$, and the supply voltage is $V_{in} = 9\,V$. Design R so that the current is limited to 20mA when there is no load (i.e., $R_L = \infty$). (3 pt)

A.4.b) Suppose now that $R = 200\Omega$ and that the load resistor R_L has a variable and unknown resistance. What is the lowest resistance of R_L for which the voltage is still correctly regulated at $5V$? (3 pt)

(Sub-Total A.4: 6pt)

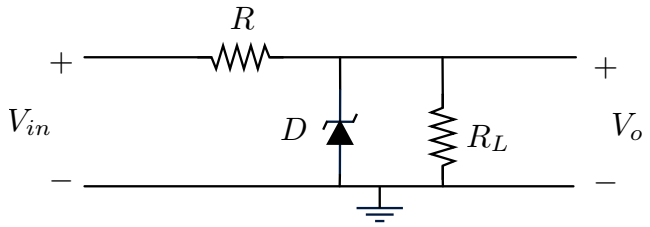

Figure 3: Circuit for Question A.4.

A.5

Consider the filter in Fig. 4. Suppose that $V_{in}(t)$ is a sinusoidal voltage signal with $V_{in}(t) = 3\sin(20000\pi t - \frac{\pi}{2})$, i.e., amplitude 3, frequency 10000 Hz, and phase shift of $-\frac{\pi}{2}$ rad . Using the theory of AC circuit analysis and complex impedances, derive the expression of the output voltage signal $V_{out}(t)$ for $R_1 = R_2 = 500\,\Omega$ and $C = 0.1\,\mu F$.

(Sub-Total A.5: 6pt)

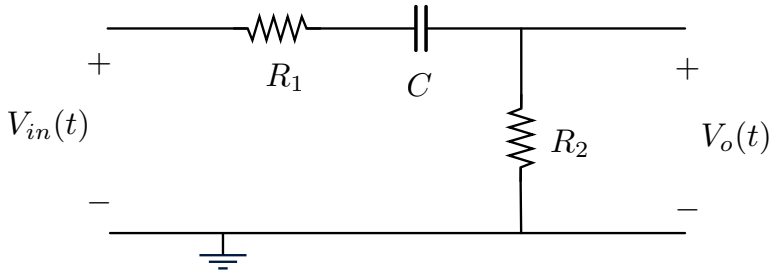

Figure 4: Circuit for Question A.5.

Part B

B.1

Consider the amplifier circuit in Fig. 5. This is similar to the circuit considered in question A.3.b), in which case the switch was connected to the contact B, thus connecting the resistor R_1 to V_r.

Unfortunately, there is no extra voltage source available to supply $V_r = 2\,V$, so the circuit has to be implemented differently. This is currently done by connecting the switch to the contact A, thus connecting the resistor R_1 directly to a potentiometer. Suppose that $R_3 = 10\,k\Omega$, and that the potentiometer is set at 50% of its range. Consider the same values as in question A.3.b): $R_1 = 100\,\Omega$ ad nd $R_2 = 200\,\Omega$.

Motivate whether the circuit connected to A has been correctly implemented, that is, whether or not one obtains the same output V_o regardless if one switches to contact A or to contact B. If the implementation using contact A is incorrect, how could it be corrected?
Note: A detailed analysis of the circuit is not strictly required, as long as the motivation is well-founded.

(Sub-Total B.1: 5pt)

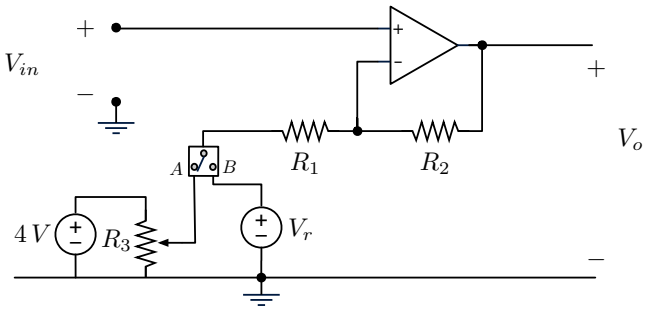

Figure 5: Circuit for Question B.1.

B.2

The purpose of the voltage regulation circuit illustrated in Fig. 6 is to keep a constant output voltage V_o at a certain value, despite possible variations of the supply voltage V_{in}. The following characteristics of the circuit are known: $V_{in} = 9V$, $V_z = 5.6V$, $V_{BE} = 0.6V$, $\beta = h_{FE} = 100$, and $R = 200\,\Omega$. Suppose that R_L is a varying load, whose resistance can vary. Analyze the circuit to find:

B.2.a) what is the output voltage V_o, assuming the transistor is switched on and the Zener diode is conducting in the reverse direction. (2pt)

B.2.b) what is the smallest value or R_L for which the circuit still behaves as intended. (3pt)

(Sub-Total B.2: 5pt)

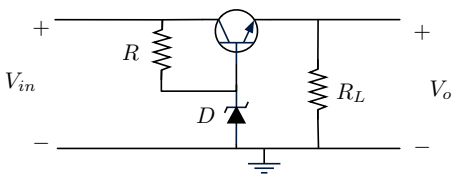

Figure 6: Circuit for Question B.2.

B.3

This question is about the design of filters for sinusoidal voltage signals. Consider an inverting amplifier with complex impedances, whose transfer function is $H(jw) = -\frac{Z_2}{Z_1}$, where Z_1 and Z_2 are complex impedances.
Suppose that the complex impedances Z_1 and Z_2 are each composed of one resistor and capacitor, respectively (R_1, C_1) and (R_2, C_2). The objective of this question is to, using two pairs of resistors and capacitors (R_1, C_1) and (R_2, C_2), design the complex impedances Z_1 and Z_2 so that the filter meets the following specifications:

1. for low frequencies, the gain of the filter is 10;
2. for high frequencies, the gain is 1;
3. the low-frequency gain can be adjusted by varying one of the resistors R_1 or R_2, without affecting the gain at very high frequencies.

B.3.a) Motivate whether (R_1, C_1) and (R_2, C_2) should both be connected in series, or if they should both be connected in parallel, to meet the last specification.
Hint: Begin by deriving the expressions for Z_1 when the resistor-capacitor pair (R_1, C_1) is connected in series and in parallel, respectively. That is, derive the expression for $Z_1 = Z_{R_1} + Z_{C_1}$ and $Z_1 = Z_{R_1} // Z_{C_1}$. (3 pt)

B.3.b) Given your choice of connection in series or parallel, derive the transfer function of the filter and suggest values for R_1, R_2, C_1, and C_2 that meet all the specifications. Indicate what are the cut-off frequencies for your choice of values. (2 pt)

(Sub-Total B.3: 5pt)

B.4

Consider the comparator circuit described in question A.2, but now for 8-bit binary numbers x and y that have been stored in 8-bit shift registers and are read serially, one bit per clock cycle, MSB first. Therefore, you may consider that the input to the sequential machine are two bit streams, x_i and y_i, MSB first. The output $z = (z_1, z_2, z_3)$ of the comparator should be $z = (0, 0, 0)$ while the comparison is ongoing. Once the comparison end, the output should have the following values for at least one clock pulse: $z = (0, 0, 1)$ if $x < y$, $z = (1, 0, 0)$ if $x > y$, and $z = (0, 1, 0)$ if $x = y$.

This circuit can be implemented by combining the following elements:

- a 1-bit comparator with two bits A and B as inputs and the same 3-bit output w as described in question A.2: given two input bits A and B, the output is $w = (0, 0, 1)$ if $A < B$, $w = (1, 0, 0)$ if $A > B$, and $w = (0, 1, 0)$ if $A = B$;
- a 3-bit counter (also known as MOD-8 counter), which outputs a 3-bit binary number $c = (c_2, c_1, c_0)$ with the count value from 0 to 7, which is incremented by 1 per clock cycle.
- at most two D flip-flops;
- a few combinatorial circuits to obtain the new states and the output from the input signals and the previous elements.

Design a sequential machine (Moore or Mealy type) that implements the 8-bit comparator circuit, with the appropriate motivation for your design by means of a state diagram, and explain its operation. Draw the resulting connections between all the elements, including the Boolean functions that give the new states and the output.
Note: the Boolean functions do not need to be in minimal SP-form.

(Sub-Total B.4: 5pt)