EXAM

1TE717 Digital Technologies and Electronics
Faculty of Engineering Sciences

2018–08–20, 08:00–13:00

Location: Fyrislundsgatan 80, Sal 1

Aids:

- Mathematics and / or Physics handbook,
- a small graphical calculator (e.g. TI-83 and similar),
- one A4 paper (two sides) with handwritten formulas or notes.

Note that exercise materials (exercise tasks, old exams, and solutions) are **NOT** allowed.

Observe: Do not treat more than one problem on each page.
Each step in your solutions must be motivated.
Lacking motivation will results in point deductions.
Write a clear answer to each question and clearly indicate which formulas are used.
Mark the total number of pages on the cover or first page

The exam consists of Part A and Part B, for a total of 50 points. The points for each problem are also indicated.

Passing Grade: To pass the course, you need to successfully attain the learning goals of the course. This means that you would pass the exam if you obtain **at least 50%** of the points at **each question of part A**.

Exam Grade: Passing the exam would grant the grade 3. Grades 4 and 5 are obtained based on the total score obtained in the exam (Parts A and B).

Responsible: André Teixeira, office phone 018 471 7003, mobile phone 073 429 7831.

Good Luck!

Part A

A.1

Design a combinatorial network that implements the following logical function $f(x_3, x_2, x_1, x_0) = \Sigma(0, 2, 5, 7, 8, 13) + d(10, 12, 15)$ in minimal SP-form using only NAND gates. Draw the logical circuit. (Sub-Total A.1: 4 pt)

A.2

This question is about designing a sequential machine that detects a given sequence within a stream of bits x_i. Suppose that the sequence to be detected is 1011. While the sequence is not detected, the circuit should have the output $u = 0$. Every time that the sequence is detected, the output u should be set to 1, and then return to zero when a new input bit x_i is read.
Perform the first steps of the design of the sequential network: i) derive the state-diagram, ii) choose the state-coding, and iii) write the truth tables determining the behavior of the sequential network and its outputs.
Given your design choice, indicate whether it is a Mealy or Moore type, and how many D flip-flops would be needed to implement your circuit. Motivate your answer!
Note: you need ***not*** *to derive the minimal SP-form Boolean expressions, nor to draw the final circuit diagrams with gates and flip-flops.*

(Sub-Total A.2: 5pt)

A.3

A.3.a) Consider the network in Fig. 1, where $R_4 = R_5 = 10\Omega$, $R_1 = R_2 = R_3 = 20\,\Omega$, $V_1 = 5\,V$ and $V_2 = 2\,V$. Determine the current passing through R_2 (magnitude and direction). (4 pt)

A.3.b) Consider the amplifier circuit in Fig. 2, where $R_1 = 100\,\Omega$, $R_2 = 200\,\Omega$, $R_3 = 200\,\Omega$ and $V_{in} = 3V$. Assume that the OpAmp is ideal and that the supply voltages are sufficiently large. Using Ohm's and Kirchoff's laws, derive the expression for the output voltage V_o as a function of V_{in} and determine the current passing through R_3 (magnitude and direction). (5 pt)

(Sub-Total A.3: 9 pt)

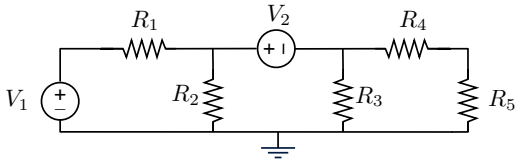

Figure 1: Circuit for Question A.3.a).

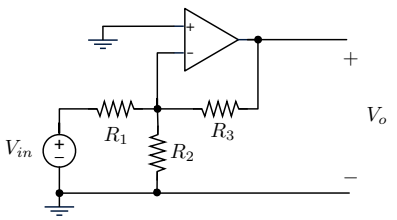

Figure 2: Circuit for Question A.3.b).

A.4

Consider the circuit in Fig. 3, where the bipolar transistor has the following characteristics: $\beta = 100$, $V_{CE_{sat}} = 0.2\,V$, and $V_{BE} = 0.6\,V$. Suppose that $V_s = 12\,V$, $R = 200\,\Omega$, and $V_{in} = 5\,V$.

A.4.a) Suppose that $R_b = 10\,k\Omega$. Determine the values of V_{CE}, I_E, and I_C. (3 pt)

A.4.b) Determine what is the largest value of R_b so that the transistor is on saturation mode when it is conducting. (3 pt)

(Sub-Total A.4: 6pt)

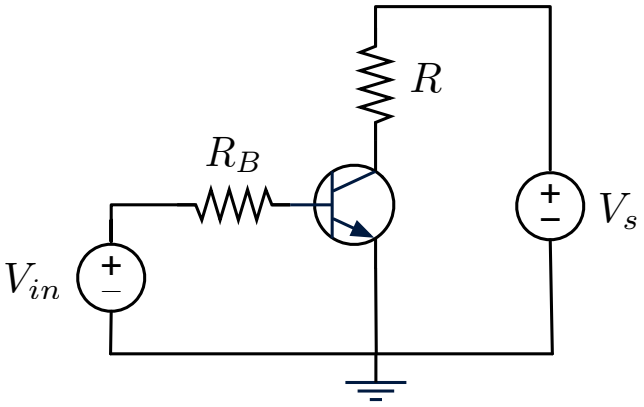

Figure 3: Circuit for Question A.4.

A.5

Consider the filter in Fig. 4. Suppose that $V_{in}(t)$ is a sinusoidal voltage signal with $V_{in}(t) = 2\sin(8000\pi t + \frac{\pi}{3})$, i.e., amplitude 0.5, frequency 4000 Hz, and phase shift of $\frac{\pi}{3}$ rad. Using the theory of AC circuit analysis and complex impedances, derive the expression of the output voltage signal $V_o(t)$ for $R = 50\,\Omega$, $C = 1.6\,\mu F$, and $L = 1\,mH$, and classify this circuit as either a low-pass, high-pass, band-pass, or a band-stop filter.

(Sub-Total A.5: 6pt)

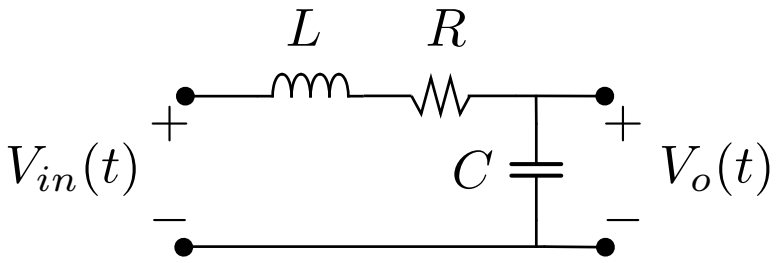

Figure 4: Circuit for Question A.5.

Part B

B.1

Consider the OpAmp circuit in Fig. 5, where $R_1 = 10\,k\Omega$. Design R_2 and R_3 so that $V_o = 3V_r - V_{in}$.

(Sub-Total B.1: 5pt)

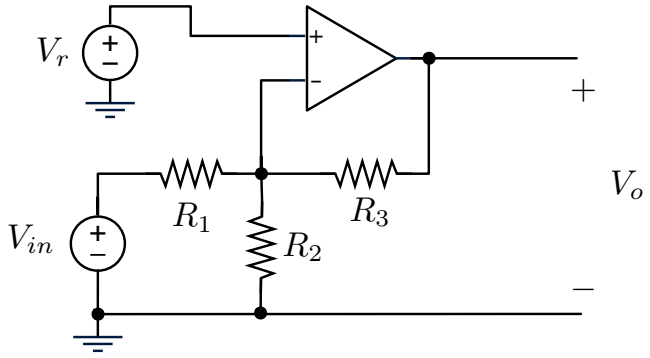

Figure 5: Circuit for Question B.1.

B.2

Consider the circuit shown in Fig. 6, where the diode D_1 has a forward voltage drop of $V_D = 0.7\,V$, all the other components are assumed to be ideal, and the voltage supplies of the OpAmps are sufficiently large. The transistor T_1 is a n-channel enhancement-type MOSFET that begins conducting if $V_{GS} > V_{GS,th} = 2\,V$.

Describe the behavior of the circuit, motivated by a brief explanation of the role of each component and of the signal V_r. Additionally, sketch what the output voltage $V_o(t)$ would be for the input signal $V_{in}(t)$ and $V_r(t)$ shown in Fig. 7.

(Sub-Total B.2: 5pt)

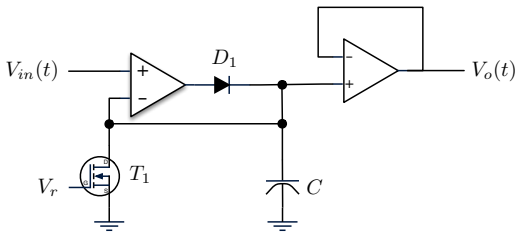

Figure 6: Circuit for Question B.2.

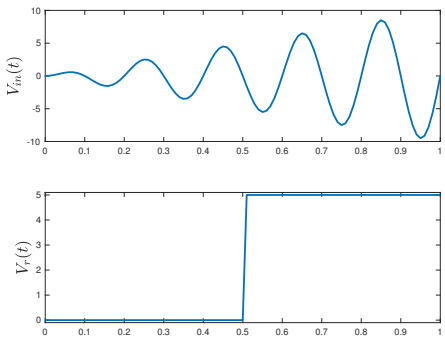

Figure 7: Input signals for Question B.2.

B.3

This question is about the design of filters for sinusoidal voltage signals. Design a passive band-pass filter using a **series circuit** of one resistor R, one capacitor C, and one inductor L (similar to the one in A.5), and **motivate** your design choice.
Confirm that the design is according to the specifications by, for your choice of values, deriving the transfer function of the circuit, evaluating it for at least two different frequencies of your choice, and discussing the results obtained.

(Sub-Total B.3: 5pt)

B.4

Consider the problem described in question A.2. Suppose now that the sequence to be detected has been stored in a 4-bit serial-in serial-out shift register.
The shift register has the following inputs and output:

- D_0 is the serial **input** to register. The value of D_0 is loaded into the first bit of the shift register when the stored data is shifted.
- CLK is the clock **input** bit that triggers a shift of the data in the register when it changes from 0 to 1.
- Q_3 is the serial **output** of the register, corresponding to the last bit stored in the register.

To detect the sequence stored in the shift register, the network specified in A.2 has to be modified to control the shift-register and read from it, and the shift-register needs to be properly connected to the sequential network.
Draw the state diagram of a **Mealy-type** sequential network, using at most 4 states, that reads the sequence from and controls operation of the shift register, and produces the desired output u once the sequence is detected in the input bit stream x_i. Specify how the inputs and output of the shift-register should be connected to the sequential network.

Note: you may need to add one auxiliary output signal to the sequential network.

(Sub-Total B.4: 5pt)