EXAM

1TE717 Digital Technologies and Electronics
Faculty of Engineering Sciences

2023–10–20, 08:00 - 13:00

Location: Danmarksgatan 30, sektion 1

Aids: The following aids are allowed:

- Mathematics and / or Physics handbook,
- a small graphical calculator (e.g. TI-83 and similar),
- one A4 paper (two sides) with formulas or notes.

Note that exercise materials (exercise tasks, old exams, and solutions) are **NOT** allowed.

Observe: Do not treat more than one problem on each page and write a clear answer to each question. Each step in your solutions must be motivated. Lacking motivation will results in point deductions. **Mark the total number of pages on the cover or first page, and write the exam code on top of every page.**

Grades: The *preliminary* grading criterium is

Grade 3: ≥ 4 points on each problem and total score of $20 - 29$ points.

Grade 4: ≥ 4 points on each problem and total score of $30 - 39$ points.

Grade 5: ≥ 4 points on each problem and total score of $40 - 50$ points.

Responsible: Isaac Skog, mobile phone 0708186805.

Good Luck!

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1 Assessed ILO: Analyse and design circuits with operational amplifiers for basic functions.

1.a) Consider the voltage to current converter circuit in figure 1. Assume the OpAmp to be ideal and derive an expression for the current I_x flowing through resistor Rx as a function of the voltages $U1$ and $U2$. (4 pt)

Hint: The negative feedback is the dominating feedback.

1.b) Consider the square wave generator circuit in figure 2. Assume that OpAmp is ideal and do the following.

- Draw a graph that shows the voltage $U+$ as a function of time. (1 pt)
- Draw a graph that shows the voltage $U-$ as a function of time. (1 pt)
- Show that the output square wave has a period time $T = RC\ln(9)$ seconds. (4 pt)

Hint: The voltage across the capacitor in a RC-circuit that is started to be charged at $t = 0$ is given by $u_c(t) = u_s - (u_s - u_{init})e^{-t/RC}$, where u_s and u_{init} denote the supply voltage and initial capacitor voltage, respectively.

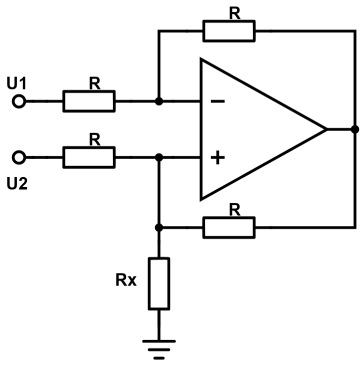

Figure 1: Circuit for problem 1a.

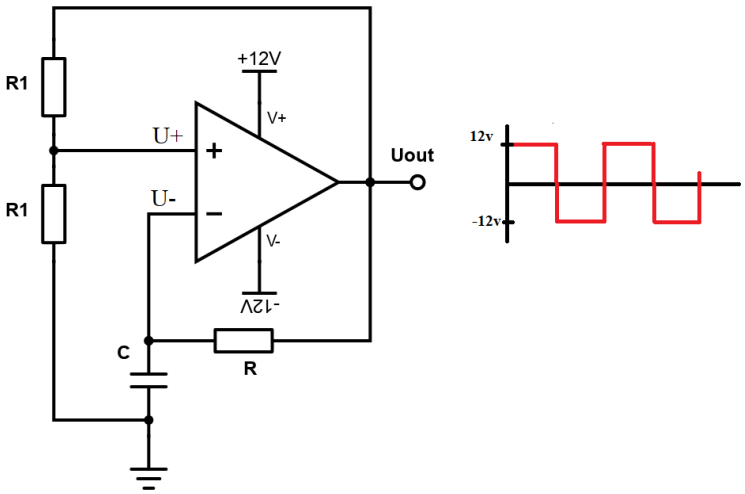

Figure 2: Circuit for problem 1b.

2 Assessed ILO: Design and realise simple circuits with diodes and transistors.

2.a) Consider the voltage regulator circuit in figure 3. The zener diodes has a zener voltage $U_z = 4.7$ $[V]$, requires a minimum backward bias current of 10 $[mA]$, and has a maximum power rating of 0.5 $[W]$ (recall $P = UI$). The load requires a voltage of 4.7 $[V]$ and draws a current between 10 and $I_{\max}$ $[mA]$.

- What is the maximum current allowed to flow through the zener-diode? (1 pt)
- What is the minimum allowable resistance R? (2 pt)
- What is the maximum allowable load current $I_{\max}$. (2 pt)

2.b) Consider the common emitter amplifier circuit in figure 4. Assume that the transistor is operating in its active region.

- Show that

$$U_{\text{out}} = 12 - \frac{R_c(U_{\text{in}} + U_{\text{bias}} - U_{be})}{R_e(1 + \frac{1}{\beta})}$$

  where U_{be} is the bias to emitter voltage and β is the DC gain of the transistor. (3 pt)
- Let $U_{be} = 0.6$ $[V]$, $\beta >> 1$, and $U_{\text{in}} = 0.1\sin(t)$ $[V]$. Select the gain R_c/R_e and bias U_{bias} so that $U_{\text{out}} = 6 - 5\sin(t)$ $[V]$. (2 pt)

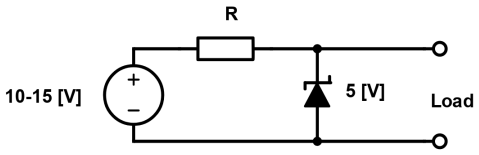

Figure 3: Circuit for problem 2a.

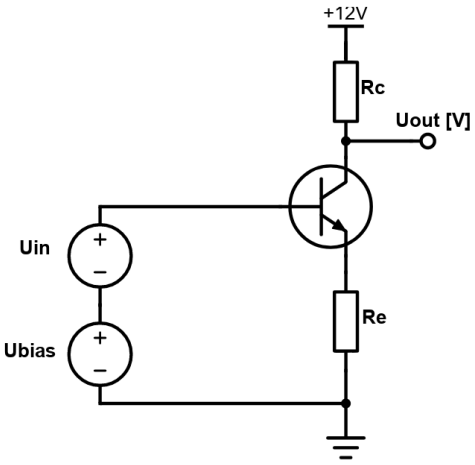

Figure 4: Circuit for problem 2b.

3 Assessed ILO: Design combinatorial and sequential nets that implement given logical functions and state machines.

Consider the electronic dice system in figure 5. When the switch is closed the counter counts the clock pulses. The counter outputs the number of pulses in terms of the 3-bit word $\{x_0, x_1, x_2\}$, where x_0 is the least significant bit.

3a) Determine the display logics so that the word $\{x_0, x_1, x_2\}$ is mapped to the correct display on the dice. That is, derive the Boolean expressions $D_i = f_i(x_0, x_1, x_2)$, $i = 1, \ldots, 7$, where D_i denotes the i:th diode. (4 pt)

3b) Designs the clock pulse counter and make sure it wraps around properly.

- Specify the state diagram and the number of flip-flops needed (1 pt)
- Specify Boolean expressions for the state-machine logics (2 pt)
- Draw the circuit diagram of the counter (3 pt)

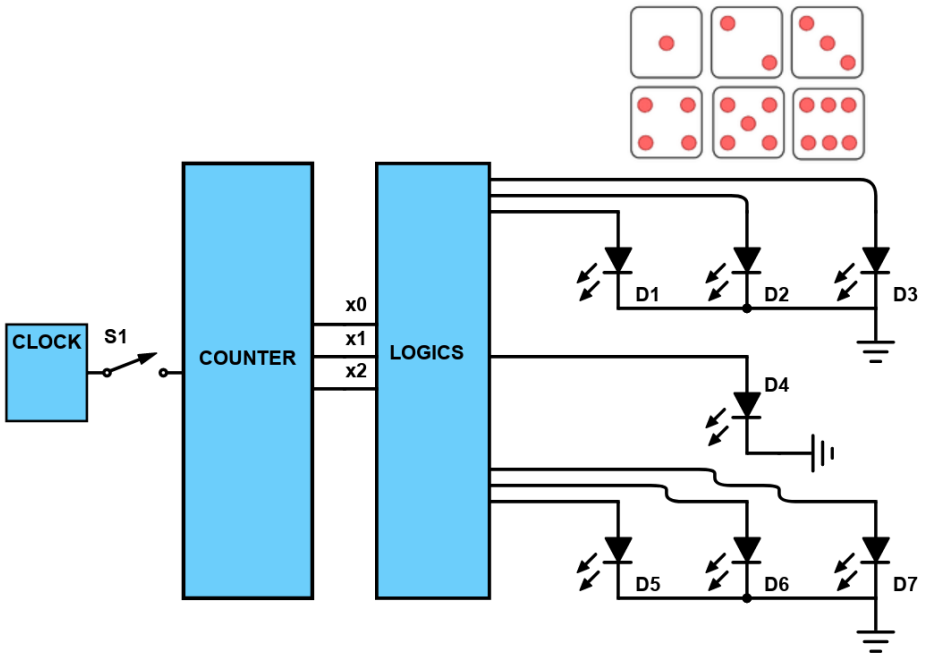

Figure 5: Electronic dice system.

4 Assessed ILO: Use phasor diagrams and complex impedances for analysing circuits with capacitors and coils.

Consider the RL-filter in figure 6 and assume that input $u_{in}(t) = A\cos(\omega t)$ $[V]$.

4.a) Show that the frequency function from $u_{in}(t)$ to $u_{out}(t)$ is given by (4 pt)

$$H_{u_{in},u_{out}}(j\omega) = \frac{wL}{\sqrt{R^2+\omega^2L^2}} e^{j\left(\frac{\pi}{2}-\arctan(\omega L/R)\right)}$$

4.b) Show that $H_{u_{in},u_{out}}(j\omega)$ is a high-pass filter. (2 pt)

4.c) The cut-off frequency ω_0 of the RL filter is defined as the solution to

$$|H_{u_{in},u_{out}}(\omega_0)| = \frac{1}{\sqrt{2}} \lim_{\omega\to\infty} |H_{u_{in},u_{out}}(j\omega)|.$$

Show that $\omega_0 = R/L$ $[rad/s]$ (2 pt)

4.d) Determine an expression for $u_{out}(t)$ if $u_{in}(t) = A\cos(\omega_0 t) + B\sin(\omega_0 t)$ $[V]$. (2 pt)

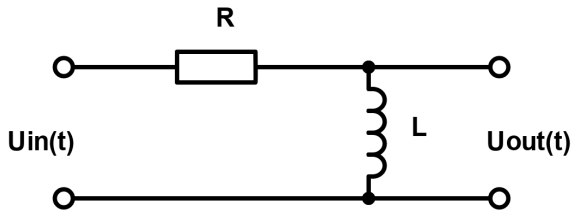

Figure 6: Circuit for problem 4.

5 Assessed ILO: Use circuit theory for analysing resistive nets and for designing such nets for basic signal conditioning.

5.a) Consider the circuit in figure 7 and do the following.

- Determine the current through the $R3$ resistor. (3pt)
- Determine the equivalent resistance as seen from the voltage source U. (3pt)

5.b) In figure 8 a Wheatstone bridge is shown. The Wheatstone bridge is used to measure the unknown resistance Rx using the voltmeter and the adjustable resistance $R3$. If $R3$ has been adjusted so that $Um = 0\ [V]$, then show that $Rx = R2\,R3/R1$. (4pt)

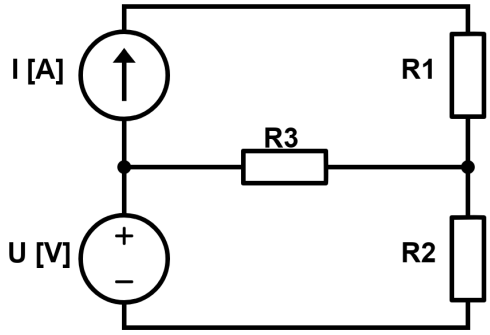

Figure 7: Circuit for problem 5a.

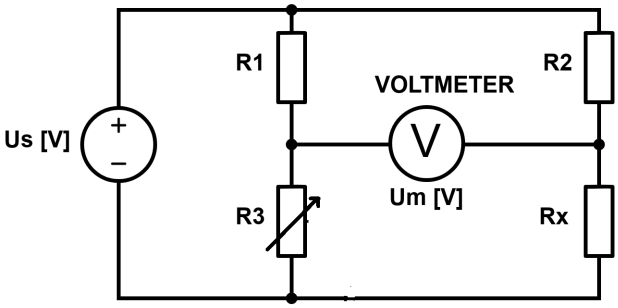

Figure 8: Circuit for problem 5b.