EXAM

1TE717 Digital Technologies and Electronics
Faculty of Engineering Sciences

2019–10–31, 08:00–13:00

Location: Polacksbacken, Skrivsal

Aids:

- Mathematics and / or Physics handbook,
- a small graphical calculator (e.g. TI-83 and similar),
- one A4 paper (two sides) with handwritten formulas or notes.

Note that exercise materials (exercise tasks, old exams, and solutions) are **NOT** allowed.

Observe: Do not treat more than one problem on each page.
Each step in your solutions must be motivated.
Lacking motivation will results in point deductions.
Write a clear answer to each question and clearly indicate which formulas are used.
Mark the total number of pages on the cover or first page

The exam consists of Part A and Part B, for a total of 50 points. The points for each problem are also indicated.

Passing Grade: To pass the course, you need to successfully attain the learning goals of the course. This means that you would pass the exam if you obtain **at least 50%** of the points at **each question of part A**.

Exam Grade: Passing the exam would grant the grade 3. Grades 4 and 5 are obtained based on the total score obtained in the exam (Parts A and B).

Responsible: André Teixeira, office phone 018 471 7003, mobile phone 073 429 7831 (preferred).

Good Luck!

Part A

A.1

Design a combinatorial network that implements the following logical function

$$f(x_3, x_2, x_1, x_0) = \Sigma(0,\, 2,\, 4,\, 8,\, 10) + d(1,\, 6,\, 13,\, 14)$$

in minimal SP-form using only NAND gates. Draw the logical circuit. (Sub-Total A.1: 4 pt)

A.2

This question is about designing a sequential machine that detects a given sequence within a stream of bits x_i.
The circuit normally gives $y = 0$ as the output, until the sequence 01010 is detected. Every time that the sequence is detected, the output y should be set to 1 for one clock cycle, and then return to zero when a new input bit x_i is read and detect a complete new sequence (i.e., without overlapping a previous sequence).

Perform the first steps of the design of the sequential network:

1. derive the state-diagram,
2. choose the state-coding,
3. write the truth tables determining the behavior of the sequential network and its outputs.

Given your design choice, indicate whether it is a Mealy or Moore type, and how many D flip-flops would be needed to implement your circuit. Motivate your answer!
Note: you need ***not*** *to derive the minimal SP-form Boolean expressions, nor to draw the final circuit diagrams with gates and flip-flops.*

(Sub-Total A.2: 5pt)

A.3

A.3.a) Consider the network in Fig. 1, where $R_2 = R_3 = R_5 = 30\,\Omega$, $R_1 = R_4 = 10\,\Omega$, and $V_1 = 5\,V$. Determine the current passing through the voltage source V_1 (magnitude and direction). (5 pt)

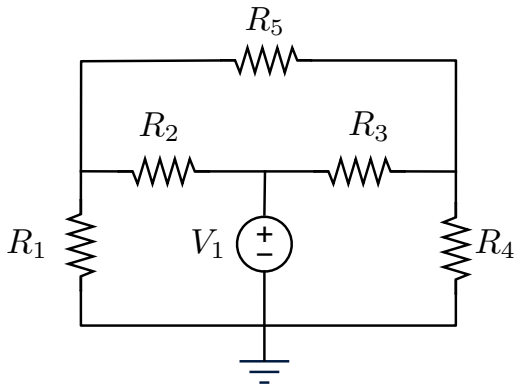

Figure 1: Circuit for Question A.3.a).

A.3.b) Consider the amplifier circuit in Fig. 2, where $R_1 = 100\,\Omega$, $R_2 = 200\,\Omega$, and $V_{in} = 3V$. Let $V_r = 2V$, and assume that the OpAmp is ideal and that the supply voltages are sufficiently large. **Using Ohm's and Kirchoff's laws**, **derive the expression** for the output voltage V_o as a function of V_{in} and V_r and determine the current passing through R_2 (magnitude and direction). (4 pt)
Note: merely identifying and writing down the correct formula, without including the supporting derivations based on circuit analysis, will give no points.

(Sub-Total A.3: 9 pt)

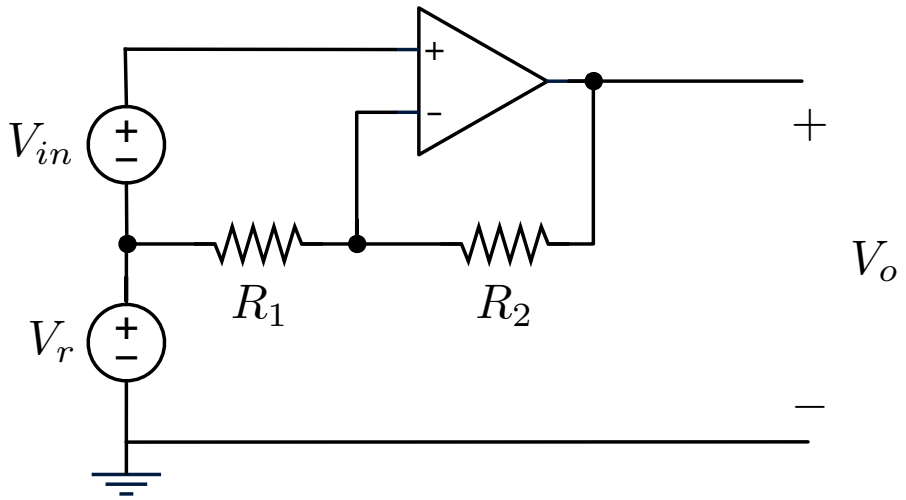

Figure 2: Circuit for Question A.3.b).

A.4

Consider the circuit in Fig. 3, where the bipolar transistor has the following characteristics: $\beta = 300$, $V_{CE_{sat}} = 0.2\,V$, and $V_{BE} = 0.6\,V$. Suppose that $V_s = 24\,V$, $R = 100\,\Omega$, and $V_{in} = 5.6\,V$. The diode shown in the circuit is an LED with $V_D = 2V$.

A.4.a) Suppose that $R_E = 50\,\Omega$. Determine the values of V_{CE}, I_E, I_C, and I_B. State and motivate whether the BJT is in the saturation, active, or cut-off region. (3 pt)

A.4.b) Determine what is the largest value of R_E so that the transistor is on saturation mode when it is conducting. (3 pt)

(Sub-Total A.4: 6pt)

A.5

Consider the filter in Fig. 4. Suppose that $V_{in}(t)$ is a sinusoidal voltage signal with $V_{in}(t) = 3\sin(10000\pi t + \frac{\pi}{2})$, i.e., amplitude 3, frequency 5000 Hz, and phase shift of $\frac{\pi}{2}$ rad. Using the methods of AC circuit analysis and complex impedances, derive the expression of the output voltage signal $V_o(t)$ for $R = 50\,\Omega$, $C = 1\,\mu F$, and $L = 1\,mH$, and classify this circuit as either a low-pass, high-pass, band-pass, or a band-stop filter.

(Sub-Total A.5: 6pt)

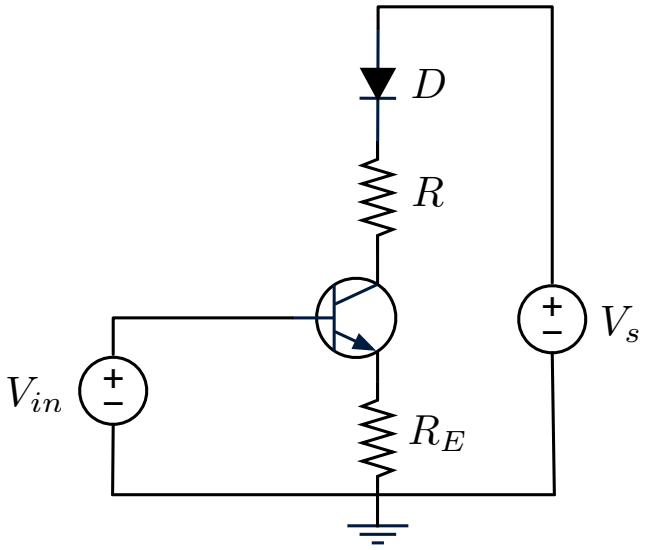

Figure 3: Circuit for Question A.4.

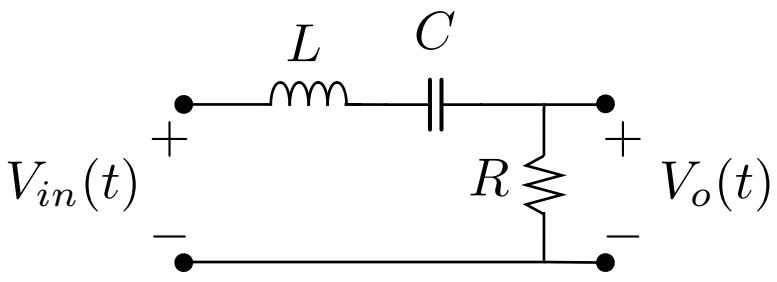

Figure 4: Circuit for Question A.5.

Part B

B.1

B.1.a) Consider the question A.3.a) and its circuit. Determine the equivalent resistance as seen from the terminals of the voltage source V_1. (3 pt)

B.1.b) Consider the amplifier circuit in Fig. 5, where $R_1 = 100\,\Omega$ and the two Zener diodes are identical and have $V_z = 5\,V$ and $V_d = 0.5\,V$. Let $V_{in}(t)$ be a sinusoidal voltage with amplitude $V_p = 7\,V$. Describe the behavior of the circuit, motivated by the operation of its components, and sketch the shape of the output voltage. (5 pt)

(Sub-Total B.1: 8pt)

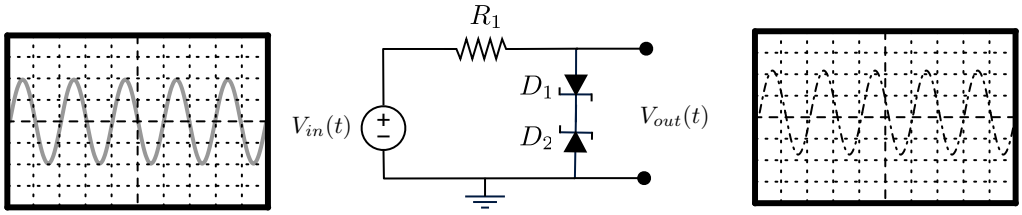

Figure 5: Circuit for Question B.1.b).

B.2

Design a **passive** band-stop (notch) filter using a **series circuit** of one resistor R, one capacitor C, and one inductor L, and **motivate** your design choice. If you wish to use given values for the components, then consider $L = 1\,mH$, $C = 1\,\mu F$, and $R = 50000\,\Omega$. Confirm that the design is according to the specifications by deriving the transfer function of the circuit, evaluating it for at least three different frequencies of your choice, and discussing the results obtained.
Note: the design of an active filter is also accepted, but it will incur in point deductions.

(Sub-Total B.2: 6pt)

B.3

In this question, you are asked to design a pseudo-random number generator that generates random numbers between 0 and 6 with the following probabilities:

Number	0	1	2	3	4	5	6
Probability	5/16	1/8	1/8	1/16	1/8	1/16	3/16

The circuit is to be controlled by two push-buttons (A and B) and a high-frequency clock. The generator is started by pressing button A, and no number is shown while it the circuit is running. The generator is stopped by pressing button B, at which point the chosen random number is displayed through a 4-bit output (y_3, y_2, y_1, y_0) during at least one clock cycle. A new number can be generated by repeating the process (press A to re-start, and B to pause and display the number).
The circuit is to be designed using D flip-flops. Draw the state diagram of a sequential network that displays the numbers with the desired probabilities. Given your design choice, indicate whether it is a Mealy or Moore type, and how many D flip-flops would be needed to implement your circuit. Motivate your answer! (Sub-Total B.3: 6pt)