EXAM

1TE717 Digital Technologies and Electronics
Faculty of Engineering Sciences

2023–08–14, 08:00 - 13:00

Location: Danmarksgatan 30, sektion 1

Aids: The following aids are allowed:

- Mathematics and / or Physics handbook,
- a small graphical calculator (e.g. TI-83 and similar),
- one A4 paper (two sides) with formulas or notes.

Note that exercise materials (exercise tasks, old exams, and solutions) are **NOT** allowed.

Observe: Do not treat more than one problem on each page and write a clear answer to each question. Each step in your solutions must be motivated. Lacking motivation will results in point deductions. Mark the total number of pages on the cover or first page

Grades: The *preliminary* grading criterium is

Grade 3: ≥ 4 points on each problem and total score of $20 - 29$ points.

Grade 4: ≥ 4 points on each problem and total score of $30 - 39$ points.

Grade 5: ≥ 4 points on each problem and total score of $40 - 50$ points.

Responsible: Isaac Skog, mobile phone 0708186805.

Good Luck!

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1 Assessed ILO: Analyse and design circuits with operational amplifiers for basic functions.

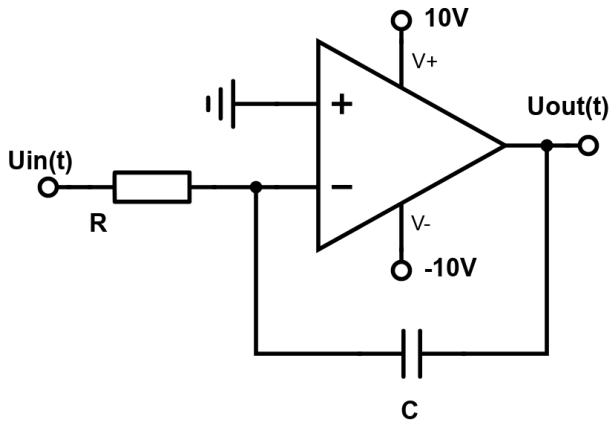

Figure 1: Circuit for problem 1.

Consider the circuit in figure 1. Assume that the OpAmp is ideal and do the following.

1.a) What is the maximum and minimum values that $U_{out}(t)$ can take on? (1 pt)

1.a) Derive an expression for $U_{out}(t)$ if $U_{in}(t) = \begin{cases} \alpha, & t \geq 0 \\ 0, & t < 0. \end{cases}$. (4 pt)

1.c) What mathematical operator does the circuit implement? (1 pt)

1.d) If $\alpha = -t$ $[V]$ and $R = 1$ $[M\Omega]$, select C so that output $U_{out}(t) = 4$ $[V]$ at $t = 2$ $[s]$. (4 pt)

2 Assessed ILO: Design and realise simple circuits with diodes and transistors.

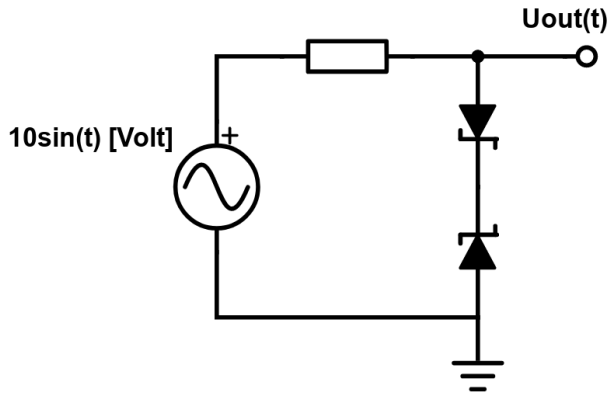

Figure 2: Circuit for problem 2a.

2.a) Consider the circuit in figure 2. The zener diodes has a zener voltage of 5 $[V]$ and a forward bias voltage drop of 0.7 $[V]$. Draw a figure of the output voltage as a function of time. (2 pt)

2.b) This problem is about using the transistor as a switch. Use two npn-transistors and as many resistor you want to design an NOR-gate.

- Draw the circuit diagram of your circuit. Make sure to specify the inputs and outputs of your circuit. (3 pt)
- Specify the values of the resistors in your circuit given the following component characteristics. Assume the circuit should work with 5V logics and the maximum input and output current of the NOR-gate is 1 mA. Further, assume that the transistor has a DC-gain $h_{FE} = 100$, a base-emitter saturation voltage $V_{BE}(sat) = 700\ [mV]$, a collector-emitter saturation voltage $V_{CE}(sat) = 100\ [mV]$, and a maximum allowed collector current $I_{c_{max}} = 10\ [mA]$. Moreover, for a logical high signal the voltage should be $\geq 4\ [V]$ and for a logical low signal the voltage should be $\leq 1\ [V]$. (5 pt)

3 Assessed ILO: Design combinatorial and sequential nets that implement given logical functions and state machines.

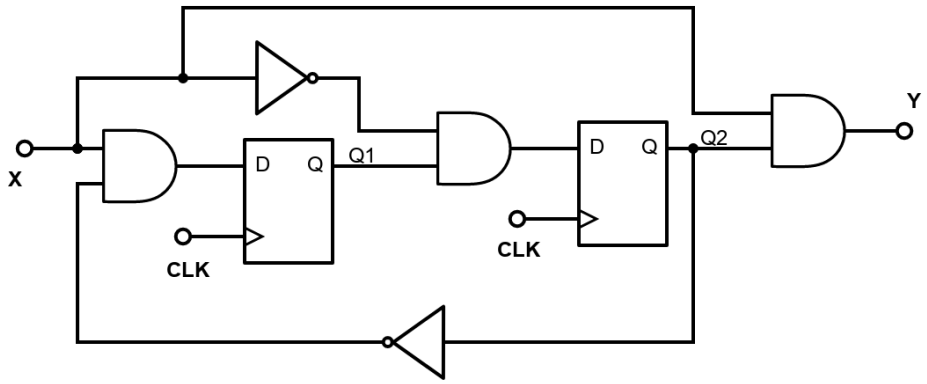

Figure 3: Circuit for problem 3.

Consider the state machine in figure 3, where X is the input and Y is the output.

3a) Is this a Mealy or Moore Machine? Motivate your answer. (1 pt)

3b) What is the maximum number of states of the machine? Motivate your answer. (1 pt)

3c) Specify a truth table that relates current state and input to the next state. (4 pt)

3d) Draw the state diagram for the circuit, which also indicates the output of the circuit. (3 pt)

3e) For which input sequence does the state-machine generate a logical true? (1 pt)

4 Assessed ILO: Use phasor diagrams and complex impedances for analysing circuits with capacitors and coils.

Consider the active filter in figure 4 and assume that input $u_{in}(t) = cos(\omega t)\ [V]$.

4.a) Determine the frequency function $H_{u_{in},u_{out}}(j\omega)$ from $u_{in}(t)$ to $u_{out}(t)$. (4 pt)

4.b) If $R_1 = 10\ [k\Omega]$, $R_2 = 1\ [k\Omega]$, $C_1 = 1\ [\mu F]$, what type of filter is this? (2 pt)

4.c) If $R_1 = 10\ [k\Omega]$, $R_2 = 1\ [k\Omega]$, $C_1 = 1\ [\mu F]$, what is the cut-off frequency of the filter? (1 pt)

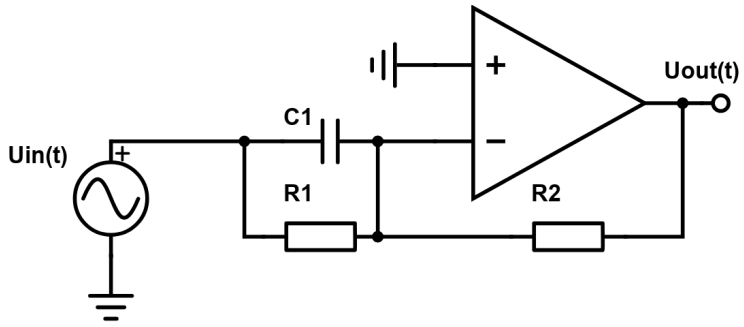

Figure 4: Circuit for problem 4.

4.d) Sketch the filter gain curve $20\log_{10}(|H_{u_{in},u_{out}}(j\omega)|)$ for $0 \leq \omega \leq 10^3$ $[rad/s]$. (3 pt)

5 Assessed ILO: Use circuit theory for analysing resistive nets and for designing such nets for basic signal conditioning.

5.a) Determine the current through the R_4 resistor in the circuit in figure 5. (4pt)

5.b) Determine the current through the 4 [Ω] resistor in the circuit in figure 6. (6pt)

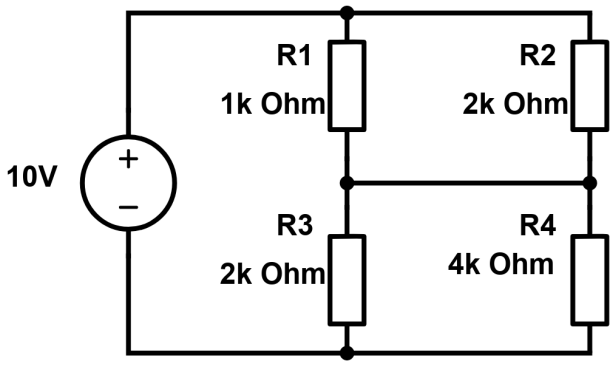

Figure 5: Circuit for problem 5a.

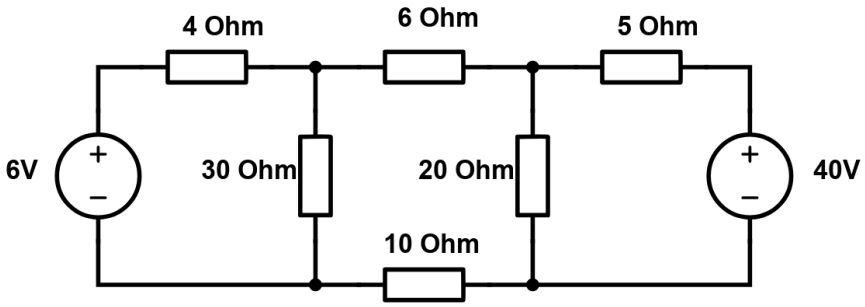

Figure 6: Circuit for problem 5b.