



1. Description

1.1. Project

Project Name	reflowOven
Board Name	STM32F407G-DISC1
Generated with:	STM32CubeMX 6.2.1
Date	04/25/2021

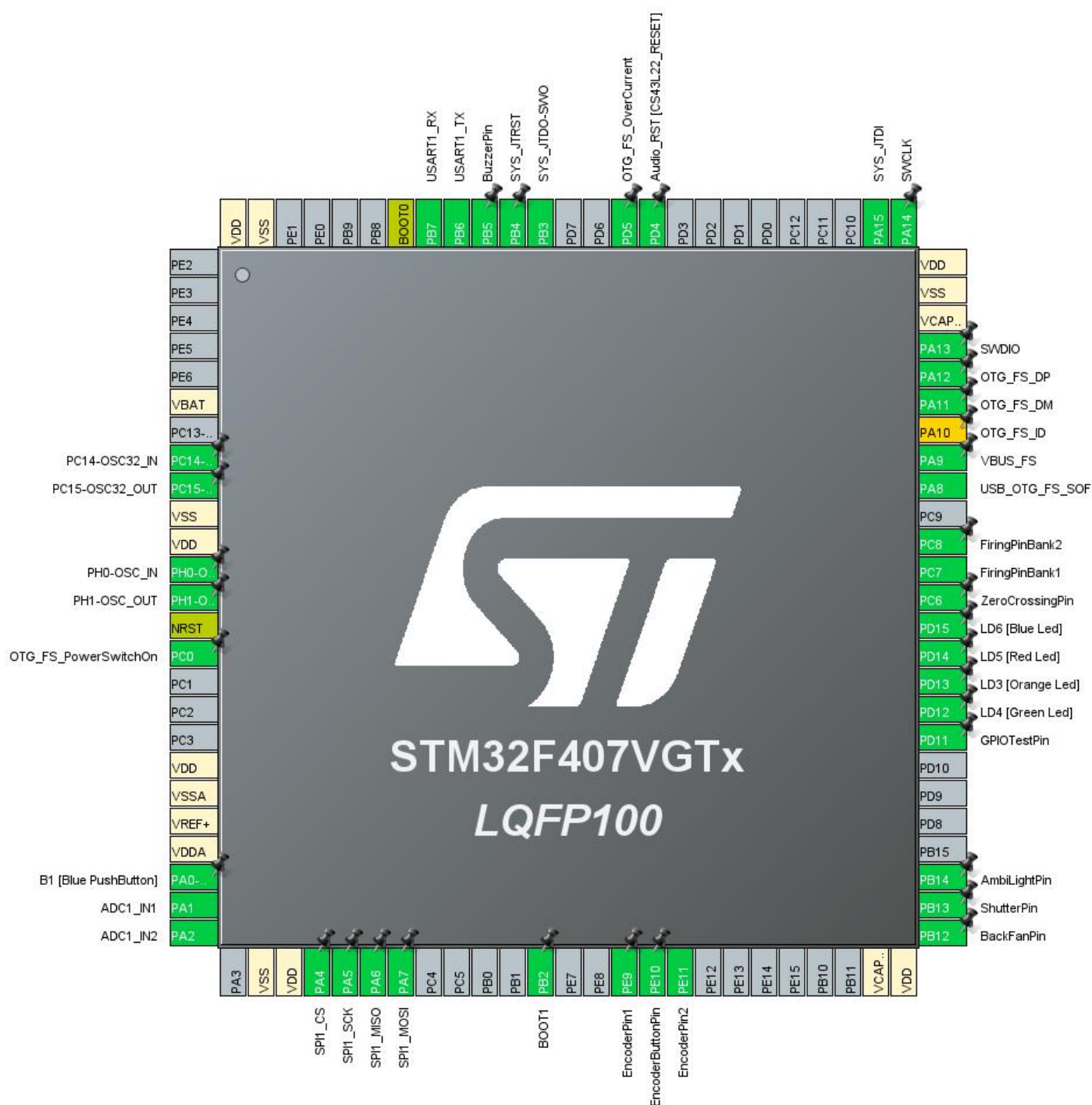
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F407/417
MCU name	STM32F407VGTx
MCU Package	LQFP100
MCU Pin number	100

1.3. Core(s) information

Core(s)	Arm Cortex-M4
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2. Pinout Configuration



3. Pins Configuration

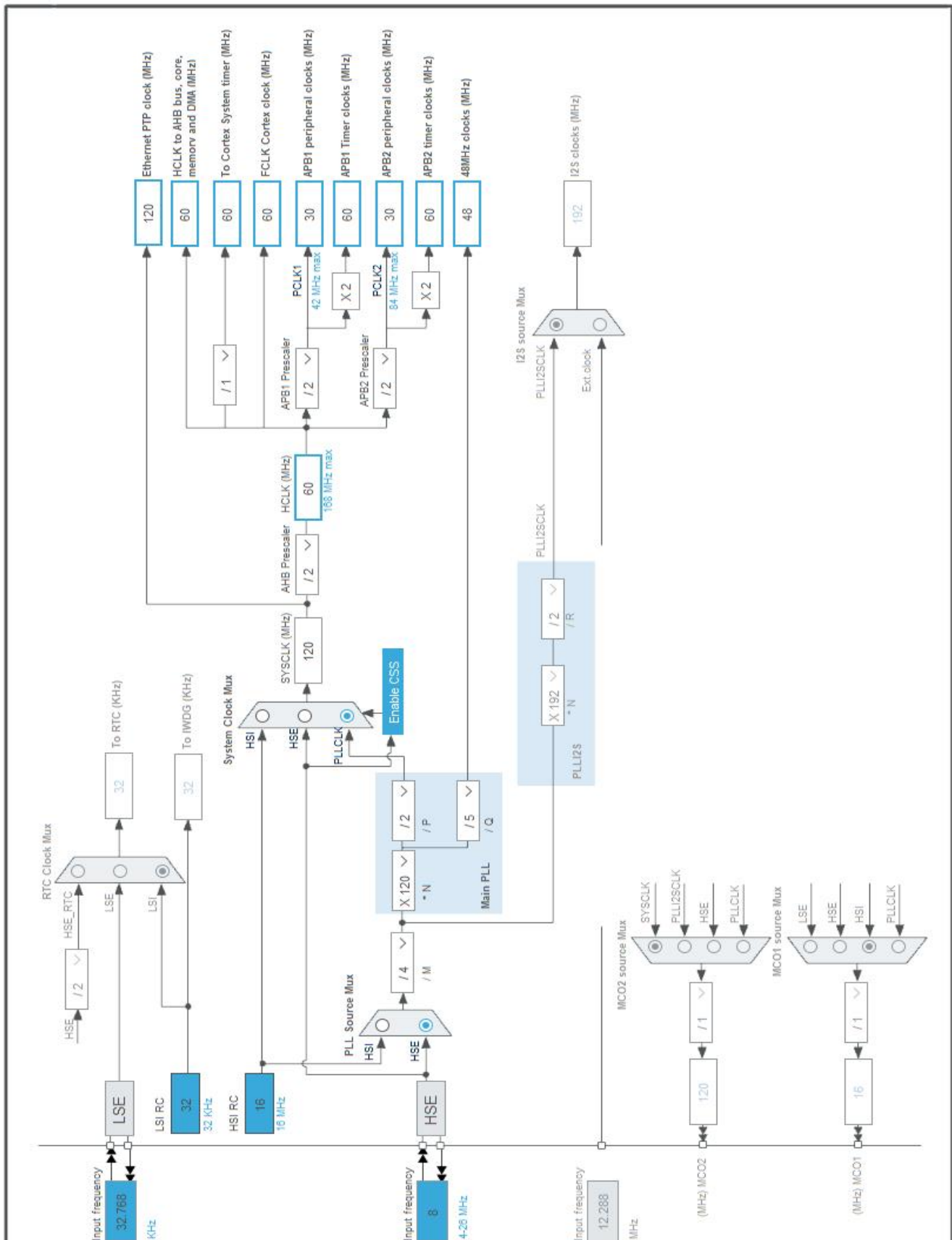
Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
8	PC14-OSC32_IN	I/O	RCC_OSC32_IN	PC14-OSC32_IN
9	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	PC15-OSC32_OUT
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN	I/O	RCC_OSC_IN	PH0-OSC_IN
13	PH1-OSC_OUT	I/O	RCC_OSC_OUT	PH1-OSC_OUT
14	NRST	Reset		
15	PC0 *	I/O	GPIO_Output	OTG_FS_PowerSwitchOn
19	VDD	Power		
20	VSSA	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP	I/O	GPIO_EXTI0	B1 [Blue PushButton]
24	PA1	I/O	ADC1_IN1	
25	PA2	I/O	ADC1_IN2	
27	VSS	Power		
28	VDD	Power		
29	PA4 *	I/O	GPIO_Output	SPI1_CS
30	PA5	I/O	SPI1_SCK	SPI1_SCK
31	PA6	I/O	SPI1_MISO	SPI1_MISO
32	PA7	I/O	SPI1_MOSI	SPI1_MOSI
37	PB2 *	I/O	GPIO_Input	BOOT1
40	PE9	I/O	TIM1_CH1	EncoderPin1
41	PE10 *	I/O	GPIO_Input	EncoderButtonPin
42	PE11	I/O	TIM1_CH2	EncoderPin2
49	VCAP_1	Power		
50	VDD	Power		
51	PB12 *	I/O	GPIO_Output	BackFanPin
52	PB13 *	I/O	GPIO_Output	ShutterPin
53	PB14 *	I/O	GPIO_Output	AmbiLightPin
58	PD11 *	I/O	GPIO_Output	GPIONTestPin
59	PD12 *	I/O	GPIO_Output	LD4 [Green Led]
60	PD13 *	I/O	GPIO_Output	LD3 [Orange Led]
61	PD14 *	I/O	GPIO_Output	LD5 [Red Led]
62	PD15 *	I/O	GPIO_Output	LD6 [Blue Led]

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
63	PC6	I/O	GPIO_EXTI6	ZeroCrossingPin
64	PC7	I/O	TIM3_CH2	FiringPinBank1
65	PC8	I/O	TIM3_CH3	FiringPinBank2
67	PA8	I/O	USB_OTG_FS_SOF	
68	PA9	I/O	USB_OTG_FS_VBUS	VBUS_FS
69	PA10 **	I/O	USB_OTG_FS_ID	OTG_FS_ID
70	PA11	I/O	USB_OTG_FS_DM	OTG_FS_DM
71	PA12	I/O	USB_OTG_FS_DP	OTG_FS_DP
72	PA13	I/O	SYS_JTMS-SWDIO	SWDIO
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	SWCLK
77	PA15	I/O	SYS_JTDI	
85	PD4 *	I/O	GPIO_Output	Audio_RST [CS43L22_RESET]
86	PD5 *	I/O	GPIO_Input	OTG_FS_OverCurrent
89	PB3	I/O	SYS_JTDO-SWO	
90	PB4	I/O	SYS_JTRST	
91	PB5 *	I/O	GPIO_Output	BuzzerPin
92	PB6	I/O	USART1_TX	
93	PB7	I/O	USART1_RX	
94	BOOT0	Boot		
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	reflowOven
Project Folder	C:\Users\mmitr\STM32CubeIDE\workspace_1.6.0\reflowOven
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.25.2
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_SPI1_Init	SPI1
4	MX_TIM5_Init	TIM5
5	MX_TIM1_Init	TIM1
6	MX_TIM2_Init	TIM2
7	MX_ADC1_Init	ADC1
8	MX_USART1_UART_Init	USART1
9	MX_TIM3_Init	TIM3
10	MX_USB_DEVICE_Init	USB_DEVICE

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F407/417
MCU	STM32F407VGTx
Datasheet	DS8626_Rev8

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

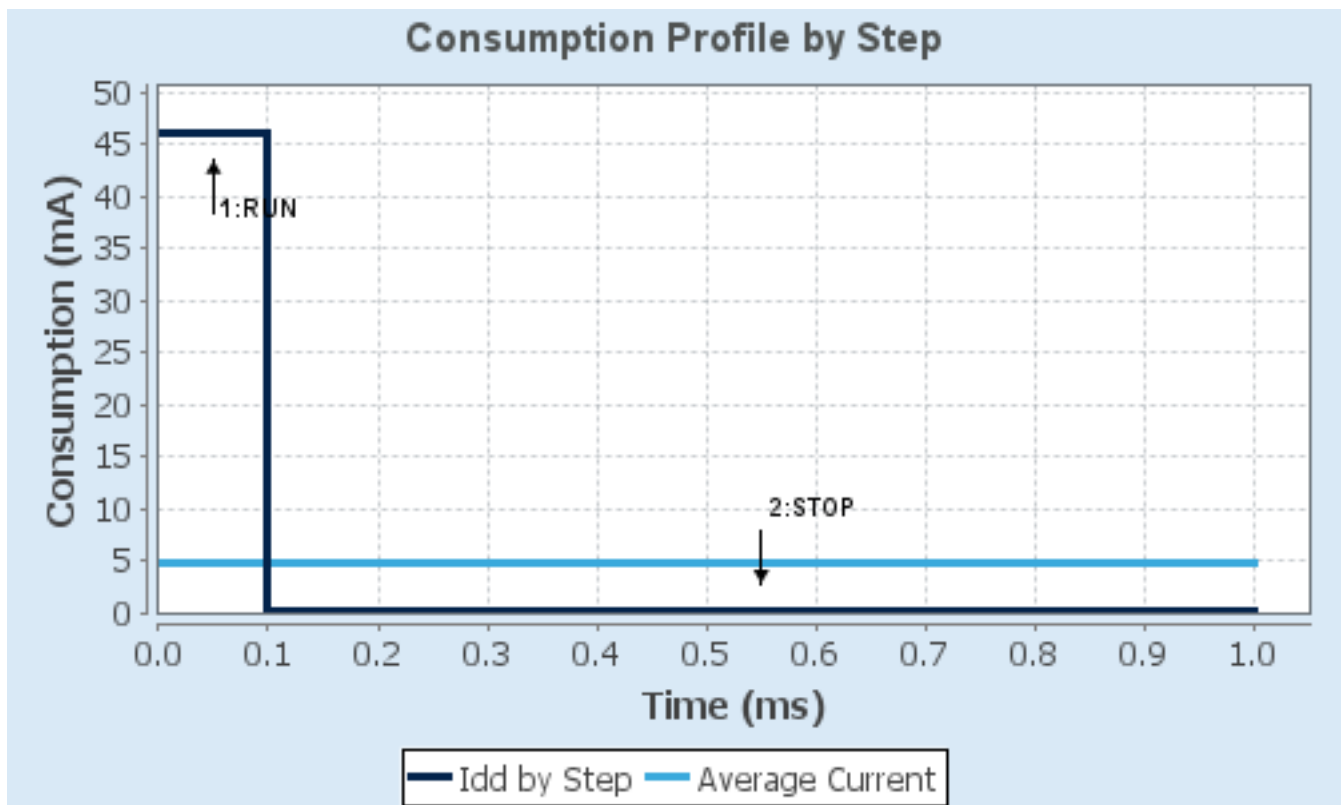
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	168 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	46 mA	280 μ A
Duration	0.1 ms	0.9 ms
DMIPS	210.0	0.0
Ta Max	98.47	104.96
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	4.85 mA
Battery Life	29 days, 4 hours	Average DMIPS	210.0 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. ADC1

mode: IN1

mode: IN2

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode
ADC_Settings:	
Clock Prescaler	PCLK2 divided by 2
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
<u>Rank</u>	1
Channel	Channel 1
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0
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WatchDog:

Enable Analog WatchDog Mode	false
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7.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled

Data Cache	Enabled
Flash Latency(WS)	1 WS (2 CPU cycle)
RCC Parameters:	
HSI Calibration Value	16
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000
Power Parameters:	
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.3. SPI1

Mode: Full-Duplex Master

7.3.1. Parameter Settings:

Basic Parameters:	
Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First
Clock Parameters:	
Prescaler (for Baud Rate)	256 *
Baud Rate	117.187 KBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge
Advanced Parameters:	
CRC Calculation	Disabled
NSS Signal Type	Software

7.4. SYS

Debug: JTAG (5 pins)

Timebase Source: SysTick

7.5. TIM1

Combined Channels: Encoder Mode

7.5.1. Parameter Settings:

Counter Settings:	
Prescaler (PSC - 16 bits value)	0

Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode

Encoder Mode TI1 and TI2 *

____ Parameters for Channel 1 ____

Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	10 *

____ Parameters for Channel 2 ____

Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	10 *

7.6. TIM2

Clock Source : Internal Clock

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	59999 *
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	1 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Update Event *

7.7. TIM3

Clock Source : Internal Clock

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	599 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	999 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Update Event *

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.8. TIM5

mode: Clock Source

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	59 *
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0xffffffff
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Update Event *

7.9. USART1

Mode: Asynchronous

7.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	9600 *
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.10. USB_OTG_FS

Mode: Device_Only

mode: Activate_SOF

mode: Activate_VBUS

7.10.1. Parameter Settings:

Speed	Device Full Speed 12MBit/s
Low power	Disabled
Link Power Management	Disabled
VBUS sensing	Enabled
Signal start of frame	Enabled

7.11. USB_DEVICE

Class For FS IP: Download Firmware Update Class (DFU)

7.11.1. Parameter Settings:

Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1

USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SUPPORT_USER_STRING_DESC (Enable user string descriptor)	Enabled
USBD_SELF_POWERED (Enabled self power)	Enabled
USBD_DEBUG_LEVEL (USBD Debug Level)	0: No debug message

Class Parameters:

USBD_DFU_MAX_ITF_NUM (DFU maximum interface numbers)	1
USBD_DFU_XFER_SIZE	1024
USBD_DFU_APP_DEFAULT_ADD (Base Address 0x)	0x08000000 *
USBD_DFU_MEDIA Interface	@Internal Flash /0x08000000/03*016Ka,01*016Kg,01*064Kg,07*128Kg,04*016Kg,01*064Kg,07*1

7.11.2. Device Descriptor:

Device Descriptor:

VID (Vendor Identifier)	1155
LANGID_STRING (Language Identifier)	English(United States)
MANUFACTURER_STRING (Manufacturer Identifier)	STMicroelectronics

Device Descriptor FS:

PID (Product Identifier)	57105
PRODUCT_STRING (Product Identifier)	STM32 DownLoad Firmware Update
CONFIGURATION_STRING (Configuration Identifier)	DFU Config
INTERFACE_STRING (Interface Identifier)	DFU Interface

* User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA1	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	
	PA2	ADC1_IN2	Analog mode	No pull-up and no pull-down	n/a	
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	PC14-OSC32_IN
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	PC15-OSC32_OUT
	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	PH0-OSC_IN
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	PH1-OSC_OUT
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPI1_SCK
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPI1_MISO
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	SPI1_MOSI
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	SWDIO
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	SWCLK
	PA15	SYS_JTDI	n/a	n/a	n/a	
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	
	PB4	SYS_JTRST	n/a	n/a	n/a	
TIM1	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	EncoderPin1
	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	EncoderPin2
TIM3	PC7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	FiringPinBank1
	PC8	TIM3_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	FiringPinBank2
USART1	PB6	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB7	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
USB_OTG_FS	PA8	USB_OTG_FS_SOF	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA9	USB_OTG_FS_VBUS	Input mode	No pull-up and no pull-down	n/a	VBUS_FS
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	Low	OTG_FS_DM
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	Low	OTG_FS_DP

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
Single Mapped Signals	PA10	USB_OTG_FS_ID	Alternate Function Push Pull	No pull-up and no pull-down	Low	OTG_FS_ID
GPIO	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OTG_FS_PowerSwitchOn
	PA0-WKUP	GPIO_EXTI0	External Event Mode with Rising edge trigger detection *	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI1_CS
	PB2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BOOT1
	PE10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	EncoderButtonPin
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BackFanPin
	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ShutterPin
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	AmbiLightPin
	PD11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIONTestPin
	PD12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD4 [Green Led]
	PD13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3 [Orange Led]
	PD14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD5 [Red Led]
	PD15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD6 [Blue Led]
	PC6	GPIO_EXTI6	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	ZeroCrossingPin
	PD4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Audio_RST [CS43L22_RESET]
	PD5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	OTG_FS_OverCurrent
	PB5	GPIO_Output	Output Open Drain *	Pull-up *	Low	BuzzerPin

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
EXTI line[9:5] interrupts	true	0	1
TIM1 break interrupt and TIM9 global interrupt	true	0	2
TIM2 global interrupt	true	0	1
USART1 global interrupt	true	0	0
TIM5 global interrupt	true	0	1
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM3 global interrupt	unused		
SPI1 global interrupt	unused		
USB On The Go FS global interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
EXTI line[9:5] interrupts	false	true	true
TIM1 break interrupt and TIM9 global interrupt	false	true	true
TIM2 global interrupt	false	true	true
USART1 global interrupt	false	true	true
TIM5 global interrupt	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

Middleware						
USB_DEVICE ✓						
Additional Software						
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing
DMA	ADC1 ✓	TIM1 ✓	SPH ✓			
GPIO ⚠		TIM2 ✓	USART1 ✓			
IVVIC ✓		TIM3 ✓	USB_FS ✓			
RCC ✓		TIM5 ✓				
SYS ✓						

10. Software Pack Report

10.1. Software Pack selected

Vendor	Name	Version	Component
ARM	CMSIS	5.7.0	Class : CMSIS Group : CORE Version : 5.4.0 Class : CMSIS Group : DSP Variant : Library Version : 1.8.0

11. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00037051.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00031020.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00037591.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00249778.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00024853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00025071.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040802.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040808.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00046011.pdf
Application note	http://www.st.com/resource/en/application_note/DM00050879.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00115714.pdf
Application note	http://www.st.com/resource/en/application_note/DM00123028.pdf

Application note http://www.st.com/resource/en/application_note/DM00129215.pdf

Application note http://www.st.com/resource/en/application_note/DM00154959.pdf

Application note http://www.st.com/resource/en/application_note/DM00160482.pdf

Application note http://www.st.com/resource/en/application_note/DM00213525.pdf

Application note http://www.st.com/resource/en/application_note/DM00220769.pdf

Application note http://www.st.com/resource/en/application_note/DM00257177.pdf

Application note http://www.st.com/resource/en/application_note/DM00272912.pdf

Application note http://www.st.com/resource/en/application_note/DM00226326.pdf

Application note http://www.st.com/resource/en/application_note/DM00236305.pdf

Application note http://www.st.com/resource/en/application_note/DM00263732.pdf

Application note http://www.st.com/resource/en/application_note/DM00281138.pdf

Application note http://www.st.com/resource/en/application_note/DM00296349.pdf

Application note http://www.st.com/resource/en/application_note/DM00327191.pdf

Application note http://www.st.com/resource/en/application_note/DM00354244.pdf

Application note http://www.st.com/resource/en/application_note/DM00373474.pdf

Application note http://www.st.com/resource/en/application_note/DM00315319.pdf

Application note http://www.st.com/resource/en/application_note/DM00380469.pdf

Application note http://www.st.com/resource/en/application_note/DM00395696.pdf

Application note http://www.st.com/resource/en/application_note/DM00431633.pdf

Application note http://www.st.com/resource/en/application_note/DM00493651.pdf

Application note http://www.st.com/resource/en/application_note/DM00536349.pdf

Application note http://www.st.com/resource/en/application_note/DM00725181.pdf