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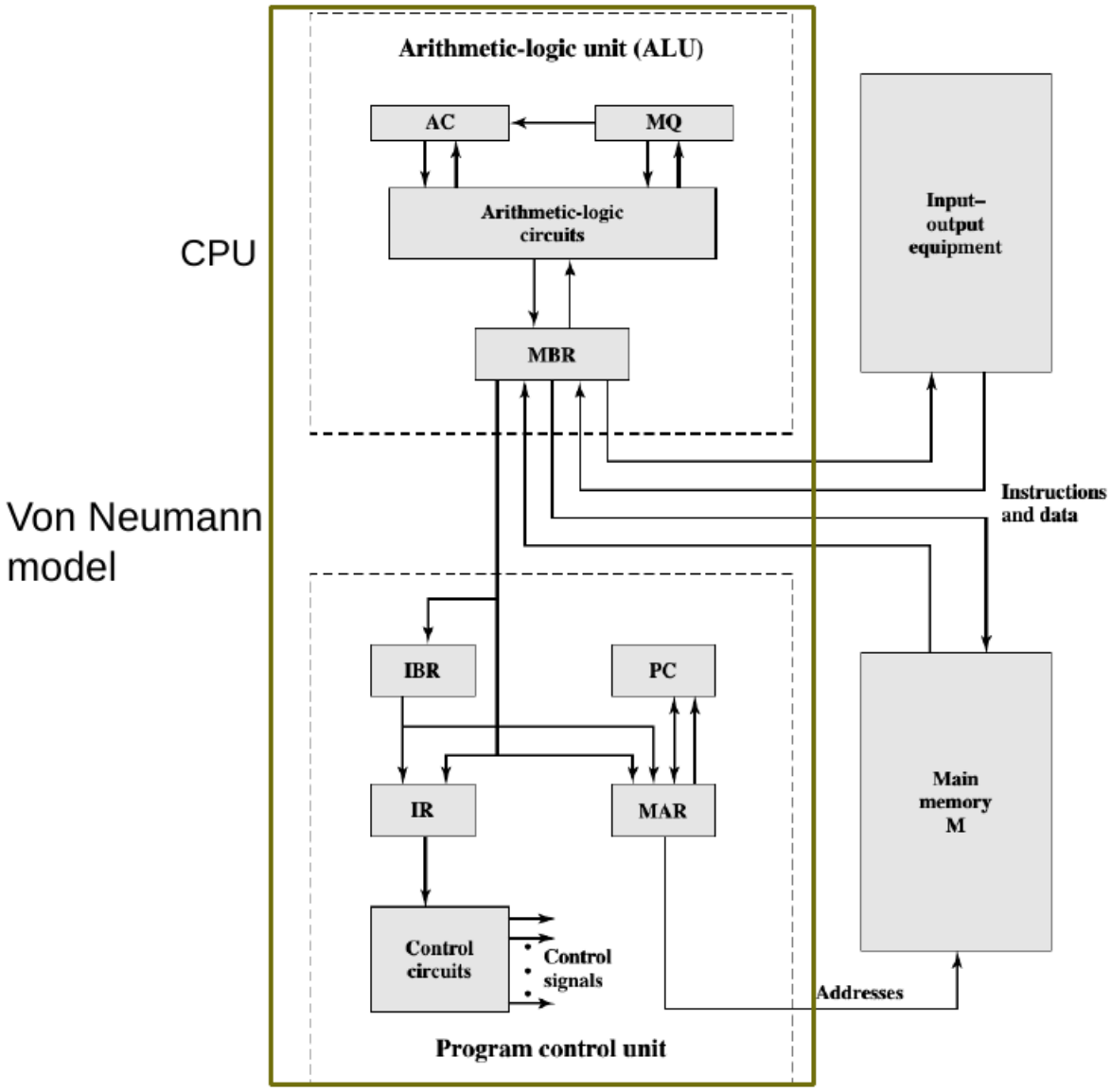
1 Fill in the blanks

1. Intel's embedded processor "embeds" the ..... MU ..... into the microprocessor.
2. One can fabricate ..... (microcontroller / microprocessor) by incorporating ..... modules to ..... (microcontroller / microprocessor).
3. If the computational resources: super computer, wearable, main frame, desktop, server, IoT, workstation are arranged in the ascending order of their computational power, then the order would be ..... wearables<iot<desktop<workstation<server<main frame<super computer
4. The harware realization of multiplier in a microcontroller / microprocessor is a ..... (architectural / organizational) issue.
5. Data bus most of the time is ..... (unidirectional / bidirectional) while the address bus is always ..... (unidirectional / bidirectional).
6. Major difference between the microcontroller and the microprocessor is .....
7. In the von Neumann architecture discussed in the class, the MBR handles a word of length ..... (20 or 40 bits). Similarly, IR ..... 8 ..... bits IBR ..... 20 ..... bits MAR ..... 12 ..... bits and finally PC ..... 12 ..... bits.
8. Output of IR is a ..... (address / control / data) signal.
9. The NXP LPC2378 ARM microcontroller is ..... 32 ..... - bit based muP embedded into microcontroller.
10. Issues or performance measures of whether a hardware multiplier implementation or software realization of multiplier algorithm in a microprocessor design, are ....., ..., ..., and .....
11. Given a memory word of 40 bits (corresponding to a row) and 1024 such rows are there, (a) how many bits are required to uniquely identify a memory word? (b) size of memory in bits?

2 Answer the following

1. Browse in the internet for a commercial processor which has also FPGA "embedded" in it.
2. What is the difference between computer organization and architecture?
3. What is a program counter? What does it count?
4. What is the difference between system bus and internal bus in a microprocessor?
5. Why is that the when the CPU frequency increases, heat dissipated also increases?
6. Describe the Von Neumann architecture with a block diagram and explain its operation. Indicate the bus size in each of the buses out there.
7. What is the major difference between Von Neumann architecture and Harvard architecture?

8. Recall the van Neumann computer hardware architecture, which is given before for convenience.



Answer the following

data bus, 40,

(a) What is the type of bus which connects MBR from main memory? What is the size of the bus? (Meaning, how many bits does the bus possess?). What are two main types of data it can carry?

(b) Repeate (a) with direction changed.

(c) What is fed to IR block? How many bits does it have?

(d) Can MAR has something to send to PC? On the other hand, what does PC send to MAR? What is the type of bus? And its size?

(e) What type of bus is used to connect MAR to main memory? What is its size?

(f) Given that the number of rows in the main memory is 1000, and each row contains 40 bits, what is the size of memory in bytes?

(g) Given that all the instructions are of constant length (RISC feature), of 20 bits, how many instructions are accommodated in a row in the main memory (in the program area)?

(h) Consider the algorithmic part - flow chart - of van Neumann model. Where is that the IBR is declared 'empty', so that the condition testing block (at the top) can use that information? Indicate it in the flow chart.

9. Recall the von Neumann computer introduced in the class. The following Fig 1 gives the execution of instructions, in which MAR & MBR are implicit. In the following Figure, one needs to include a nibble 0 in the MSB of word

corresponding to AC and IR. While the address bits are 12, the word stored in memory is also increased by 4 bits leading to 20 bit memory word. While the accumulator AC (having 20 bits in length), corresponds to MBR, the 20 bit word below it, in each step, corresponds to IR (MSB 8 bits) and MAR (LSB 12 bits). For example read, "|1|9|4|0| IR" as "|0|1|9|4|0| IR MAR" wherein the LSB 12 bits (0x 940) are MAR contents and MSB 8 bits (0x 01) are IR contents. Only a generic instruction (it can be left or right instruction) is shown. AC length is also 20 bits (or 5 nibbles in length).

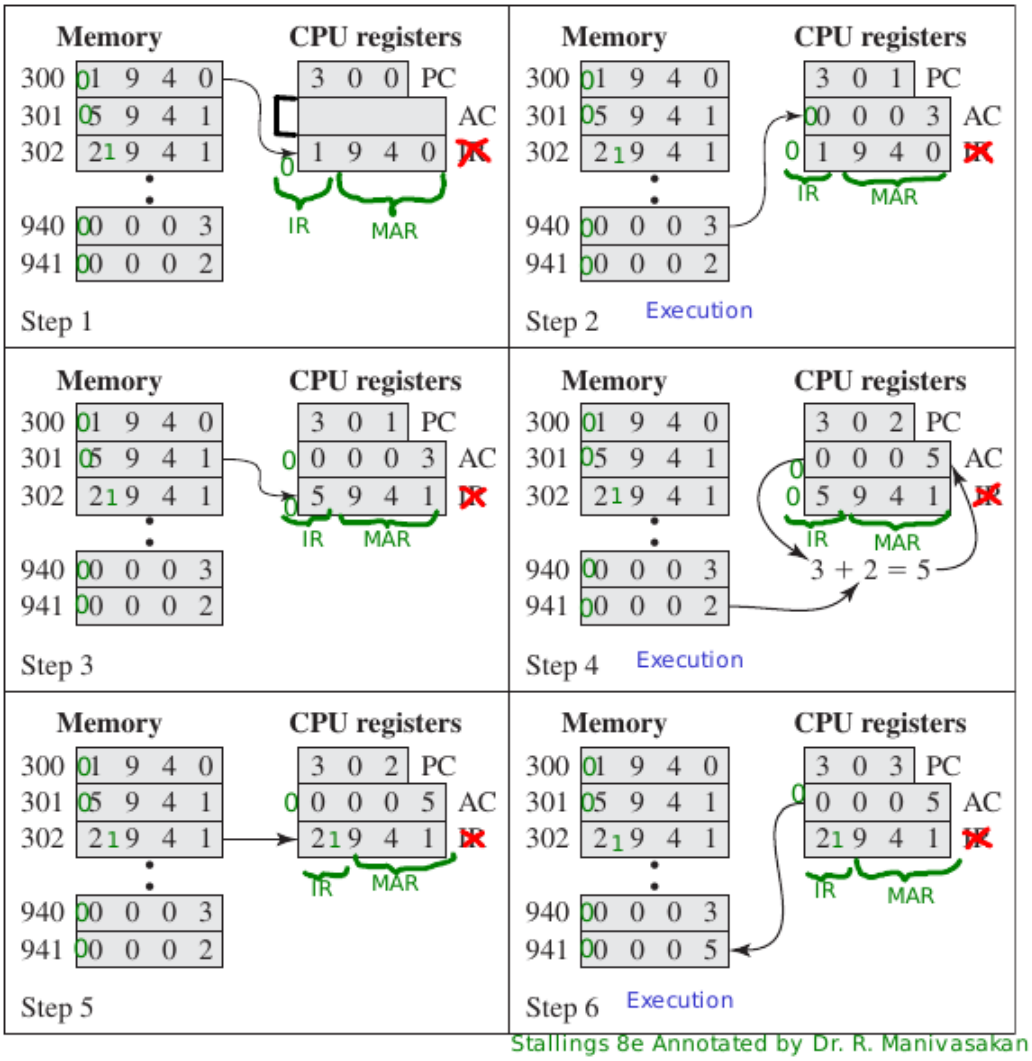


Fig 1: A program showing its execution in van Neumann's computer.

Following table gives the ISA for van Neumann first stored program computer.

Instruction Type	Opcode	Symbolic Representation	Description
Data transfer	00001010	LOAD MQ	Transfer contents of register MQ to the accumulator AC
	00001001	LOAD MQ,M(X)	Transfer contents of memory location X to MQ
	00100001	STOR M(X)	Transfer contents of accumulator to memory location X
	00000001	LOAD M(X)	Transfer M(X) to the accumulator
	00000010	LOAD −M(X)	Transfer −M(X) to the accumulator
	00000011	LOAD |M(X)|	Transfer absolute value of M(X) to the accumulator
	00000100	LOAD −|M(X)|	Transfer −|M(X)| to the accumulator
Unconditional branch	00001101	JUMP M(X,0:19)	Take next instruction from left half of M(X)
	00001110	JUMP M(X,20:39)	Take next instruction from right half of M(X)
Conditional branch	00001111	JUMP+ M(X,0:19)	If number in the accumulator is nonnegative, take next instruction from left half of M(X)
	00010000	JUMP+ M(X,20:39)	If number in the accumulator is nonnegative, take next instruction from right half of M(X)
Arithmetic	00000101	ADD M(X)	Add M(X) to AC; put the result in AC
	00000111	ADD |M(X)|	Add |M(X)| to AC; put the result in AC
	00000110	SUB M(X)	Subtract M(X) from AC; put the result in AC
	00001000	SUB |M(X)|	Subtract |M(X)| from AC; put the remainder in AC
	00001011	MUL M(X)	Multiply M(X) by MQ; put most significant bits of result in AC, put least significant bits in MQ
	00001100	DIV M(X)	Divide AC by M(X); put the quotient in MQ and the remainder in AC
	00010100	LSH	Multiply accumulator by 2; i.e., shift left one bit position
	00010101	RSH	Divide accumulator by 2; i.e., shift right one position
Address modify	00010010	STOR M(X,8:19)	Replace left address field at M(X) by 12 rightmost bits of AC
	00010011	STOR M(X,28:39)	Replace right address field at M(X) by 12 rightmost bits of AC

(a) List the instructions used in program shown in Fig 1 above.

(b) Quantitatively evaluate the value of MAR in each clock cycle (steps 1 to 6 as shown above).

(c) What is the role of AC here?

10. The stray capacitance, frequency and supply voltage, in an intel microprocessor chip and an AVR microcontroller chip, respectively are given as below:

    (a) intel processor chip 10 nF, 1.72 V and frequency 6 GHz power.

    (b) AVR microcontroller chip 5 V, 100 pF operating at 1 MHz (0.25 W).

    Given the above, answer the following:

    (a) Compute the heat (dynamic power) generated (which is to be removed or dissipated by cooling mechanism)

    (b) What is the heat removing rate (in J/sec) to be implemented by the cooling mechanism for each of the above, so that temperature of the chip doesnt increase?

    (c) While, any heat generated, less than a watt could be ignored (meaning, the heat generated, would either be naturally be dissipated or would not raise the temperature of the chip substantially), which of the above (intel processor or AVR microcontroller) doesnt need any cooling mechanism.

11. Consider a 64-bit intel processor having a 32-bit address bus, with 4 control lines (corresponding to RD/WR, chip enable etc) is proposed to be connected to the main memory (housing program and data) through (a) van Neumann architecture (b) Harvard architecture. Compute the total number of wire-traces (system bus width) to be used in each of the above cases. Give the corresponding picture. [Note that this problem concerns only the part of the system bus which connects to memory, not the part connecting to I/O].