EE2016 Microprocessors Theory and Lab, Aug - Nov 2024.

Tutorial 2 (Classes on 12, 13, 19 & 20th of August 2024)

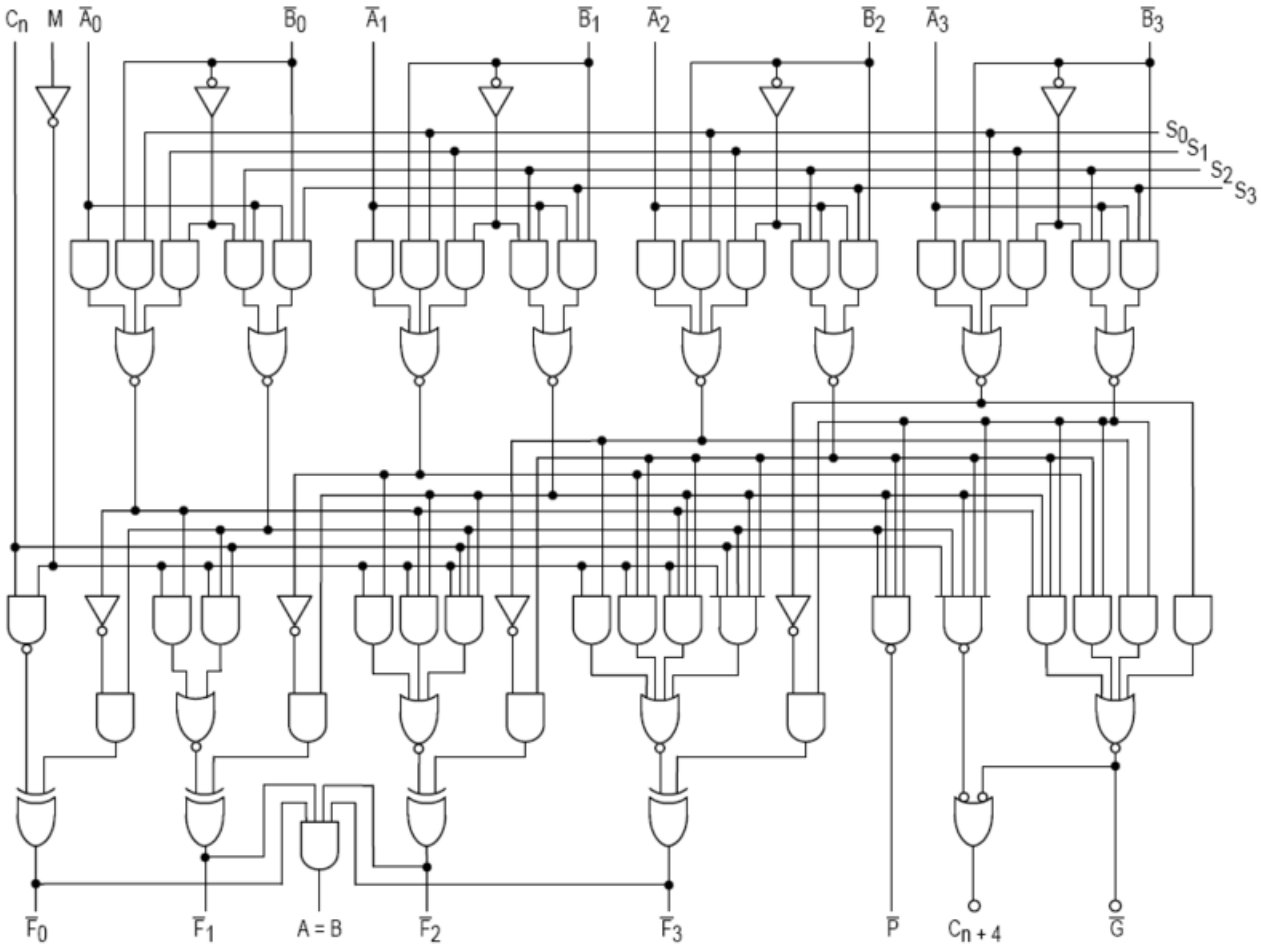
Dr. R. Manivasakan, EE Dept, IIT Madras.

1 Fill in the blanks

1. The most common processor instruction (which occurs 90 % of the time) is .... (data flow / addition / Ex-OR / multiplication).
2. The output of two or more gates should not be connected together, because ..short circuit..... .
3. Tri-state gates are solutions to ..short circuit due to connection of 2 or more outputs
4. A single bit data bus interfacing the N (N>3) flip-flops is created by ..... while the control signals involved are ..rd and wr..... To transmit data from one FF to another, the procedure is ..... connecting the outputs and inp of all ff together
5. The purpose of buffer registers connected to data bus is to ..temp data str
6. In N (=16) 8-bit registers connected through 8-bit data bus, the width of address bus is ..4....., width of data bus is ..8.....
7. Security of the processor is more in ..... (Harvard / von Neumann architecture) and the reason(s) is (are) ..sep storage for program
8. AVR microcontroller complies to ..Harvard..... (Harvard / von Neumann architecture). Hence, the program memory and data are stored in the ..dif..... same / different memory location.
9. The purpose of the functions lines in ALU is to select specific oper. Function lines are generated by ..cu.....
10. Exactly 1 KB means ..1024..... bytes.
11. The binary and decimal equivalent of hex numbers 0x 2B9H is ..... and .....001010111001 and 697
12. In Load / Store architecture (LSA) apart from LD and ST instructions other instructions ..can't..... (can also / can't) access the memory.
13. In LSA, ... (either one or both or none of) the operands ..... (can / can't) be from main memory.
14. In register-memory architecture (RMA), ... (either one or both or none of) the operands ..... (can / can't) be from main memory.
15. Which of the following is (are) volatile? (a) SRAM, (b) EEPROM (c) DRAM (d) NV-RAM
16. The memory used for microprocessor cache is ..RAM..... Harvard
17. The split-cache hardware architecture is microcomputer design in which ..... (mention how the program memory and data memory are handled).
18. Of the instructions (a) ADD R0, R1 (b) MOV R15, R16 (c) LDI R0, K ..b,c..... is (are) data transfer operation(s), ..a.. is (are) ALU arithmetic operation(s) ..... is (are) ALU logical operation(s).

2 Answer the following

1. A 512K memory chip has 8 pins for data. Find
   (a) the organization (meaning, how many words versus word length) and 524288
   (b) the number of address pins for this memory chip 19
2. In a given byte-addressable microcomputer, memory locations 0x 10000 to 0x 9FFFF are available for user programs. The first location (address) is 0x 10000 and the last location (address) is 0x 9FFFF. Calculate,
   (a) the total amount of memory (in bytes) available for user programs 9FFFF-10000+1= 9*16^4
   (b) the word length 8
   (c) the size of address bus 4+4+4+4+4= 20
   (d) the size of data bus 8
3. Consider a flip-flop. Assume active high logic. Can the control signal "WR / latch enable" and "RD enable", both high at the same time? Both of them low at the same time? no
4. How is a single 8-bit register built out of flip-flips? Show the control lines to the register and show how is it connected to RD & WR of the individual flip-flops. Mark the data lines.
5. Given a set of n $(= 2^m)$ registers (each of (word) length k bits) for some $m = 0, 1, 2, \ldots,$
   (a) What is the memory size in bits? And in bytes when $k = 8$? kn ,8n/8
   (b) What is the minimum number of address bits necessary to pick an unique register from the above set? m
   (c) Evolve an addressing scheme which uses minimum bus size. Show the digital circuit derived indicating the TT if any, at all used in the design. decoder
   (d) Give an overall block diagram indicating the various units used in (b) above viz., register bank, address bus, data bus and control lines / bus. Indicate the size of each bus. n, m, k, 4
   (e) Instead of separate "WR / latch enable" and "RD enable" physical wireline, what if one has a single physical line along with the 'rule', READ for logical 'low' and WR for logical 'high'. What are the pros and cons of such a scheme? both wont be enabled at the same time, single control line,: either one should be functioning
   (f) Explain how the steps involved in instruction MOV Rd, Rs when executed, by using the above block diagram. Here, Rd & Rs are registers of size l bits. Identify the physical path of the digital signal journey. contents from rs goes to rd
   (g) Show the timing diagram of execution of the instruction in (d). [Timing diagram has not been taught in the class and hence this is optional].
6. Consider a 8-bit processor in which the data bus is connected to internal 8-bit registers whose address range from 0x 0000 till 0x FFFF.
   (a) Show the block diagram as well as circuit diagram of the above system, showing the registers, data bus, control lines and address bus. Indicate quantitatively the various system parameters.
   (b) What is the word length here? What is the size of address bus and data bus?
   (c) Show the hardware level steps to execute the instruction `MOV R0, R1`, given that the registers R0 & R1 are at addresses `0x 0000 & 0x 0001` respectively. Show the control signals, timing diagram in the digital schematic of memory, address bus, data bus and control lines.
7. Shown below is the circuit diagram of 1960's famed 4-bit ALU 74181 MSI.



Consider the following table of inputs:

					Active-high logic	Active-high logic
	S_3	S_2	S_1	S_0	Logic $(M = 1)$	Arithmetic $(M = 0)(C_n = 1)$
	0	0	0	1	output F = ?	output F = ?
	0	1	1	0	output F = ?	output F = ?
	1	0	0	1	output F = ?	output F = ?
	1	1	0	0	output F = ?	output F = ?

Assuming active-high logic, enter the value of $F_3F_2F_1F_0$ in terms of $A_3A_2A_1A_0$ and $B_3B_2B_1B_0$ for the cases given in the above table. You could use the short hand notation of A for $A_3A_2A_1A_0$. Give the pathway of the digital signal as it traverses from the input to output.

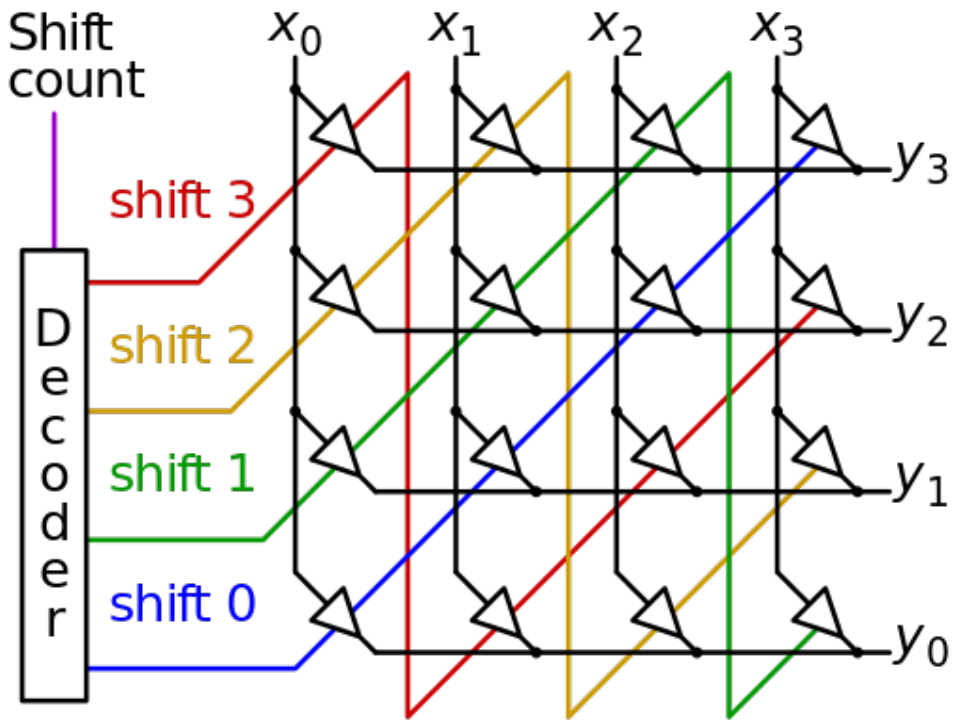
8. Floating Point Unit (FPU):

   (a) Given the two positive floating point numbers (in IEEE 754 format), $N_1 = c_1 \times 10^{q_1}$ and $N_2 = c_2 \times 10^{q_2}$, give the table containing addition, subtraction, multiplication and division operations on these numbers.

   (b) Build an FPU unit, specify the internal circuitry of adder, subtractor, multiplier and specify the and internal interconnection using various internal bus.

9. Barrel shifter:

   The anatomy of a 4-bit crossbar barrel shifter is given below:



Consider the clock interval is T_{clk} secs.

(a) The above crossbar barrel shifter circuit is supposedly to be a combinational circuit. Redraw the above diagram with ALL elements being explicitly expressed as digital logic gates (**Hint:** Strictly speaking the diodes here, doesnt make a logical gate. It is just a symbolic representation that the output of decoder controls the diode, whether to pass the digital data from input (column) to output (row). [Diode representation is from the crossbar terminology used in telephony]. Replace the diodes by a suitable logic circuit with the output of the decoder plus the input (X_i). Take care of the problem of connecting together the output of more than one digital gate or FF or combination thereof].

(b) Given the 4-bit shifter implemented through a sequence of FFs, compare the performance of barrel shifter for time it takes for 3-bit shift, with the time taken by 4-bit FF shifter for the same job.

(c) Mention the type of shifter circuit is the above barrel shifter? Shift right or left or rotate left or rotate right? Can you modify the one above (whatever type) to the other type? If you think it is possible, redraw the modified circuit. If you think it is NOT possible, then give reasons, why it is not possible.

(d) Can we modify the above circuit to implement the following

i. shift right
ii. shift left
iii. arithmetic shift right
iv. arithmetic shift left
v. left logical shift
vi. right logical shift
vii. left rotate through carry (carry is assumed available)
viii. right rotate through carry (carry is assumed available)