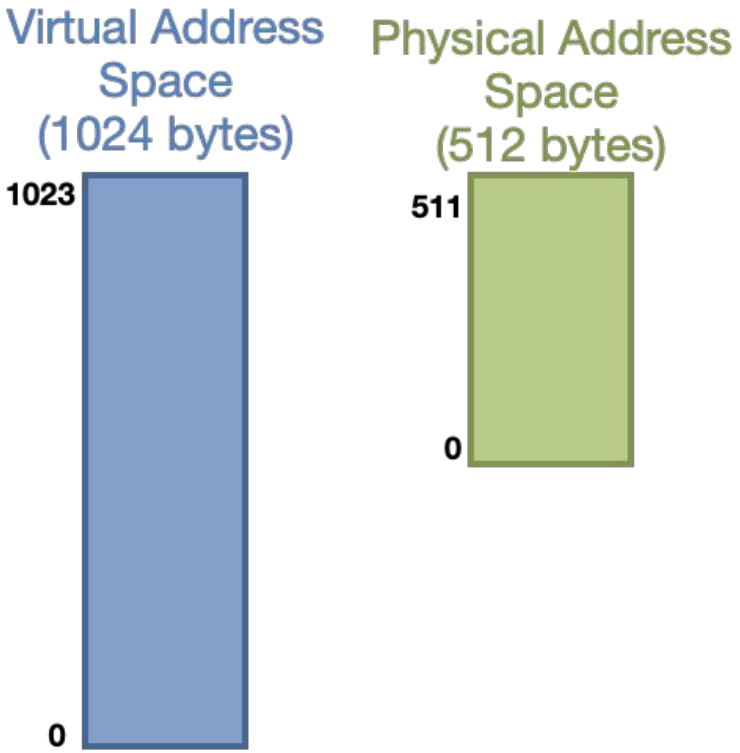
Lab 10

CS61C

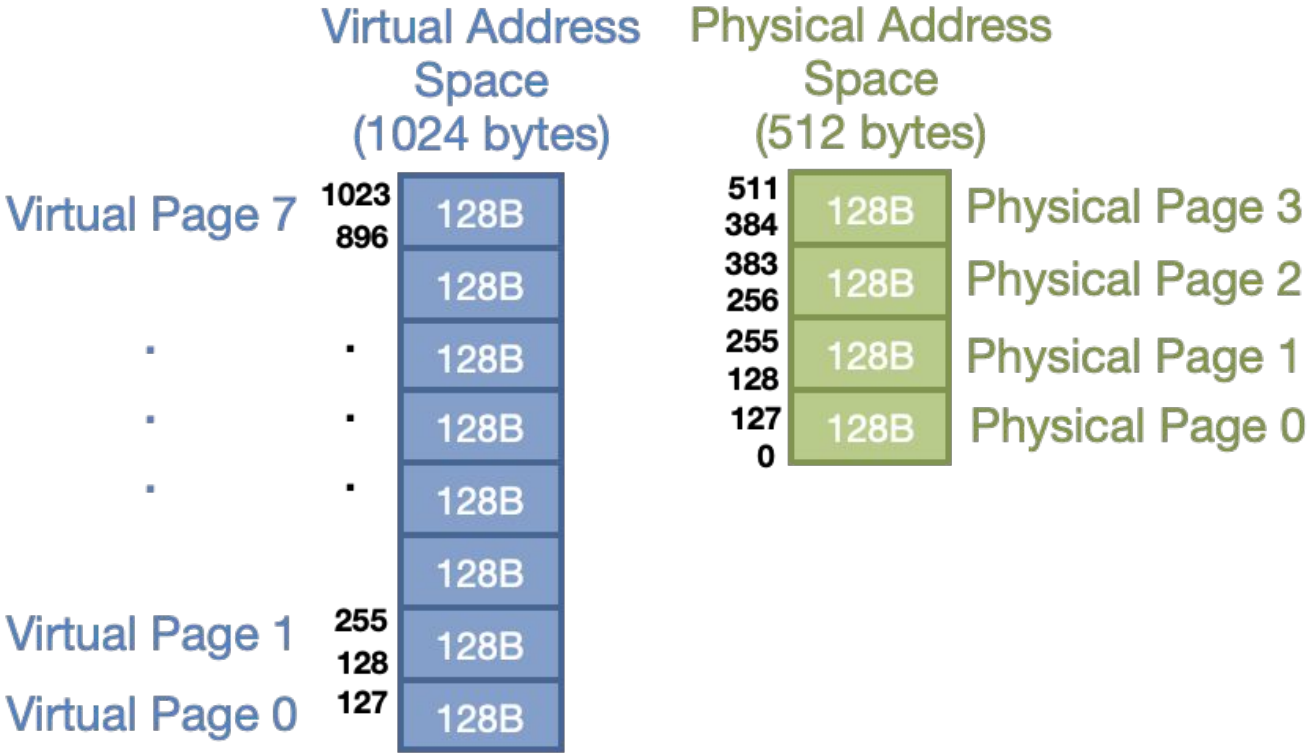
Virtual Memory

- Why do we have virtual memory?
  - Our RAM is not big enough to hold all of the data that we need at one time
  - Our program needs to “think” that the data is contiguous
    - When you are writing a program, you don’t know where it will be stored in memory
    - So we just pretend like the memory is contiguous and then the virtual memory takes care of everything in the background
  - Protection between processes

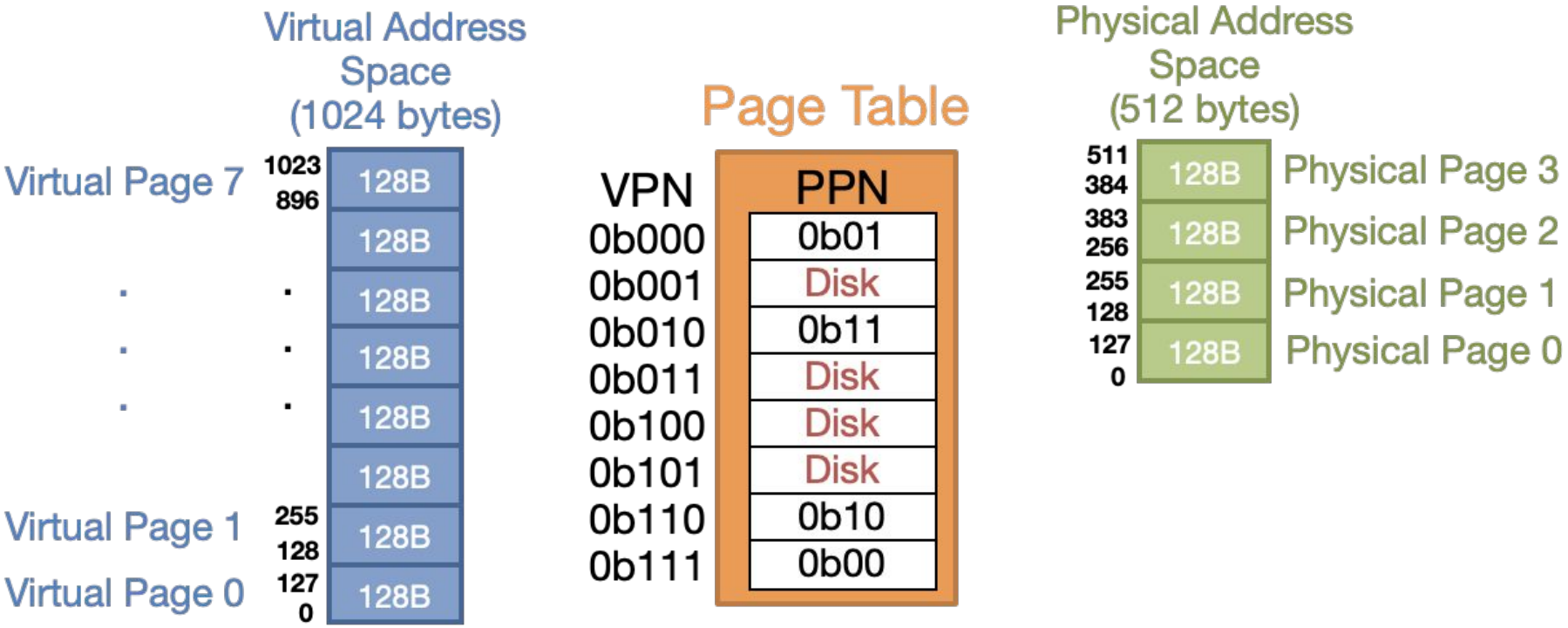
Virtual Memory



Virtual Memory



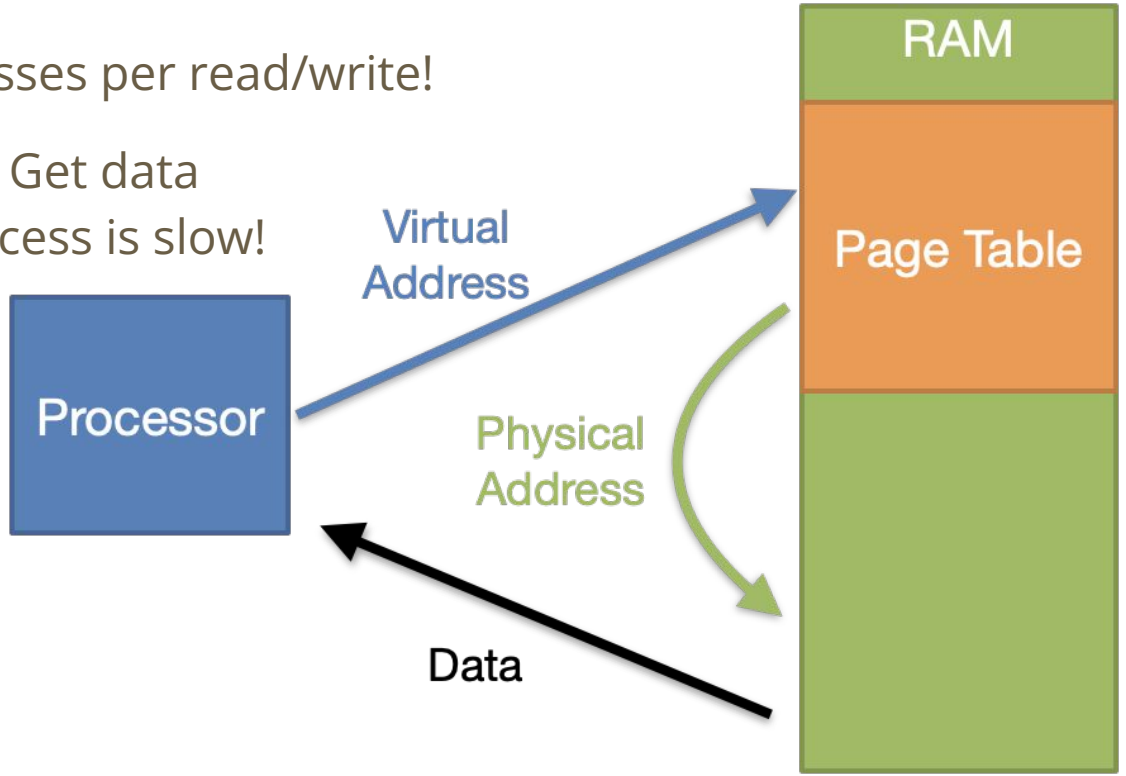
Virtual Memory



Virtual Memory

2 main memory accesses per read/write!

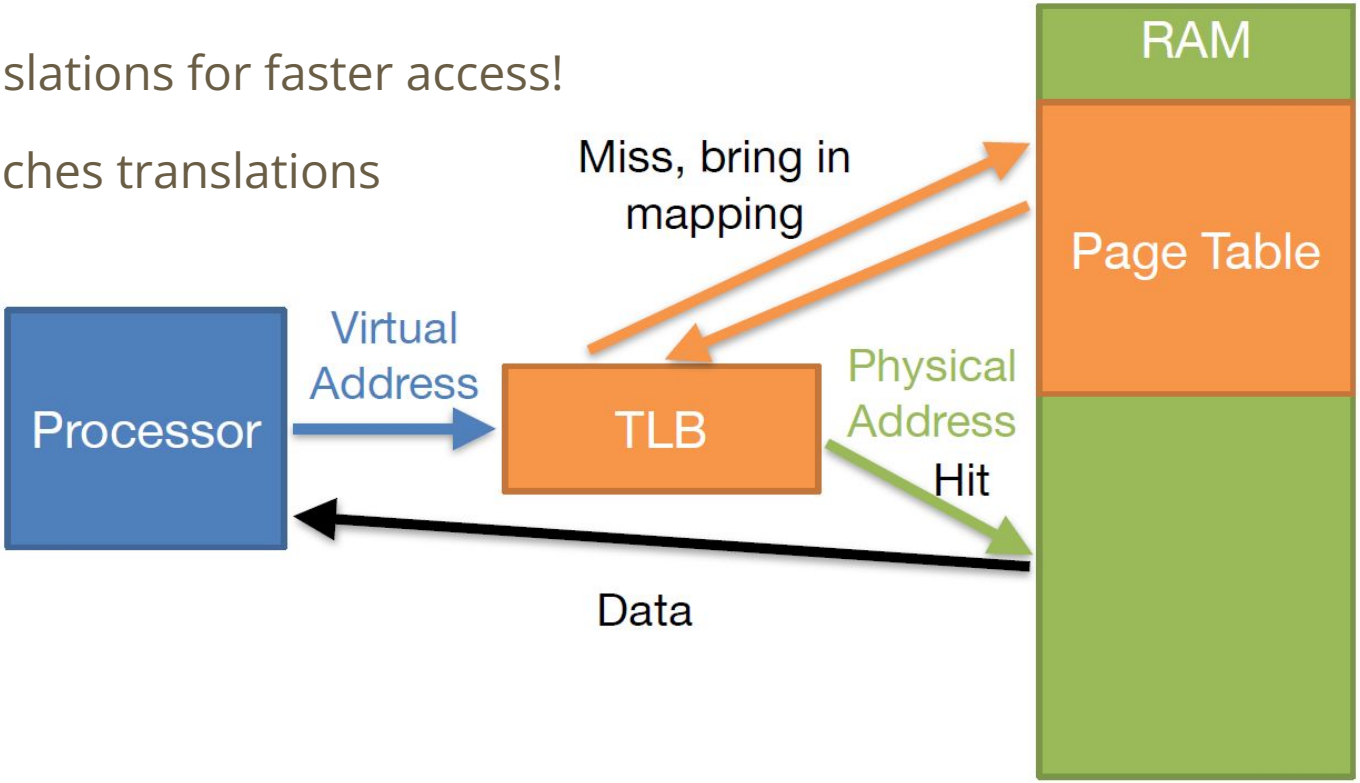
- Get translation + Get data
- Main memory access is slow!



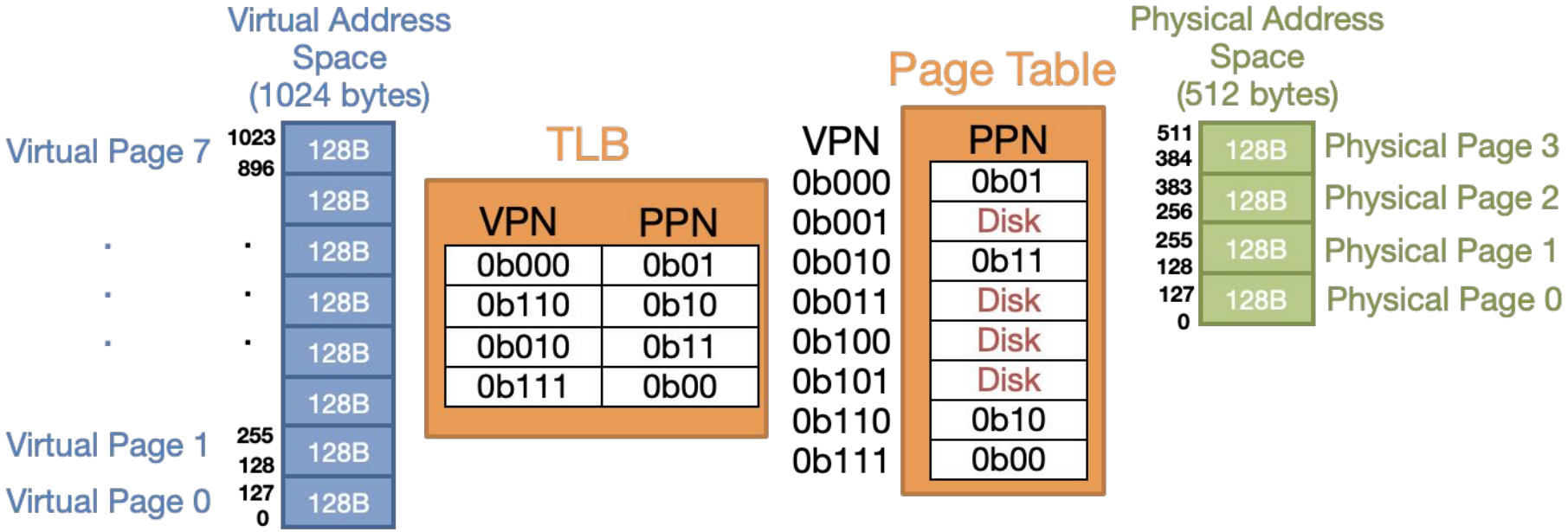
Virtual Memory

Cache translations for faster access!

- TLB caches translations



Virtual Memory



Do Exercise 1

Do Exercise 2

Exercise 2 Example

Address	Virtual Page Number	Offset
0x01	0x0 (000)	0x1 (00001)
0x22	0x1 (001)	0x2 (00010)
0x43	0x2 (010)	0x3 (00011)
0x64	0x3 (011)	0x4 (00100)
0x85	0x4 (100)	0x5 (00101)
0xA6	0x5 (101)	0x6 (00110)
0xC7	0x6 (110)	0x7 (00111)
0xE8	0x7 (111)	0x8 (01000)
0x09	0x0 (000)	0x9 (01001)
0x20	0x1 (001)	0x0 (00000)

What is the main requirement to force a TLB miss?

For CAMERA, why is a TLB miss automatically a page fault?

Do Exercise 3

Do Exercise 4

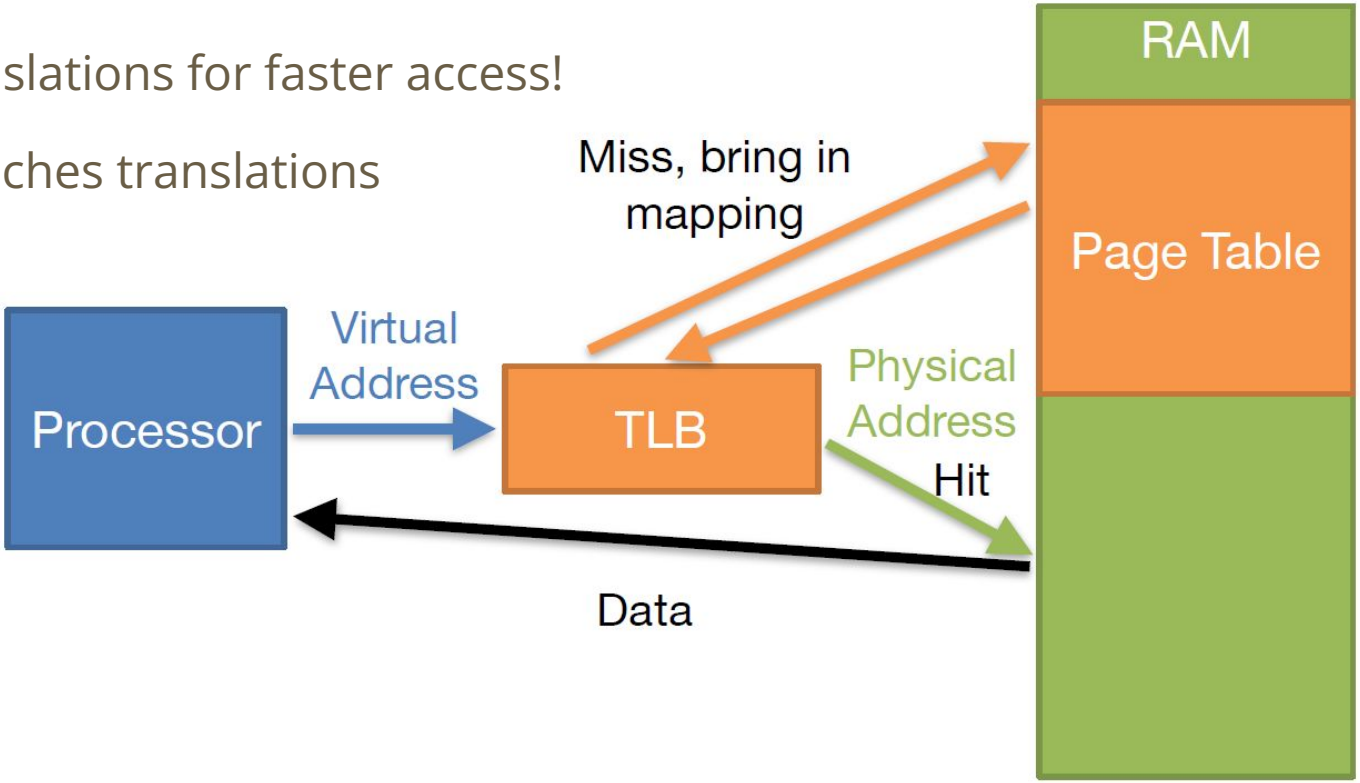
Bonus slides

Putting it all together

Putting it all together

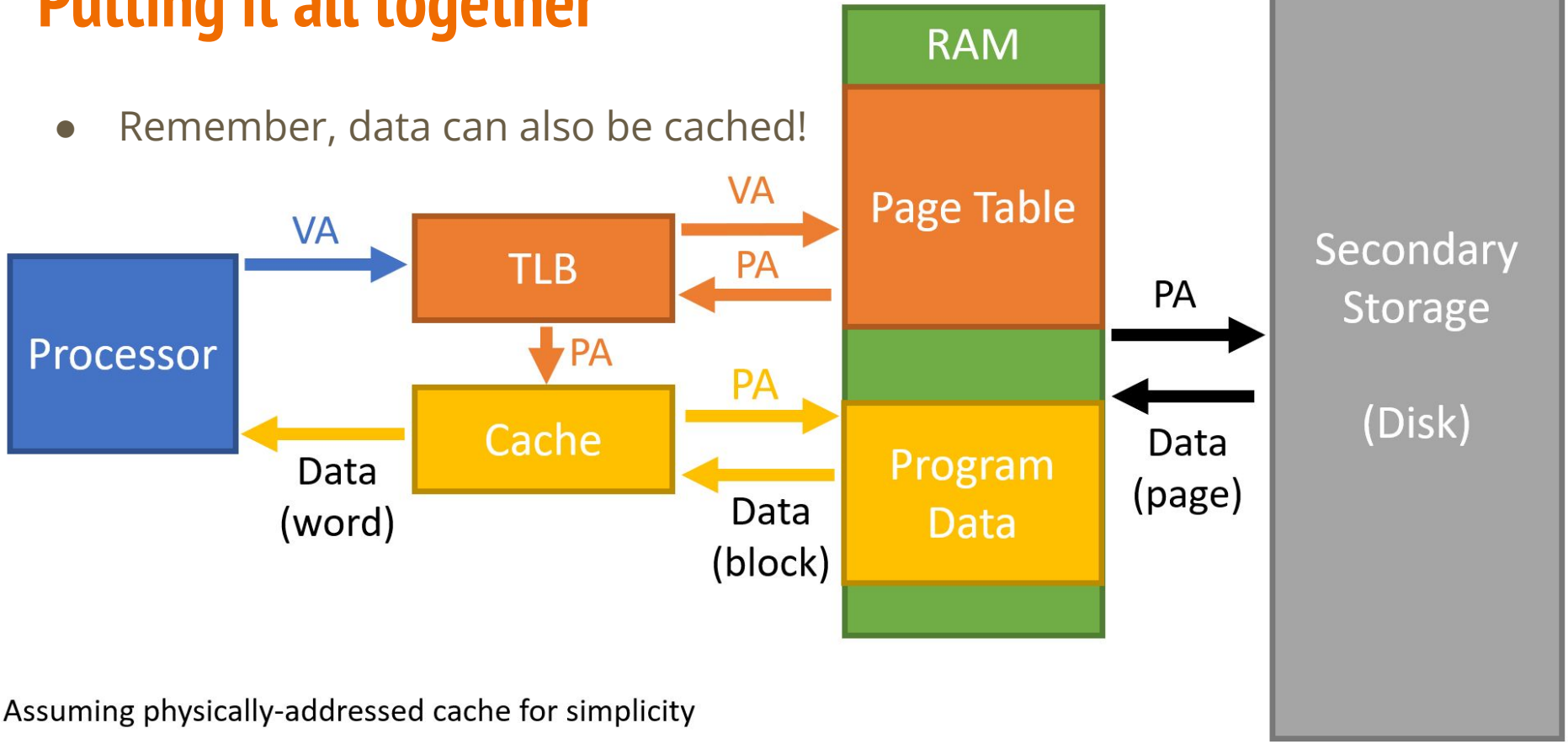
Cache translations for faster access!

- TLB caches translations



Putting it all together

- Remember, data can also be cached!



Assuming physically-addressed cache for simplicity